AAT3532

MicroPower™ Microprocessor Reset Circuit

PowerManager™

General Description

The AAT3532 PowerManager™ product is a member of AATI's Total Power Management ICs™ (TPMIC™) product family. It is a fully integrated device for monitoring microprocessor activity, external reset, and power supply conditions. The device holds the microprocessor in a reset condition for a minimum of 250ms while V_{CC} is established to ensure correct system start-up. A manual reset can be initiated via a de-bounced input pin. As an additional level of protection, the AAT3532 includes a watchdog timer which requires a periodic strobe input from the microprocessor to ensure correct operation. The AAT3532 has a programmable watchdog timer and voltage tolerance level. The quiescent supply current is extremely low, typically 23µA.

The AAT3532 is available in an 8-pin SOP package specified over -40° to 85°C temperature range.

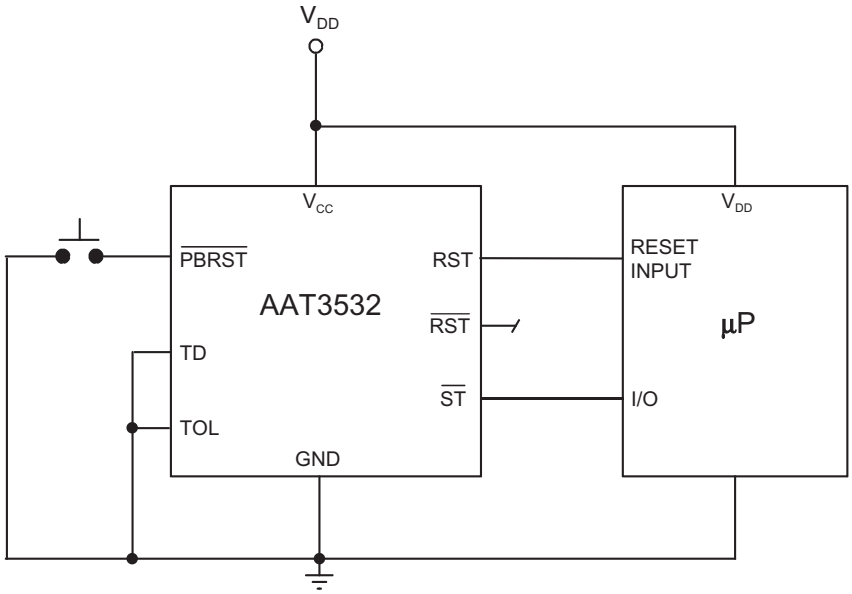
Features

- Adjustable 4.5V or 4.75V Voltage Monitor
- 250ms (min) Reset Pulse Width
- Low quiescent current: typically 23µA
- Adjustable Watchdog Timer (150ms, 600ms, or 1200ms)
- De-bounced Manual Reset Input
- Operates down to 20ns strobe input pulse width
- No external components
- Temp range -40° to 85°C
- Standard 8 pin SOP package
- Pin compatible with MAX1232

Applications

- Computers
- Controllers
- Telecom Equipment
- Embedded Systems
- Intelligent Instrumentation
- Automotive

Typical Application



Preliminary Information

Pin Descriptions

Pin #	Symbol	Function
1	$\overline{\text{PBRST}}$	Pushbutton reset input. A de-bounced active low input for manual reset. Guaranteed to recognize inputs 20ms or greater.
2	TD	Watchdog time delay set input. See Table 1 for watchdog timeout selections.
3	TOL	Tolerance set. Input selects 5% or 10% threshold detection
4	GND	IC ground connection
5	RST	Reset Output (active high). Activated when either: V_{CC} falls below the reset voltage threshold, or $\overline{\text{PBRST}}$ is forced low, or $\overline{\text{ST}}$ not strobed within the minimum timeout period, or during power-up.
6	$\overline{\text{RST}}$	Reset Output (active low, open drain). Inverse of RST.
7	$\overline{\text{ST}}$	Strobe input to watchdog timer. A pulse is required within watchdog timeout period to prevent $\overline{\text{RST}}$ and RST entering active state
8	Vcc	5V Supply

Pin Programming Selections

TD Pin	Time-Out		
	Min	Typ	Max
GND	62.5ms	150ms	250ms
Float	250ms	600ms	1000ms
V_{CC}	500ms	1200ms	2000ms

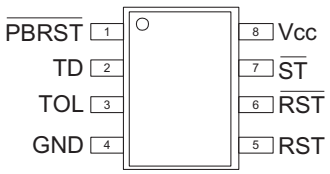
Table 1: TD Pin Programming for Watchdog Timeout Selections

TOL Pin	Tolerance
V_{CC}	10%
GND	5%

Table 2: Reset Voltage Threshold Programming Selections

Pin Configuration

SOP-8
(Top View)



Absolute Maximum Ratings (T_A=25°C unless otherwise noted)

Symbol	Description	Value	Units
V_{CC}	V_{CC} to GND	-0.5 to 6	V
$V_{I/O}$	Voltage on I/O pins relative to GND	-0.5 to (V_{CC}+0.5)	V
T_A	Operating Temperature Range	-40 to 85	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at Leads) for 10s	300	°C
V_{ESD}	ESD Rating[1]—HBM	2000	V

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

Note 1: Human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Thermal Characteristics

Symbol	Description	Value	Units
Θ_{JA}	Maximum Thermal Resistance[2]	100	°C/W
P_D	Maximum Power Dissipation[2]	1.25	W

Note 2: Mounted on an FR4 board.

DC Electrical Characteristics

(V_{IN} = 4.5V to 5.5V, T_A = -40 to 85°C unless otherwise noted. Typical values are at T_A=25°C)

Symbol	Description	Conditions		Min	Typ	Max	Units
V_{CC}	Supply Voltage			4.5	5.0	5.5	V
I_Q	Quiescent Current[1]	V_{CC} = 5.5V	CMOS Levels		23	50	µA
			TTL Levels		160	500	
V_{CCTP}	Reset Threshold 5%	TOL = GND		4.50	4.62	4.74	V
	Reset Threshold 10%	TOL = V_{CC}		4.25	4.37	4.49	V
I_{IL}	Input Leakage $\overline{ST}$, TOL			-1.0		1.0	µA
I_{OH}	Output Current RST[2]	V_{OH} = 2.4V		-8.0			mA
I_{OL}	Current RST[2], $\overline{RST}$	V_{OL} = 0.4V		10.0			mA
V_{IH}	$\overline{ST}$ and $\overline{PBRST}$ Input High			2.0		V_{CC}+0.3	V
V_{IL}	$\overline{ST}$ and $\overline{PBRST}$ Input Low			-0.3		0.8	V
$I_{\overline{RST}}$	$\overline{RST}$ Output Leakage	V_{OH} = V_{CC}				1.0	µA

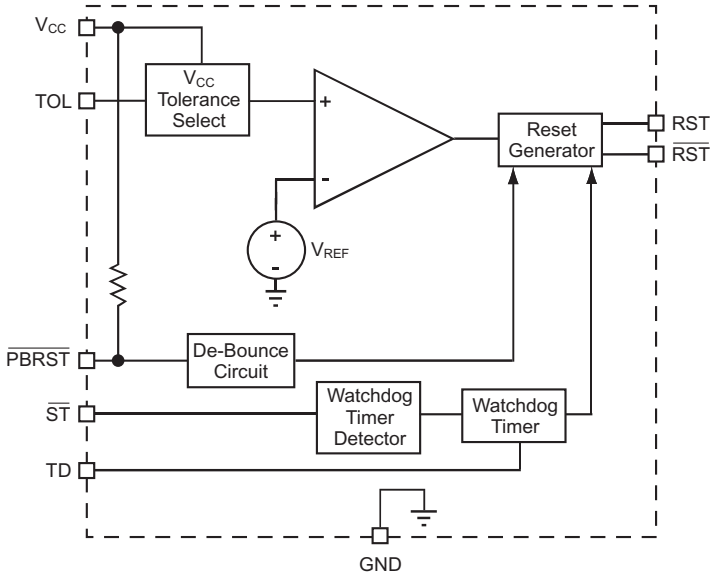
AC Electrical Characteristics

(V_{IN} = 4.5V to 5.5V, T_A = -40 to 85°C unless otherwise noted. Typical values are at T_A=25°C)

Symbol	Description	Conditions	Min	Typ	Max	Units
C_{IN}	Input Capacitance $\overline{ST}$, TOL[3]	T_A = 25ºC			5	pF
C_{OUT}	Output Capacitance RST, $\overline{RST}$[3]	T_A = 25ºC			7	pF
t_{PB}	$\overline{PBRST}$[4]	Fig 2	20			ms
t_{PBD}	$\overline{PBRST}$ Delay	Fig 2	1	4	20	ms
t_{RST}	Reset Active Time		250	610	1000	ms
t_{ST}	$\overline{ST}$ Pulse Width	Fig 3	20			ns
t_{TD}	$\overline{ST}$ Time-out Period	TD Pin = 0V	62.5	150	250	ms
		TD Pin = Open	250	600	1000	ms
		TD Pin = V_{CC}	500	1200	2000	ms
t_f	V_{CC} Fall Time[3]	4.75V to 4.25V	10			µs
t_r	V_{CC} Rise Time[3]	4.25V to 4.75V	0	5		µs
t_{RPD}	V_{CC} Detect to RST High and $\overline{RST}$ Low	V_{CC} Falling			50	µs
t_{RPU}	V_{CC} Detect to RST Low and $\overline{RST}$ Open	V_{CC} Rising	250	610	1000	ms

Notes:
1. Measured with outputs open and $\overline{ST}$ toggling at 100kHz, 50% duty cycle
2. $\overline{RST}$ is an open drain output
3. Guaranteed by design and not subject to production testing.
4. $\overline{PBRST}$ must remain low for greater than 20ms to guarantee a reset

Functional Block Diagram



Applications Information

Power Monitor

The reset function monitors the V_{CC} supply to ensure a microprocessor is correctly reset and is powered up into a known condition following a power supply failure. RST and $\overline{RST}$ will remain valid for Vcc voltages down to 1.4V.

The RST and $\overline{RST}$ pins are asserted whenever V_{CC} drops below the reset threshold voltage. This voltage can be set by programming the TOL pin. Connecting TOL to V_{CC} sets the 10% tolerance of the V_{CC} supply (typically 4.37V for V_{CC} = 5V). Connecting TOL to GND sets the 5% tolerance of the V_{CC} supply (typically 4.62V for V_{CC} = 5V). The reset pin is guaranteed to remain asserted for a minimum period of 250ms after V_{CC} has risen above the reset threshold voltage.

$\overline{RST}$ output is an open drain output. For correct operation, a pull-up resistor of 10kΩ should be connected between this output and V_{CC}.

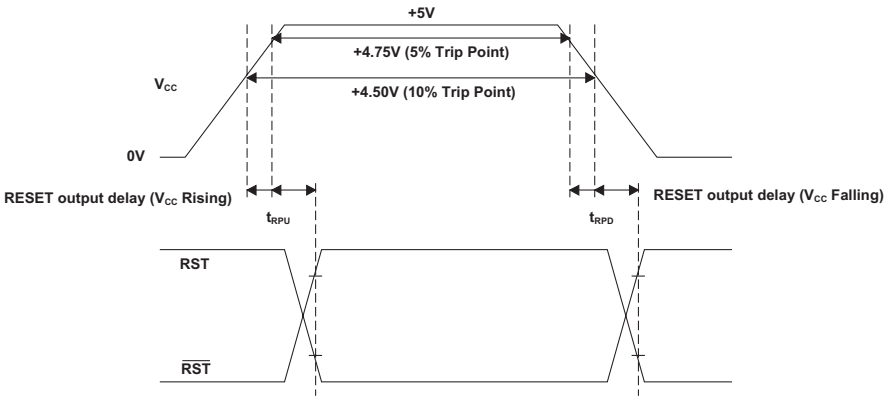


Figure 1. Reset Output Delay

Applications Information

Manual Reset

The $\overline{\text{PBRST}}$ pin makes it possible to manually reset the system by either directly connecting a mechanical push-button between the $\overline{\text{PBRST}}$ pin and GND or connecting to a logic low output. Internal de-bounce circuitry is provided to reduce the effect of noise glitches at the input. The signal should remain low for a minimum of 20ms for correct operation. Once the $\overline{\text{PBRST}}$ signal is released (or goes to a logic high), RESET ($\overline{\text{RESET}}$) remains asserted for a minimum of 250ms.

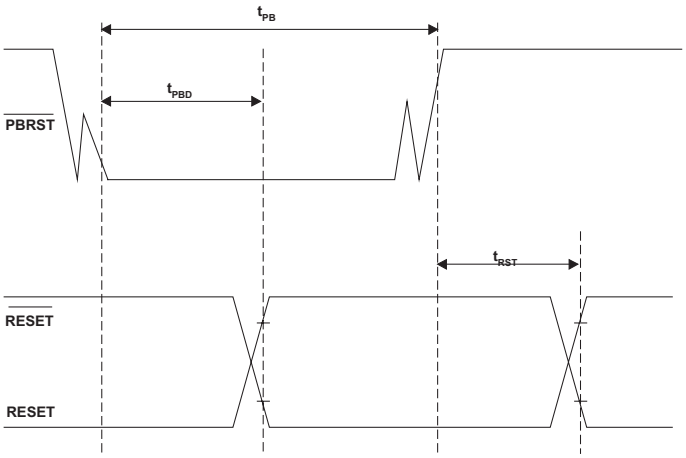


Figure 2 Push-button Reset

Watchdog Timer

The watchdog timer monitors the microprocessor to ensure that the system is functioning correctly. The $\overline{\text{ST}}$ pin of the AAT3532 can be derived from the microprocessor data signals, address signals, and/or I/O signals. The watchdog timer function forces the RST and $\overline{\text{RST}}$ signals into the active state when the $\overline{\text{ST}}$ input is not toggled by a predetermined time. This time period is set by the logic state of the TD pin as shown in Table 1. The timer starts once the RST signals become inactive. If the watchdog timer does not receive a high-to-low transition within the specified timeout period, then the RST signals are activated for a minimum 250ms. In normal operation the timer should receive a transition from the microprocessor within the timeout period, in which case the timer is reset and normal operation continues.

The AAT3532 will accept and recognize $\overline{\text{ST}}$ pulses down to a minimum of 20ns wide.

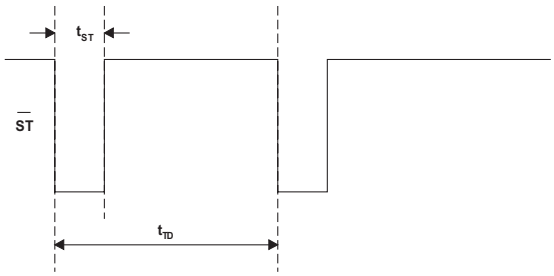


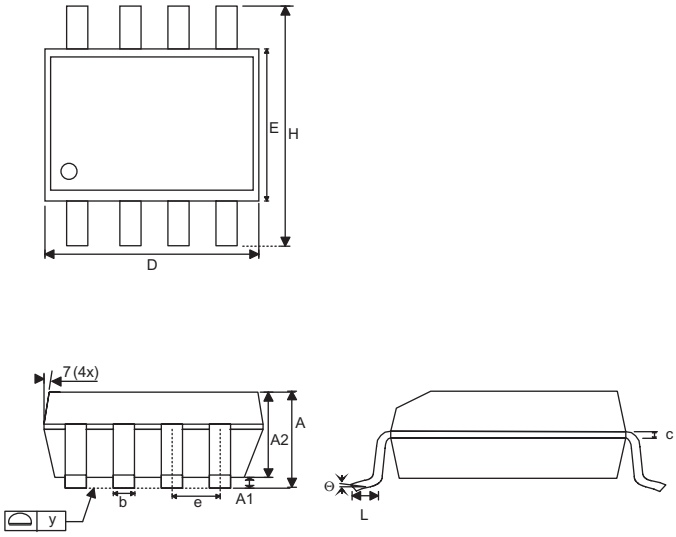
Figure 3. Watchdog Input

Ordering Information

Package	Marking	Part Number	
		Bulk	Tape and Reel
8 Pin SOIC		AAT3532IAS-B1	AAT3532IAS-T1

Package Information

SOP-8



Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.45		0.057	
B	0.33	0.51	0.013	0.020
C	0.19	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	3.80	4.00	0.150	0.157
e	1.27		0.050	
H	5.80	6.20	0.228	0.244
L	0.40	1.27	0.016	0.050
Y	0.00	0.10	0.000	0.004
θ1	0°	8°	0°	8°

Note:
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.
2. TOLERANCE± 0.1000mm (4mil) UNLESS OTHERWISE SPECIFIED
3. COPLANARITY: 0.1000mm
4. DIMENSION L IS MEASURED IN GAGE PLANE.
5. CONTROLLING DIMENSION IS MILLIMETER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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