Micro Circuit Engineering
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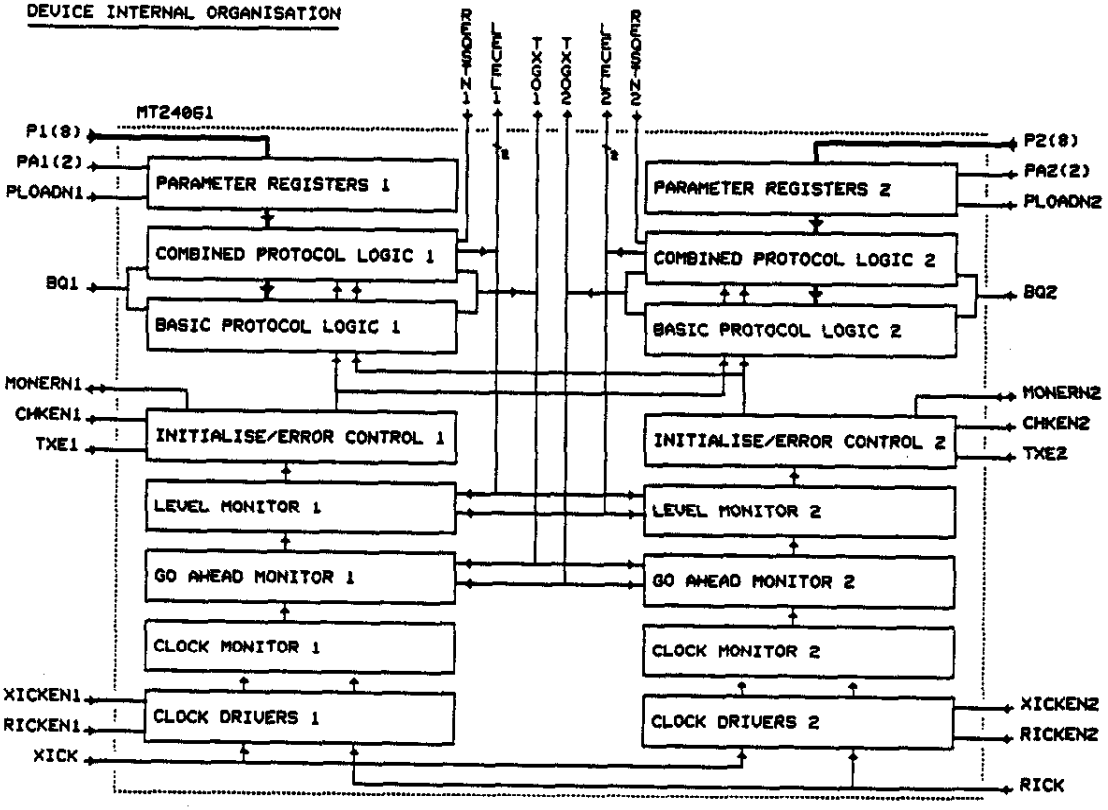
Note: This Device Supercedes MT24061.

DEVICE INTERNAL ORGANISATION



FEATURES

SUPPORTS BOTH BP AND CP DATA BUS SYSTEMS.

USE WITH MCE RECEIVER/MONITOR AND TRANSMITTER CHIPS FOR FULL-FUNCTION ARINC 629 TERMINAL.

SUPPORT FOR BUILT-IN TEST FUNCTIONS.

CONTAINS DUAL PROTOCOL LOGIC CIRCUITS WITH CROSS-MONITORING.

CONFIGURABLE AS TWO INDEPENDENT PROTOCOL UNITS FOR BUS SIMULATOR APPLICATIONS.

LOW POWER CMOS TECHNOLOGY.

48 PIN DIL OR 44 PIN J-LEAD PACKAGES.

1.0 General Description

This device is designed to work with the MCE ARINC 629 Transmitter and receiver/monitor chips. The three chips together implement a full function transmit and receive terminal.

The chip implements the ARINC 629 bus access protocol logic for both BP and CP modes of operation. It uses Bus Quiet and other inputs to generate a Go-Ahead signal (TXGO) commanding the transmitter chip to start sending a message at the appropriate time. In CP mode it also generates output signals to indicate the current level of operation and examines an input to see if there is a request pending at this level.

The chip contains two copies of the protocol logic with independent sources of timing parameters, and it uses two independent clock signals. Dual monitor circuits check the two protocol circuits agree on Go-Ahead time and current level of operation (CP), and also check the frequencies of the two clock sources agree within specified tolerances. When any disagreement is detected, a bi-directional signal (MONERN) is pulled low and the protocol circuits are re-initialised. The MONERN signal may be used to increment an error counter in the receiver/monitor chip. MONERN may be pulled low by the receiver/monitor chip to indicate a bus clash or transmission error has been detected. When this happens, the protocol logic executes the clash recovery sequence specified in the ARINC standard.

Facilities are provided to allow in-system testing of the protocol monitoring logic. This is vital to prevent the build-up of latent faults in the monitoring logic which can prevent the detection of faults in the protocol circuits. Four separate clock enables are provided to allow simulation of timing errors. Different groups of clocks may be inhibited for a few cycles to simulate timer and clock frequency errors. The width of the resulting MONERN output pulse indicates whether neither, one or both of the monitor circuits detected the discrepancy. A future application note will deal with this subject in detail.

The protocol chip can be specially configured for applications in bus simulator equipment. These units can contain many terminals, but high integrity is not needed. In these cases, the monitoring functions may be disabled, and the chip operated as two independent protocol circuits with separate Go-Ahead outputs, separate timing parameters and separate clock sources. Many protocol circuits may be used with a single receiver/monitor and transmitter chip.

The device includes strap inputs to enable extensions to the protocol which are currently under evaluation.

2.0 Bus Access Timing Parameters

When the chip is used with MCE transmitter and receiver/monitor chips, timing parameters are loaded as follows. Timing parameters for the first channel are stored in the RPP prom and loaded under the control of the receiver chip. Timing parameters for the second channel are stored in the XPP prom and loaded through a separate port under the control of the transmitter chip. Each channel is loaded with 3 bytes using 8 parallel data inputs, two address inputs and a load input. Both channels must be loaded with the same parameter values. The protocol circuits will not operate until all parameters have been loaded. Parameters may be re-loaded at any time, but changing values or BP/CP modes without disabling the chip first is likely to cause erroneous behaviour.

Channel	Address Inputs	Data inputs
1	PA11,PA10	P17,P16,P15,P14,P13,P12,P11,P10
2	PA21,PA20	P27,P26,P25,P24,P23,P22,P21,P20

Address		Parameters Loaded
1	0	SG1,TI6,TI5,TI4,TI3,TI2,TI1,TI0
1	1	SG0,TG6,TG5,TG4,TG3,TG2,TG1,TG0
0	1	BCP,ML6,ML5,ML4,ML3,ML2,ML1,ML0

TI6-0, SG1-0, TG6-0 are the binary values for Transmit Interval, Synchronisation Gap, and Terminal Gap timers respectively as defined in the ARINC 629 standard. BCP is a single bit BP/CP mode selector, BCP=1 for BP, BCP=0 for CP. ML6-0 is a binary value to set the AT timer (CP only). It specifies the time difference between TI and AT. This time difference must be set greater than (MAL + PSG) where MAL is the longest level 2 or 3 message length. Time differences map onto ML binary values as follows:

ML	Time Difference (>MAL+PSG)
3	118μS
4	149μS
.	....
.	....
126	3962μS
127	3993μS

The specific formula for AT is:

AT = (0.5(TI+1)+0.0005625)mS - (31.25(ML+1)-7)μS.

where TI and ML are the respective binary values.

AT may vary by up to ±2μS from the calculated value due to logic and synchronisation delays.

3.0 Initialisation and Error Recovery

The TXE inputs initialise and enable the protocol circuits. After taking TXE low to high, all timing parameters must be loaded before the chip becomes active. This prevents the protocol operating with invalid parameter values. When a discrepancy is detected by the monitoring circuits, an error output is asserted (MONERN) and the protocol circuits are initialised and immediately re-started. The two protocol circuits are reset and started at the same time even when the error is detected by only one of the monitor circuits. It is not necessary to re-load the timing parameters after MONERN.

When MONERN is pulled low by an external device, the protocol circuits are forced to hold their TG counters in the reset state until the next time TI elapses. This is the collision recovery action specified in the ARINC standard.

4.0 Signals

Note: Some signals are not bonded out independently in the standard package options. Special bonding options may be ordered from MCE.

P17-P10 & P27-P20

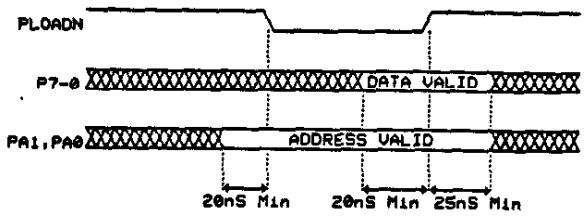
Two 8 bit data input busses for parameter loading. P17-P10 are used to load channel 1. P27-P20 are used to load channel 2. P17 and P27 are the most significant bits. Internal register data fields are defined in section 2.0.

PA11,PA10 & PA21,PA20

Two 2 bit address input busses for parameter loading. PA11,PA10 are used to load channel 1. PA21,PA20 are used to load channel 2. Internal register addresses are defined in section 2.0.

PLOADN1 & PLOADN2

Active low inputs to load parameters for each channel.



JITENN

This strap input enables an extension to the protocol associated with clash recovery on fibre-optic busses. This is an experimental feature currently under investigation. Tie this input high for standard protocol operation.

CPMOD

This strap input enables an extension to the combined protocol (CP) associated with improving bus utilisation at level 3. This is an experimental feature currently under investigation. Tie this input low for standard protocol operation.

RICK & XICK

Two independent clock inputs. RICK is the receiver clock. XICK is the transmitter clock. These should be 32MHz for a 2M bus bit rate. Minimum pulse high or low time is 12.5nS. The frequency should be maintained within ±0.01% of nominal under all conditions.

RICKEN1, XICKEN1, RICKEN2, XICKEN2

Active high clock enable inputs to the two protocol channels. Each channel uses both XICK and RICK, and each may be enabled independently. The use of these inputs for in-system testing of the monitoring logic will be described in a separate application note. For normal operation all of these inputs should be tied high.

CHKEN1 & CHKEN2

These active high strap inputs enable the monitoring circuits. For normal operation they should be both tied high. They should be both tied low only when the two protocol channels are being used independently and monitoring is not required.

TXE1 & TXE2

Active high enable inputs to the two protocol channels. These signals will be normally tied together and driven from TXE on the receiver/monitor chip. They are internally linked to a single pin on the 44 pin j-lead package option.

MONERN1 & MONERN2

Bi-directional active low error signals from/to each protocol channel. A low going output pulse indicates the monitoring circuits have detected a discrepancy between the two protocol channels or clocks. These signals have open-drain drivers and they should be normally joined together (they are internally linked on the 44 pin j-lead package option). When one monitor channel detects an error, the MONERN pulse width is nominally 593.75nS wide (low). When the two MONERN signals are linked and both monitor channels detect an error, the resulting pulse width is nominally 1093.75nS. On input MONERN should be pulled low for a minimum of 25nS to initiate clash recovery action.

LVL11,LVL10 & LVL21,LVL20

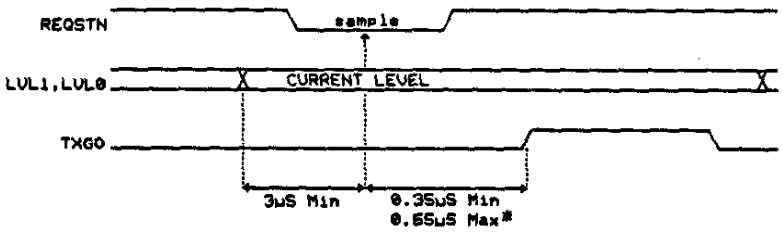
Two 2 bit output busses indicating the current level of operation. In BP mode they always indicate level 1. LVL11,LVL10 are outputs from protocol channel 1. LVL21,LVL20 are outputs from protocol channel 2. The levels are encoded as follows:

LVLx1,LVLx0	LEVEL
0 0	Level 1
0 1	Level 2
1 1	Level 3 Backlog
1 0	Level 3 New

In normal use both channels will output the same levels. Only one channel is used to drive the associated transmitter chip. Channel 2 outputs are not brought out to pins on the 44 pin j-lead package option.

REQSTN1 & REQSTN2

Active low inputs tell the protocol logic there is a request pending at the current level (indicated by the LVLxx outputs). These inputs are sampled just before each transmission opportunity. The Go-Ahead signal will only be issued if there is a request pending. REQSTN1 controls protocol channel 1 and REQSTN2 controls protocol channel 2. They are normally linked together and driven from the REQSTN output of the associated transmitter chip. They are internally linked and brought out to a single pin on the 44 pin J-lead package option.



* This time can be much longer in BP and CP Level 1 when TXGO is controlled by TI.

BQ1 & BQ2

Active high Bus Quiet inputs generally driven from the BQ output of the associated receiver chip. The protocol timers are optimised for a median delay of 190nS from the end of the last bit of a wordstring at the receiver inputs (RXI/RXN) to the assertion of BQ. BQ1 controls protocol channel 1 and BQ2 controls protocol channel 2. They are normally linked together. They are internally linked and brought out to a single pin on the 44 pin J-lead package option.

TXGO1 & TXGO2

Active high transmit go-ahead output to the associated transmitter chip. Nominal pulse width is 250nS. TXGO1 is generated by protocol channel 1 and TXGO2 is generated by protocol channel 2.

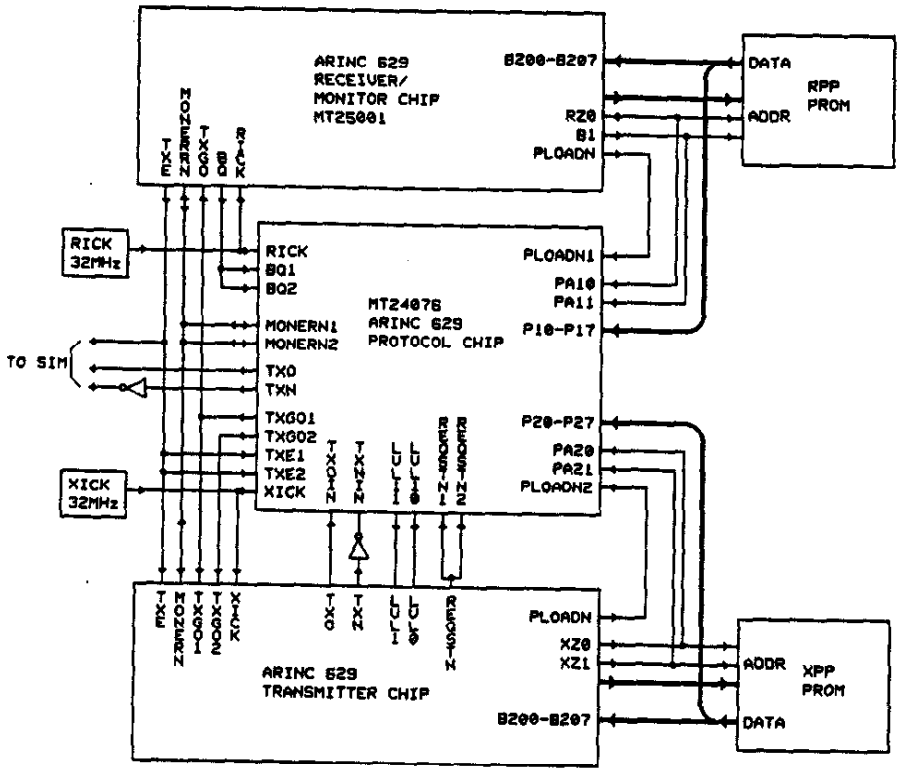
TXOIN & TXNIN

Manchester encoded data inputs from the Transmitter chip (MT25003). Note that TXNIN must be inverted between MT25003 and this chip using an external inverter with propagation delay of less than 10nS.

TXO & TXN

Manchester encoded data outputs to the SIM. The protocol chip reconstructs the missing parity bit in data from the transmitter and delivers the corrected data to the SIM with a one clock cycle (31.25nS) delay from TXOIN/TXNIN. Note that TXN must be inverted between this chip and the SIM using an external inverter.

5.0 Interconnection of Transmit, Receive and Protocol chips



6.0 Configuring the chip as Two Independent Protocol Circuits

This requires a special bonding option with CHKEN1 & 2 tied low and MONERN1 & MONERN2 bonded out to separate pins. XICK should be tied high and RICK should be tied low. Channel 1 clock is supplied to XICKEN1 and channel 2 clock is supplied to XICKEN2. CHKEN1 & CHKEN2 are both tied low to disable the monitor circuits. This also disables the check for valid timing parameters before activating the protocol circuits. The protocol circuits are now activated immediately TXE is taken high. Timing parameters are loaded in the usual way except the two channels may be supplied with different values. JITENN and CPMOD are common and so will be configured the same in both channels. TXE1, REQSTN1, BQ1, LVL11,LVL10 & TXGO1 are associated with channel 1 only. TXE2, REQSTN2, BQ2, LVL21,LVL20 & TXGO2 are associated with channel 2 only. MONERN1 is only used as an input to signal clash detection to channel 1. MONERN2 performs the same function for channel 2.

7.0 General Electrical Characteristics

All timing parameters are specified for the following conditions unless otherwise stated:

Ambient temperature range -55°C to 125°C
VDD voltage range 4.5v to 5.5v
Output load Capacitance 50pF
Falling edge measurements are made to Vol=0.8v
Rising edge measurements are made to Voh=2.0v

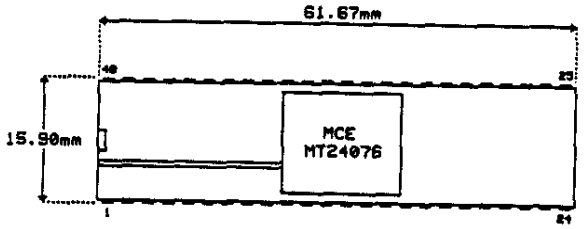
All outputs have 4mA drive except TXGO1 & TXGO2 which have 8mA drive.

MONERN1 & MONERN2 are open drain output stages.

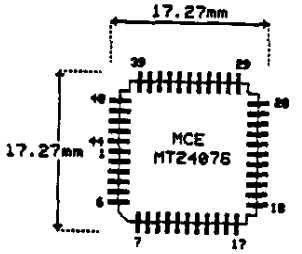
The following signals have internal high value (50KΩ approx.) pullup resistors:
JITENN, CPMOD, CHKEN1, CHKEN2, PLOADN1, PLOADN2, RICKEN1, RICKEN2, XICKEN1, XICKEN2, MONERN1, MONERN2.

The following signals have internal high value (50KΩ approx.) pulldown resistors:
BQ1, BQ2, TXE1, TXE2.

8.0 Package Outline



48 PIN DIL CERAMIC PACKAGE
TOP VIEW



44 PIN J-LEAD PACKAGE
TOP VIEW

9.0 Pin Assignments

48 Pin DIL Package

Pin	Signal	Pin	Signal
1	P14	25	P27
2	P15	26	P21
3	P16	27	P22
4	P17	28	P20
5	BQ2	29	PA20
6	BQ1	30	PA21
7	VSS (0v)	31	XICK
8	TXE2	32	RICKEN2
9	TXE1	33	XICKEN2
10	TXGO1	34	TXOIN
11	MONERN	35	CPMOD
12	TXO	36	LVL21
13	PLOADN1	37	LVL20
14	PLOADN2	38	TXNIN
15	TXGO2	39	RICKEN1
16	LVL10	40	XICKEN1
17	LVL11	41	TXN
18	VDD (+5v)	42	RICK
19	REQSTN2	43	P12
20	REQSTN1	44	P11
21	P23	45	P10
22	P24	46	PA10
23	P25	47	PA11
24	P26	48	P13

44 Pin J-Lead Package

Pin	Signal	Pin	Signal
1	P13	23	P27
2	P14	24	P21
3	P15	25	P22
4	P16	26	P20
5	P17	27	PA20
6	BQ	28	PA21
7	VSS (0v)	29	XICK
8	TXE	30	RICKEN2
9	TXGO1	31	XICKEN2
10	MONERN	32	TXOIN
11	TXO	33	CPMOD
12	PLOADN1	34	VSS(0v)
13	PLOADN2	35	TXNIN
14	TXGO2	36	RICKEN1
15	LVL10	37	XICKEN1
16	LVL11	38	TXN
17	VDD (+5v)	39	RICK
18	REQSTN	40	P12
19	P23	41	P11
20	P24	42	P10
21	P25	43	PA10
22	P26	44	PA11

Note: JITENN, CHKEN1 & CHKEN2 are not bonded out. MONERN1 & MONERN2 are both bonded to a single pin. Special bonding options are available from MCE.

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