CT2566
MIL-STD-1553 to Microprocessor Interface Unit

Features

- ***Second Source** Compatible to the **BUS-66300***
- **PGA Version available, (second source to the BUS-66312)**
- **Compatible with MIL-STD-1750 CPUs**
- **Compatible with MOTOROLA, INTEL, and ZILOG CPUs**
- **Compatible with Aeroflex's CT2565 BC/RT/MT and CT2512 RT**
- **Minimizes CPU overhead**
- **Signal controls for shared memory implementation**
- **Transfers complete messages to shared memory**
- **Provides memory mapped 1553 interface**
- **Packaging – Hermetic Metal**
  - **78 Pin, 2.1" x 1.87" x .25" PGA type package**
  - **82 Lead, 2.2" x 1.61 x .18" Flat Package**

AEROFLEX CIRCUIT TECHNOLOGY
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Description

Aeroflex CT2566 MIL-STD-1553 to Microprocessor Interface Unit simplifies the CPU to 1553 Data Bus interface. The CT2566 provides an interface by using RAM allowing the CPU to transmit or receive 1553 traffic simply by accessing the memory. All 1553 message transfers are entirely memory or I/O mapped. The CT2566 supports 1553 interface devices such as Aeroflex's CT2512 dual RT or the CT2565 dual BC, RT, and MT. The CT2566 operates over the full military -55°C to +125°C temperature range.

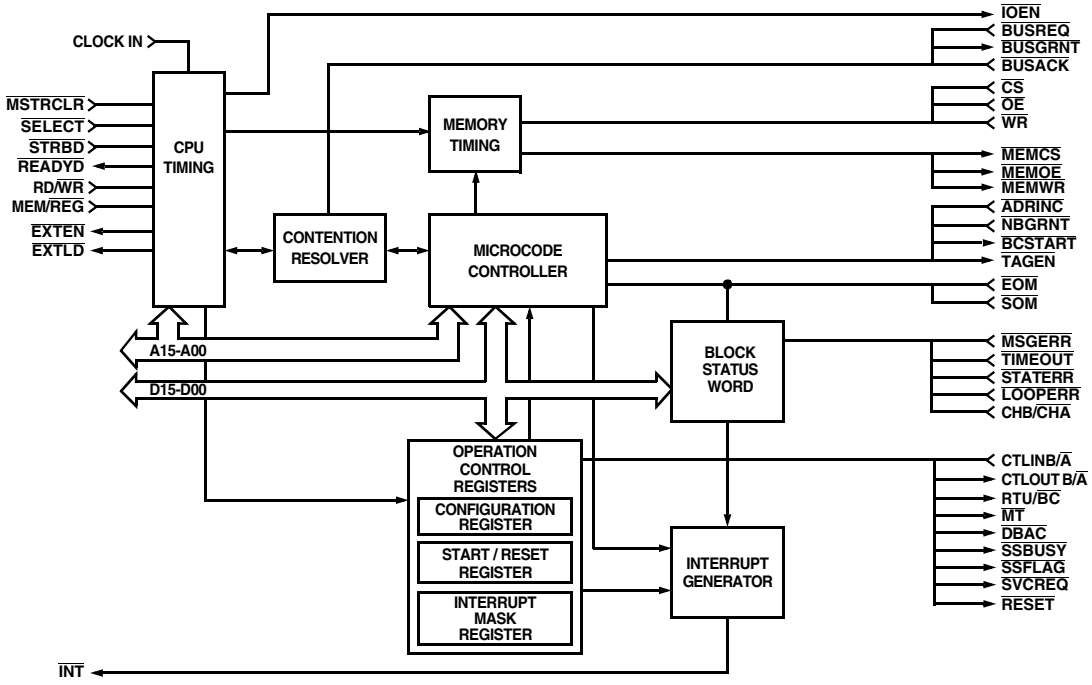


Figure 1 – Functional Block Diagram

Specifications at Nominal Power Supply Voltages

PARAMETER	VALUE	UNITS
Logic		
I_{IH} (With V_{IH} = 2.7V)	–630	µA
I_{IL} (With V_{IL} = 0.0V)	–700	µA
I_{OH}	4.0 min	mA
I_{OL}	4.0	mA
V_{IH}	2.0	V
V_{IL}	0.8	V
V_{OH}	3.7	V
V_{OL}	0.4	V
Clock	12	MHz
Power Supplies		
Voltage	5.0±10%	V
Current Drain	10 typ	mA
Temperature Range		
Operating (Case)	–55 to +125	°C
Storage	–65 to +150	°C
Physical Characteristics		
Size		
78 pin DIP	2.1 x 1.87 x 0.25 (53 x 47.5 x 6.4)	in (mm)
82 pin flatpack	2.1 x 1.87 x 0.25 (55.6 x 40.6 x 3.71)	in (mm)
Weight		
78 pin DIP	1 (28)	oz (g)
82 pin flatpack	1 (28)	oz (g)

Table 1 – Specifications

GENERAL

The CT2566 was designed to perform required handshaking to the 1553 interface device, storing or retrieving message(s) from a user supplied RAM and notifying the CPU that a 1553 transaction has occurred. The CPU uses this RAM to read the received data as well as to store messages to be transmitted onto the Bus.

The CT2566 can be used to implement BC, RT, or MT operation and can be either memory mapped or I/O mapped to CPU address space. Registers internal to the CT2566 control its operation.

The CT2566 can access up to four external, user supplied registers and can address up to 64K words of RAM. The RAM selected must be a non-latched static RAM (capable of meeting the timing constraints for the CT2566). A double buffering architecture is provided to prevent incomplete or partially updated information from being transmitted onto the 1553 Data Bus.

The CT2566 requires an external, user supplied clock.

COMPATIBLE MICROPROCESSOR TYPES

The CT2566 may be used with most common microprocessors, including, the Motorola 68000 family, the Intel 8080 family, Zilog Z8000 products, and available MIL-STD-1750 processors.

Interfacing the CT2566 to the 1553 Data Bus requires external circuitry such as Aeroflex's CT2565(BC/RT/MT) and ACT4489D transceivers. Figure 2 shows the interconnection for these components.

PIN NO.	NAME	I/O	DESCRIPTION
1	$\overline{\text{SELECT}}$	I	Select. When active, selects CT2566 for operation.
2	RD/$\overline{\text{WR}}$	I	Read/Write. Controls CPU bus data direction.
3	$\overline{\text{READYD}}$	O	Ready Data. When active indicates data has been received from, or is available to the CPU.
4	$\overline{\text{EXTEN}}$	O	External Enable. Output from CT2566 to enable output from external devices. Same timing as $\overline{\text{MEMOE}}$.
5	$\overline{\text{TAGEN}}$	O	Tag Enable. Enables an external time tag counter for transferring the time tag word into memory.
6	$\overline{\text{EOM}}$	I	End of Message. Input from 1553 device indicating end of message.
7	$\overline{\text{SOM}}$	I	Start of Message. Input from 1553 device indicating start of message in RTU mode.
8	$\overline{\text{STATERR}}$	I	Status Error. Input from 1553 device when status word has either a bit set or unexpected RT address (in BC mode only).
9	$\overline{\text{ADRINC}}$	I	Address Increment. Sent from 1553 device to increment address counter following word transfer.
10	MEM/$\overline{\text{REG}}$	I	Memory/Register. Input from CPU to select memory or register data transfer.
11	CLOCK IN	I	Clock input; 50% duty cycle, 12MHz, max.
12	$\overline{\text{LOOPERR}}$	I	Loop Error. Input from 1553 device if short loop BIT fails.
13	$\overline{\text{BUSREQ}}$	I	Bus Request. When active, indicates 1553 device requires use of the address/data bus.
14	$\overline{\text{BUSGRNT}}$	O	Bus Grant. Handshake output to 1553 device in response to BUS REQUEST indicating address/data bus available to 1553 device.
15	Not Used	-	-
16	$\overline{\text{MEMCS}}$	O	Memory Chip Select. Low from CT2566 to enable external RAM. Used with 4K x 4 RAM type device to read RAM or used in conjunction with $\overline{\text{MEMWR}}$ to write data into RAM.
17	$\overline{\text{OE}}$	I	Output Enable. Input from 1553 device used to enable memory on the parallel bus.
18	N/C	-	Not Used.
19	$\overline{\text{NBGRNT}}$	I	Low pulse from 1553 device preceding start of received new protocol sequence. Used with superseding command to reset DMA in progress.
20	+ 5 Volt	I	Logic power supply.
21	D15	I/O	Data Bus Bit 15 (MSB).
22	D13	I/O	Data Bus Bit 13.
23	D11	I/O	Data Bus Bit 11.
24	D09	I/O	Data Bus Bit 9.
25	D07	I/O	Data Bus Bit 7.
26	D05	I/O	Data Bus Bit 5.
27	D03	I/O	Data Bus Bit 3.

Table 2 – Pin Functions (78 Pin DIP)

PIN NO.	NAME	I/O	DESCRIPTION
28	D01	I/O	Data Bus Bit 1.
29	$\overline{\text{SSFLAG}}$	O	Subsystem Flag. Output to 1553 device to set RT subsystem flag status bit.
30	$\overline{\text{SSBUSY}}$	O	Subsystem Busy. Output to 1553 device to set RT subsystem busy flag.
31	RTU/$\overline{\text{BC}}$	O	Output to 1553 device used in conjunction with MT to set operating mode.
32	A14	O	Address Bit 14.
33	A12	O	Address Bit 12.
34	A10	O	Address Bit 10.
35	A08	O	Address Bit 8.
36	A06	O	Address Bit 6.
37	A04	O	Address Bit 4.
38	A02	I/O	Address Bit 2.
39	A00	I/O	Address Bit 0 (LSB).
40	GND	-	Signal Return.
41	$\overline{\text{STRBD}}$	I	Strobe Data. Used in conjunction with $\overline{\text{SELECT}}$ to indicate a data transfer cycle to/from CPU.
42	$\overline{\text{IOEN}}$	O	Input/Output Enable. Output from CT2566 to enable external buffers/latches connecting the hybrid to the address/data bus.
43	$\overline{\text{EXTLD}}$	O	External Load. Used to load data into external device via the CT2566 data bus. Same timing as $\overline{\text{MEMWR}}$.
44	CHB/$\overline{\text{CHA}}$		Input from 1553 in RT mode used to indicate received 1553 message came in either Channel A or B.
45	$\overline{\text{INT}}$	O	Interrupt. Interrupt pulse line to CPU.
46	$\overline{\text{BCSTART}}$	O	Bus Controller Start. Outputs to 1553 in initiate BC cycle.
47	$\overline{\text{RESET}}$	O	Reset. Output to external device from CT2566 consisting of the OR condition of CPU reset and CPU Master Clear.
48	MSGERR	I	Message Error. Input from 1553 device when an error occurs in message sequence.
49	CTLIN B/$\overline{\text{A}}$	I	Input to change active memory map area (0 = area A).
50	CTLOUT B/$\overline{\text{A}}$	O	Output from CT2566 selecting which area is to be active (0 = area A).
51	$\overline{\text{TIMEOUT}}$	I	Input from 1553 device indicating no response time-out.
52	$\overline{\text{MSTRCLR}}$	I	Master Clear. Power-on reset from CPU. Resets DMA in progress and internal registers to logic “0”.
53	$\overline{\text{BUSACK}}$	I	Bus Acknowledge. Input from 1553 device acknowledge receipt of $\overline{\text{BUSGRNT}}$.
54	$\overline{\text{WR}}$	I	Write. Input from 1553 device for writing data into memory.
55	$\overline{\text{CS}}$	I	Chip Select. Input from 1553 device that is routed to $\overline{\text{MEMCS}}$.

Table 2 – Pin Functions (78 Pin DIP) (Cont.)

PIN NO.	NAME	I/O	DESCRIPTION
56	$\overline{\text{MEMOE}}$	O	Memory Output Enable. Output from CT2566 to enable memory output data.
57	MEMWR	O	Memory Write. Output pulse from CT2566 to write data bus data into memory.
58	Not Used	-	-
59	$\overline{\text{MT}}$	O	Bus Monitor. Used in conjunction with RTU/$\overline{\text{BC}}$ to set operating mode.
60	D14	I/O	Data Bus Bit 14.
61	D12	I/O	Data Bus Bit 12.
62	D10	I/O	Data Bus Bit 10.
63	D08	I/O	Data Bus Bit 8.
64	D06	I/O	Data Bus Bit 6.
65	D04	I/O	Data Bus Bit 4.
66	D02	I/O	Data Bus Bit 2.
67	D00	I/O	Data Bus Bit 0 (LSB).
68	$\overline{\text{SVCREQ}}$	O	Service Request. Used to set service request bit in RT Status Word.
69	$\overline{\text{DBAC}}$	O	Dynamic Bus Acceptance. Used to set status bit in RT Status Word.
70	A15	O	Address Bit 15 (MSB).
71	A13	O	Address Bit 13.
72	A11	O	Address Bit 11.
73	A09	O	Address Bit 9.
74	A07	O	Address Bit 7.
75	A05	O	Address Bit 5.
76	A03	O	Address Bit 3.
77	A01	I/O	Address Bit 1.
78	GND	-	Chassis Ground.

Table 2 – Pin Functions (78 Pin DIP) (Cont.)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	N/C	42	N/C
2	$\overline{\text{SELECT}}$	43	GROUND
3	$\overline{\text{STRBD}}$	44	CHASSIS GROUND
4	RD/$\overline{\text{WR}}$	45	A00 (LSB)
5	$\overline{\text{IOENBL}}$	46	A01
6	$\overline{\text{READYD}}$	47	A02
7	$\overline{\text{EXTLD}}$	48	A03

Table 3 – CT2566FP Pin Functions (82 Pin Flat Package)

PIN NO.	FUNCTION	PIN NO.	FUNCTION
8	$\overline{\text{EXTEN}}$	49	A04
9	CHB/$\overline{\text{CHA}}$	50	A05
10	$\overline{\text{TAGEN}}$	51	A06
11	$\overline{\text{INT}}$	52	A07
12	$\overline{\text{EOM}}$	53	A08
13	$\overline{\text{BCSTART}}$	54	A09
14	$\overline{\text{SOM}}$	55	A10
15	$\overline{\text{RESET}}$	56	A11
16	$\overline{\text{STATERR}}$	57	A12
17	$\overline{\text{MSGERR}}$	58	A13
18	$\overline{\text{ADRINC}}$	59	A14
19	CTLIN B/$\overline{\text{A}}$	60	A15
20	MEM/$\overline{\text{REG}}$	61	RTU/$\overline{\text{BC}}$
21	CTLOUT B/$\overline{\text{A}}$	62	$\overline{\text{DBAC}}$
22	CLOCK IN	63	$\overline{\text{SSBUSY}}$
23	$\overline{\text{TIMEOUT}}$	64	$\overline{\text{SVCREQ}}$
24	$\overline{\text{LOOPERR}}$	65	$\overline{\text{SSFLAG}}$
25	$\overline{\text{MSTRCLR}}$	66	D00
26	$\overline{\text{BUSYREQ}}$	67	D01
27	$\overline{\text{BUSACK}}$	68	D02
28	$\overline{\text{BUSGRNT}}$	69	D03
29	$\overline{\text{WR}}$	70	D04
30	N/C	71	D05
31	$\overline{\text{CS}}$	72	D06
32	$\overline{\text{MEMCS}}$	73	D07
33	$\overline{\text{MEMOE}}$	74	D08
34	$\overline{\text{OE}}$	75	D09
35	$\overline{\text{MEMWR}}$	76	D10
36	Not Used	77	D11
37	N/C	78	D12
38	$\overline{\text{NBGRNT}}$	79	D13
39	$\overline{\text{MT}}$	80	D14
40	+5V	81	D15
41	N/C	82	N/C

Table 3 – CT2566FP Pin Functions (82 Pin Flat Package) (Cont.)

MEMORY MANAGEMENT

The RAM used by the CT2566 can be any standard static memory with a WRITE STROBE pulse width requirement less than 70ns. The RAM area is broken down into pointers, look-up tables, and data blocks. All 1553 operation control is accomplished through the RAM, including fault monitoring and data block transfers.

For most applications, a 4K x 16 memory is sufficient to store the number of messages, but the CT2566 can access up to 64K words.

DOUBLE BUFFERING

A Double Buffering system is available to prevent partially updated data blocks from being read by the CPU or transferred onto the 1553 Data Bus. To use Double Buffering the CPU must divide the RAM into two areas: “current” and “non-current”. Two Stack Pointers, Descriptor Stacks, and Look-Up Tables are required to be used by the CPU.

The 1553 device has access only to the current area of RAM, and will use the current Descriptor Stack and Look-Up Table. While the 1553 device is processing messages using the current area pointers, the CPU can be setting up the next set of messages in the non-current area of RAM.

Once an EOM or BCEOM occurs, the CPU can swap the current and non-current areas by toggling bit 13 of the Configuration Register (See register section for description). The 1553 device will then have access to the new current area. Meanwhile, the CPU can begin processing the data received during the previous transfer or can begin setting up the next set of 1553 messages.

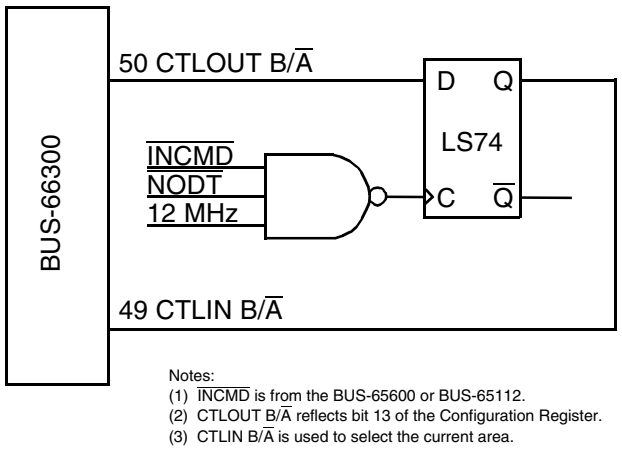


Figure 3 – Synchronized map switching the CT2566

An external circuit (shown in Figure 3) can be added to ensure that the swapping of the current and non-current areas doesn’t occur while the CT2566 is processing a message from the 1553 device. During message processing, the $\overline{INCMD}$ is a logic "0" and the CPU’s map area selection is inhibited. CTLIN B/$\overline{A}$ will be automatically latched back into the CT2566 when $\overline{INCMD}$ and NODT change to a logic "1".

DESCRIPTOR STACK

The CT2566 uses a Descriptor Stack in BC and RTU modes. Each stack entry contains four words which refer to one 1553 message (See Figure 4). The Block Status Word, shown in Figure 5, indicates the physical bus which received the message (RTU mode), reports whether or not an error was detected during message transfer, and indicates whether the message was completed (SOM replaced with EOM).

The user-supplied Time-Tag word is loaded at the start of a message transfer and is updated at the end of the transfer.

The contents of the fourth word in the Descriptor Stack depends on the operating mode. In BC mode, it contains the address of the message data block containing the 1553 message formatted as shown in Figure 6. In RTU mode, the word contains the received 1553 Command Word as shown in Figure 7.

A Stack Pointer must be initialized by the CPU. The Descriptor Stack contains 64, four word entries, and

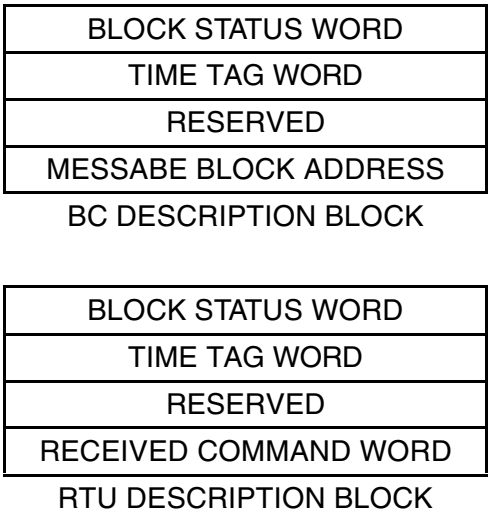


Figure 4 – Descriptor Stack Entries

automatically wraps around (the 64th entry is followed by the first entry). The 1553 device uses the current area Stack Pointer to determine the address of the Stack entry to be used for the current 1553 message. The CT2566 automatically increments the current area Stack Pointer by four upon the completion of each

message regardless of whether or not an error was detected during the processing of that message.

LOOK-UP TABLES

In RTU mode a Look-Up Table is provided to allow the CT2566 to store messages in distinct areas of RAM based upon the subaddress of the received command word. See RTU operation for details.

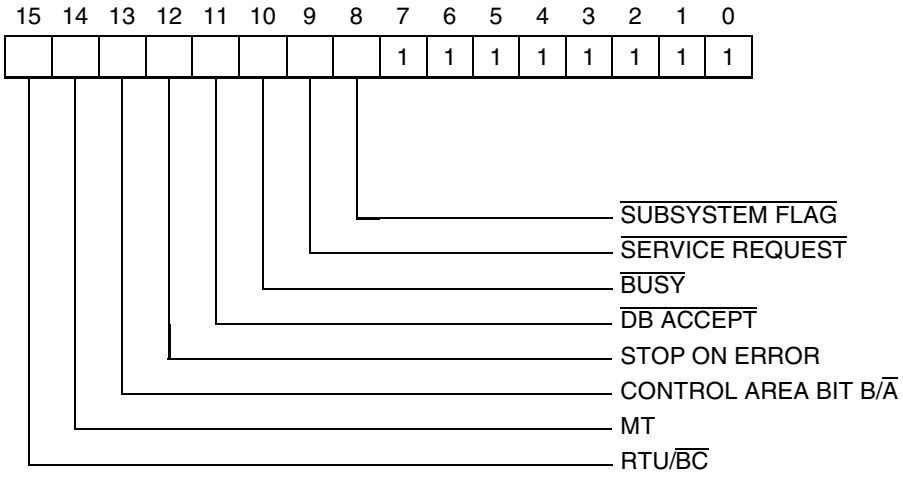
The CT2566 uses the T/$\overline{R}$ and the five subaddress bits to form a pointer into the "current area" Look-Up Table. The first 32 words of this table are initialized by the user with the addresses of the data blocks to be used for receiving data into subaddress 0,1,2,…31. The next 32 words are initialized by the user with the address of the data blocks to be used when transmitting data from subaddress 0,1,2,…31.

CT2566 REGISTERS

The CT2566 is controlled through the use of three internal registers: the Interrupt Mask Register, Configuration Register, and Start/Reset Register. In addition, the CT2566 can access up to four external, user supplied registers. Possible external register applications include: defining the RTU address, storing a CPU Time Tag, and reading a captured Built-In-Test (BIT) Word from the 1553 interface unit. For further information, consult factory.

Table 2 – Internal Registers Address Definition

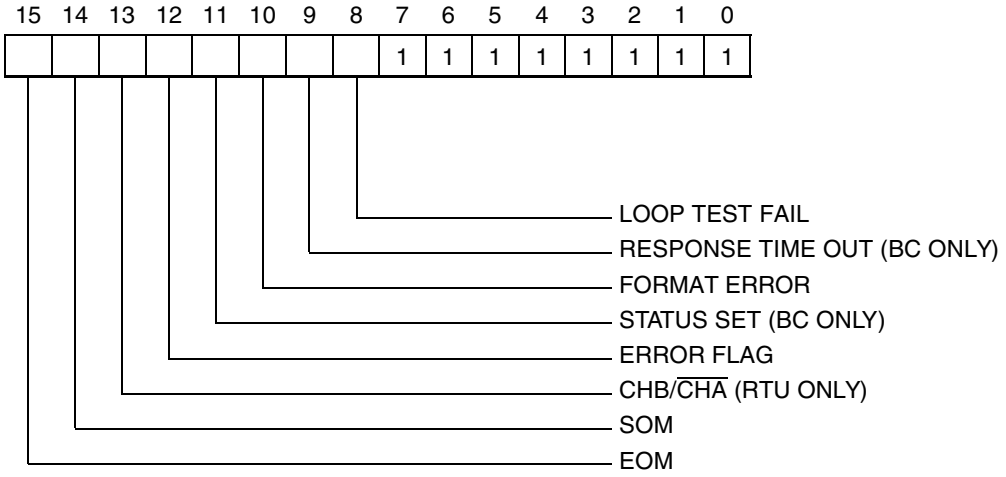
CT2566 Address Bits A2	A1	A0	Definition
0	0	0	Interrupt Mask Register
0	0	1	Configuration Register
0	1	0	Not Used
0	1	1	Start/Reset Register (write only)
1	0	0	External Register
1	0	1	External Register
1	1	0	External Register
1	1	1	External Register



BIT	DEFINITIONS
$\overline{\text{SUBSYSTEM FLAG}}$	1553 status word bit.
$\overline{\text{SERVICE REQUEST}}$	1553 status word bit.
$\overline{\text{BUSY}}$	1553 status word bit.
$\overline{\text{DB ACCEPT}}$	1553 status word bit.
STOP ON ERROR	Causes BC to stop at the end of current data block if an error is detected.
CONTROL AREA B/$\overline{A}$	Used for double buffering (See Double Buffering).
RTU/$\overline{BC}$/MT	Operating Mode.

Bit 15	Bit 14	Mode
0	0	BC
0	1	MT
1	0	RTU
1	1	ILLEGAL

Figure 8 – Configuration Register



Note: In BC mode Bit 13, CHB/$\overline{\text{CHA}}$ contains a logic "0" regardless of which channel is used.

Figure 5 – Block Status Word

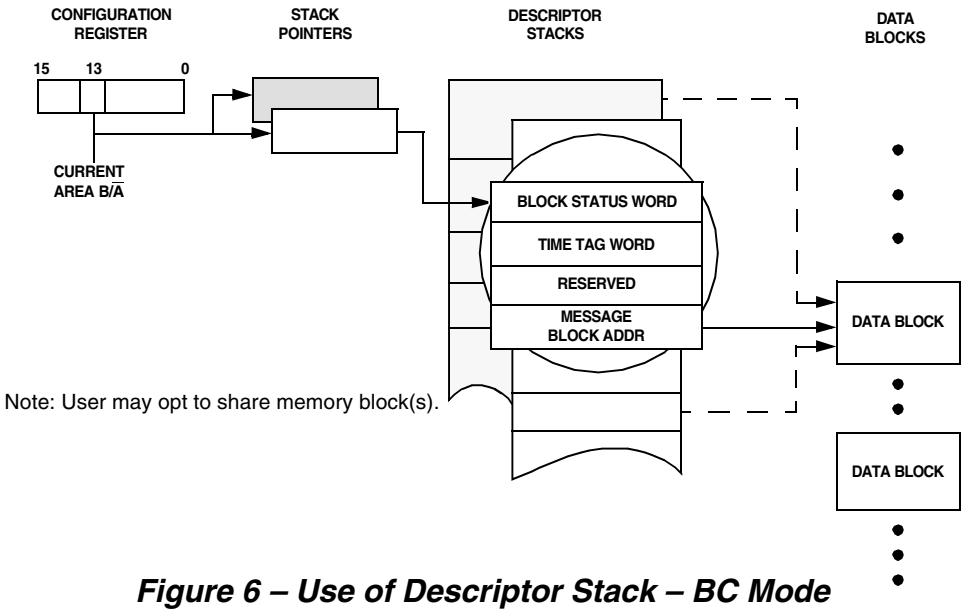


Figure 6 – Use of Descriptor Stack – BC Mode

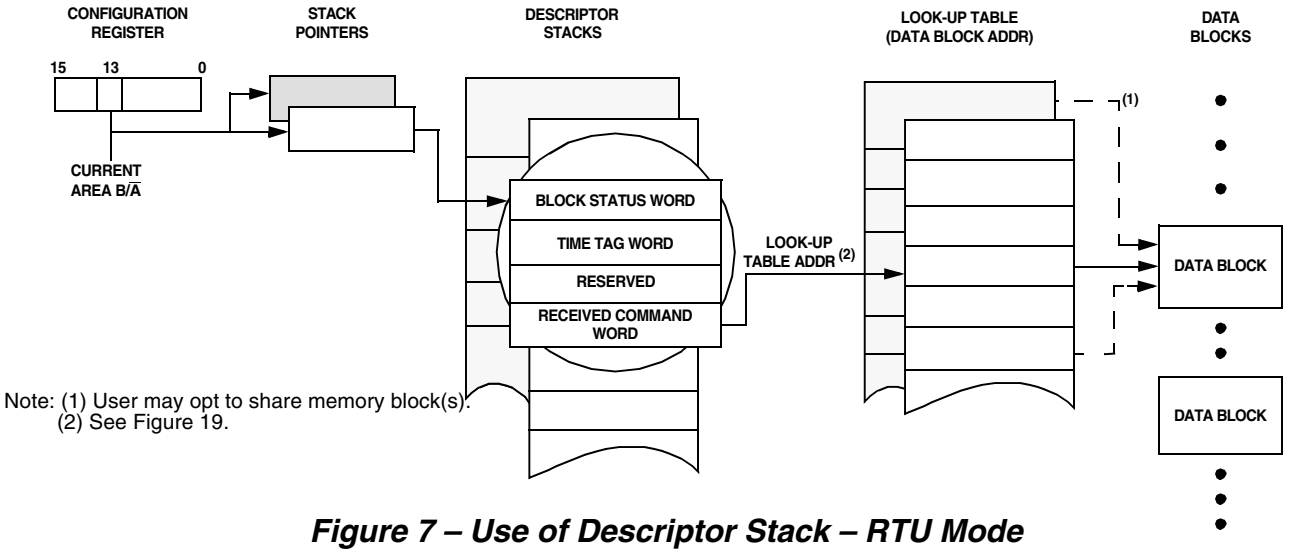
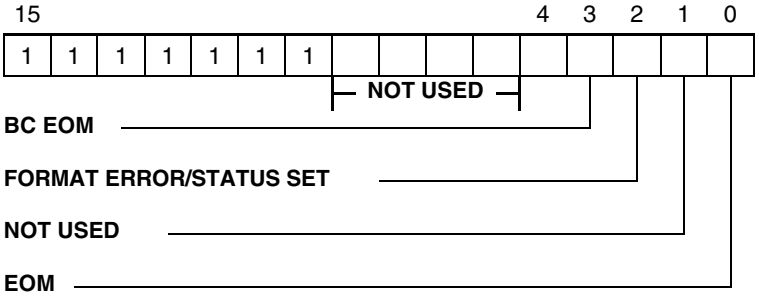


Figure 7 – Use of Descriptor Stack – RTU Mode

INTERRUPT MASK REGISTER

This register is an eight bit read/write register used to enable the interrupt conditions. All interrupts are enabled with a logic "1" (See Figure 9).

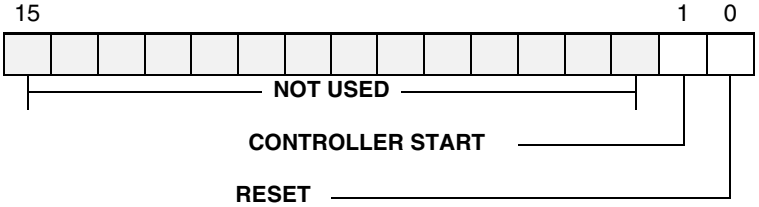


INTERRUPT	DEFINITION
EOM	End of Message. Set by CT2566 (during BC or RTU mode) every time a 1553 message is transferred (regardless of validity).
FORMAT ERROR/ STATUS SET	Set by CT2566 for these conditions: **Loop Test Failure:** Last transmitted word did not match received word. **Message Error:** Received message contained an address error, one of eight 1553 status bits set, or 1553 specification violated (parity error, Manchester error, etc). **Time-Out:** Expected transmission was not received during allotted time **Status Set:** Received status word contained status bit(s) set or address error.
BC EOM	Bus Controller End of Message. Set by CT2566 (in BC mode) when all messages have been transferred.

Figure 9 – Interrupt Mask Register

START/RESET REGISTER

Only two bits of this write only register are used, as illustrated in Figure 10.



BIT	DEFINITION
RESET	Issued by the CPU to place the CT2566 in the power-on condition; Configuration, and Interrupt Mask registers are reset to logic “0”.
CONTROLLER START	Issued by the CPU (BC mode) to start message transmission. The CPU must first load the number of messages to transfer (256, max) in the message count location of RAM (area A or B). Value is loaded in 1’s complement (load FFFE to transmit one message). In MT mode it is used to begin reception of 1553 messages. Issued by CPU in MT mode to enable monitor operation.

Figure 10 – Start/Reset Register

BC Operation

The BC mode is selected by setting the two MSBs of the Configuration Register to logic "0". This can be done by writing directly to the register or by issuing a MSTRCLR or RESET command. Note that a RESET will also clear the Interrupt Mask Register.

BC Initialization.

For BC operation, the user initializes the RAM as shown in Table 3 and follows the steps in Figure 11, BC Initialization. The CPU loads the data blocks with 1553 messages (See Figure 12). The first word of each data block must contain the Control Word (shown in Figure 13) for the message. The starting addresses of the data blocks are placed in the fourth word of the Descriptor Stack in the order the messages are to be transmitted (i.e. the address of the first message is loaded into the fourth location of the Stack, the address of the second message is placed into the eighth location, etc). Once the data blocks and the Descriptor Stack have been initialized, the CPU loads the current area message count with the number of messages to transfer (load in 1's complement).

Table 3 - Typical BC Memory Map (4K memory)]

HEX ADDRESS	FUNCTION
Fixed Areas	
0100	Stack Pointer A
0101	Message Count A
0104	Stack Pointer B
0105	Message Count B
User Defined Areas	
0108-013F	Not Used
0140-017F	Data Block 1
0180-01BF	Data Block 2
01C0-01FF	Data Block 3
•	•
•	•
0F00-0FFF	Descriptor Stack A
0000-00FF	Descriptor Stack B

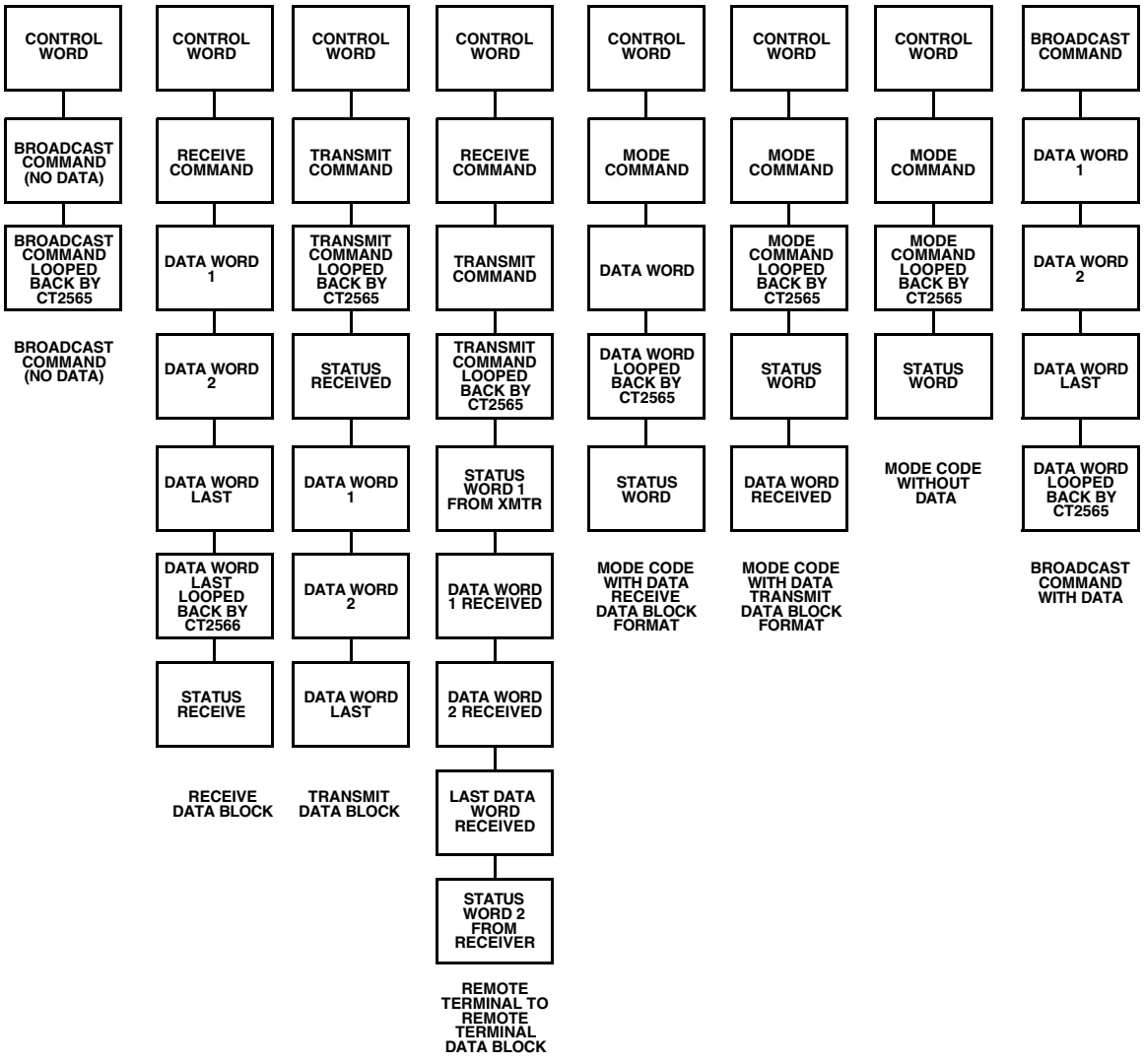


Figure 12 – BC Message Data Block Formats

The CPU selects an internal register by asserting MEM/$\overline{REG}$ and the A2 bit to logic "0" (See Table 2). External registers are selected by asserting MEM/$\overline{REG}$ logic "0" and A2 bit to a logic "1". The signals $\overline{EXTEN}$ and $\overline{EXTLD}$ are used to read and write from the external registers (See Figures 26 to 28).

Configuration Register

The Configuration Register is an eight bit read/write register used to define the 1553 operating mode (BC, MT, or RTU) and the associated RTU status bits. The four MSBs define the mode of operation; the four LSBs define the RTU status bits (See Figure 8).

All bits in the Configuration Register (except bit 12) will be present on the respective CT2566 output pins to the 1553 device. The MT bit is inverted at the output.

To begin transferring messages onto the bus, the CPU must issue a Controller Start Command (See Figure 14). This is done by setting bit 1 of the Start/Reset Register to a logic "1". An EOM interrupt will be generated each time a message transfer has been completed. A BCEOM will be generated once the specified number of messages has been transferred (message counter = FFFF).

A Format Error Status Set Interrupt will be generated at the end of a message if a timeout condition or error condition was detected. If the STOP ON ERROR bit in the Configuration Register is set, the CT2566 will stop bus transactions until a new Controller Start command is issued by the CPU. These interrupts may be masked by the CPU through the Interrupt Mask Register.

BC START SEQUENCE

After setting the CONTROLLER START bit in the Start/Reset Register, the CT2566 takes the following actions:

1. Reads the Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Stores an SOM flag in the Block Status Word to indicate a transfer operation is in progress.
3. Stores the Time Tag if used.
4. Reads the Data Block Address from the fourth location of the Descriptor Stack and transfers the Data Block Address into an internal Address Register.
5. Issues a BCSTART pulse to the associated 1553 device to start the message transfers.

Note that data words are transferred to an from memory by the associated 1553 interface unit using the internal Address Register.

BC EOM Sequence.

Upon completion of a 1553 message (valid or invalid) the 1553 interface unit issues an EOM pulse to the CT2566 which takes the following actions:

1. Reads the Stack Pointer to get the address of the current Descriptor Stack Entry.

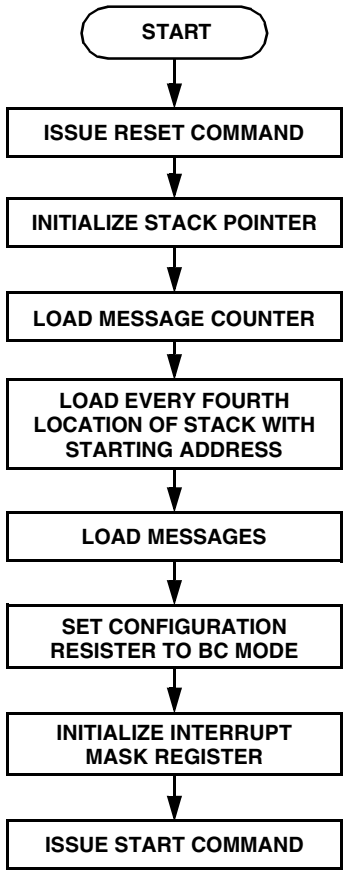
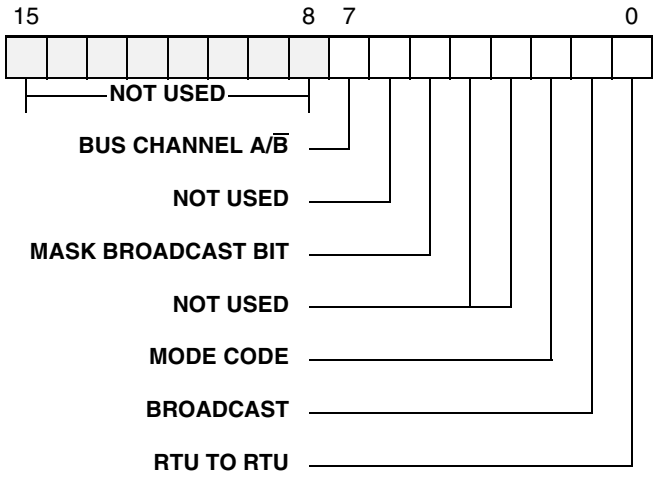
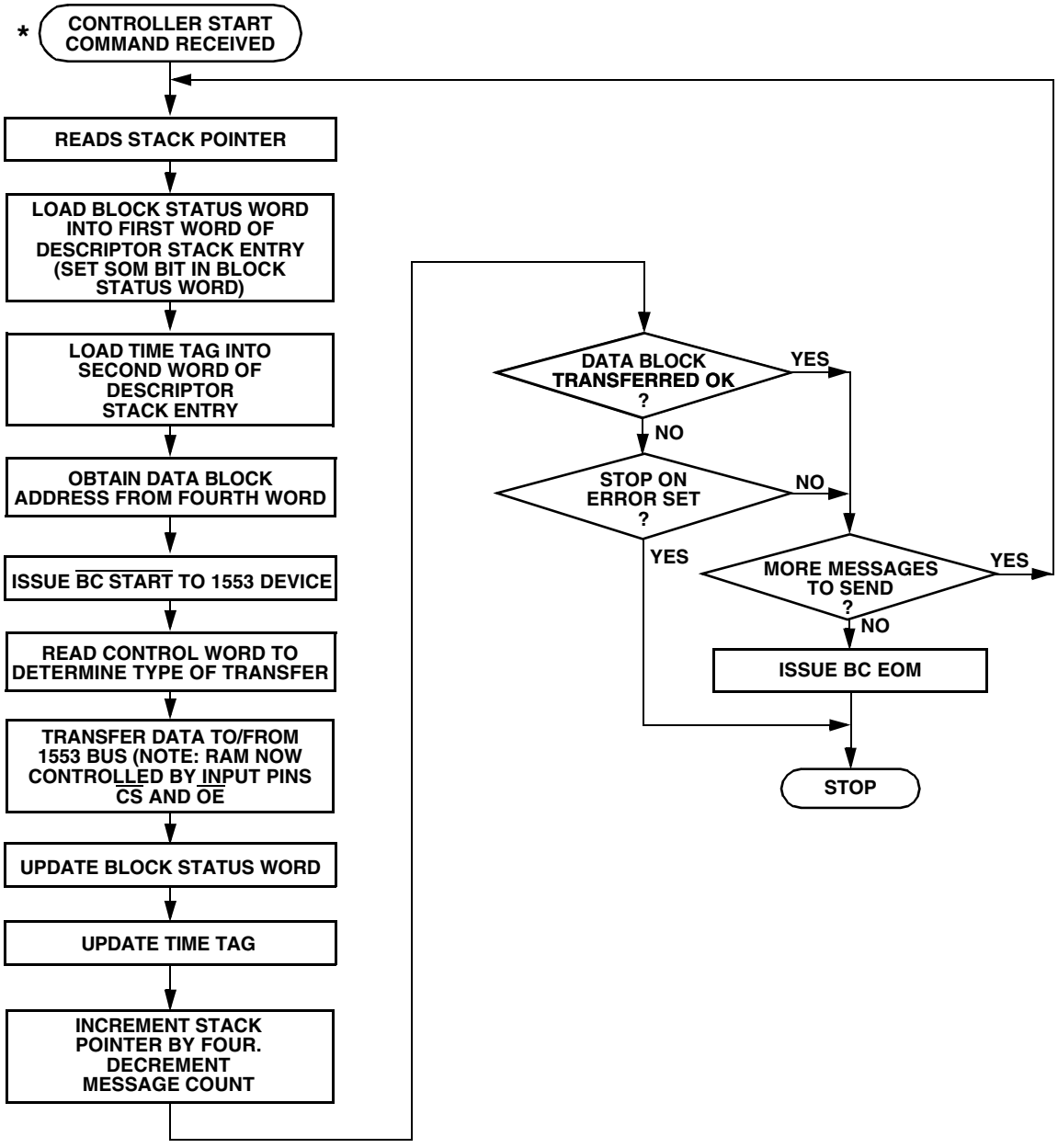


Figure 11
BC Initialization (under user control)



Note: When the BC expects the BROADCAST bit set in the status word, a logic "1" will mask the status interrupt error flag. A FORMAT error will be generated if the MASK BROADCAST bit is not set.

Figure 13 – BC Control Word



***** **After controller start is issued the subsystem must wait until BCEOM is active before issuing the next controller start.**

Figure 14 – BC Sequence of Operation (Under CT2566 Control)

2. Updates the Block Status Word by resetting the SOM and setting EOM and any error bits.
3. Updates the Time Tag if used.
4. Increments the contents of the Stack Pointer by four and increments the Message Counter by one.
5. Initiates a message transfer beginning with new Controller Start sequence if more messages are to be transmitted.
6. Generates a BCEOM interrupt if enabled and no further messages are to be transmitted.

Note that if an error is received and STOP ON ERROR is set, the CT2566 completes the current BCEOM sequence and then stops. The Stack Pointer will point to the next message to be transmitted.

RTU Operation

The RTU mode is selected by setting bit 15 of the Configuration Register to logic "1" and bit 14 to logic "0".

RTU Initialization

For RTU operation, the user initializes the RAM as shown in Table 4 and follows the steps shown in Figure 15, RTU Initialization Chart.

Look-Up Tables

The first 32 words of the Look-Up Table are initialized with the addresses of the data blocks to be used when received data from subaddress 0, 1, 2,…31. The next 32 table locations should be initialized with the address of the data blocks to be used when the RTU is instructed to transmit data from subaddress 0, 1, 2,…31. The data blocks may be any length sufficient to contain the particular message as long as the data block does not cross a 256 word boundary. Data blocks may be shared by Look-Up Tables A and B, if desired by the user (See Figure 16). The 1553 device can only access the current Look-Up Table and the current Descriptor Stack. The CPU selects the current area through bit 13 of the Configuration Register.

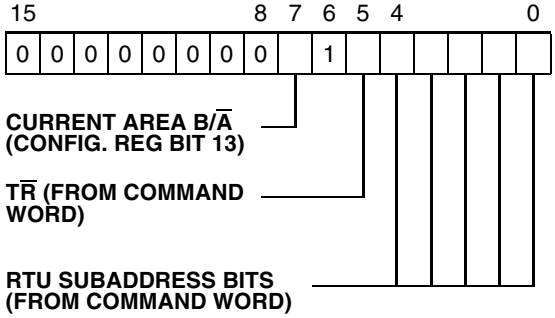
Once in the RTU mode, the CT2566 will store the command word in the fourth location of the current area Descriptor Stack. The status of the message will be recorded in the first location of the stack.

The data associated with the message will be transferred to/from the data block indicated by the Look-Up Table entry for that subaddress. If a system Time Tag is provided by the user the CT2566 will record the time of the SOM sequence in the second word of the Stack entry.

When the CT2566 received an EOM pulse from the 1553 device, it resets the SOM bit in the Block Status Word and sets the EOM bit and any error bits as necessary. The Time Tag entry will be updated and an EOM interrupt will be generated by the CPU, if enabled.

Table 4 – Typical RTU memory map (4K memory)

HEX ADDRESS	FUNCTION
Fixed Areas	
0100	Descriptor Stack Pointer A
0101	Reserved
0104	Descriptor Stack Pointer B
0105	Reserved
0108-013F	Spare
0140-017F	Look-Up Table A
01C0-01FF	Look-Up Table B
User Defined Areas	
0180-019F	Data Block 1
01A0-01BF	Data Block 2
0200-021F	Data Block 3
0220-023F	Data Block 4
0240-025F	Data Block 5
0260-027F	Data Block 6
•	•
•	•
0EE0-0EFF	Data Block 107
0000-00FF	Descriptor Stack A
0F00-0FFF	Descriptor Stack B



RTU LOOK-UP TABLE ADDRESS

RTU SOM Sequence

Initiated when 1553 terminal puts a 1553 command word on D00-D15 and pulses $\overline{SOM}$ low. The CT2566 saves the command received in an internal register. Figure 17 illustrates the RTU Sequence of Operation once a 1553 command word is received. Once the command word is received, the CT2566 performs the following steps:

1. Reads the Stack Pointer to get the address of the current Descriptor Stack Entry.
2. Stores a SOM flag in the Block Status Word to indicate a transfer operation is in progress.
3. Stores the Time Tag if used.

4. Stores the Command Word received.
5. Reads a Block address from the Look-Up Table using the T/R bit and the subaddress from the Command Word; transfers the Block address into the address register. Data words are transferred to/from memory by the associated 1553 interface unit using the address register.

RTU EOM Sequence

At the end of a 1553 message (valid or invalid) the CT2566 received an EOM pulse and then performs the following:

1. Updates the Block Status Word.
2. Updates the Time Stage if used.
3. Increments the Stack Pointer by four.
4. Generates an Error Interrupt if enabled.

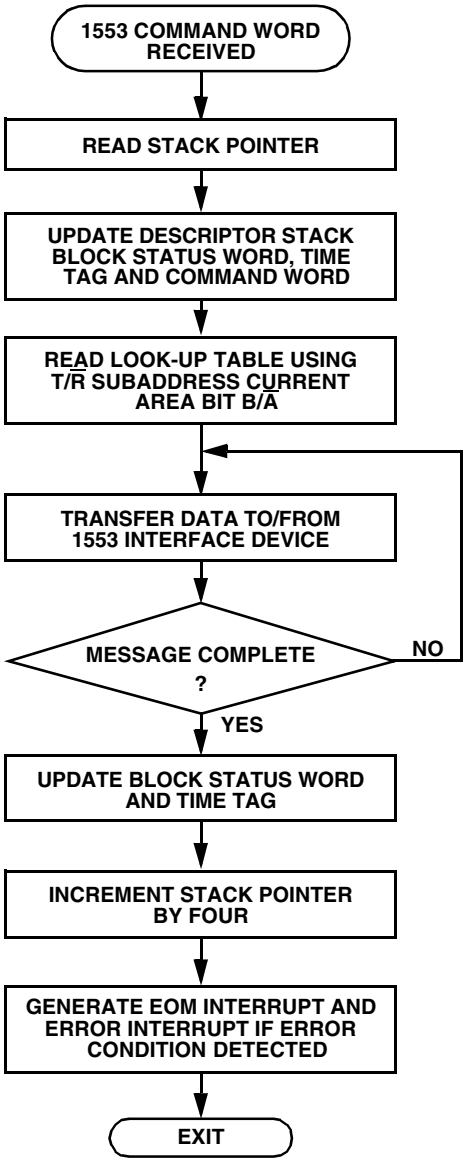


Figure 17 – RTU Sequence of Operation (under CT2566 control)

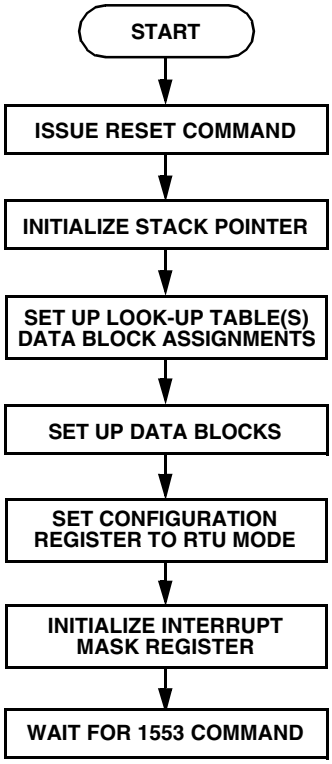


Figure 15 RTU Initialization (under user control)

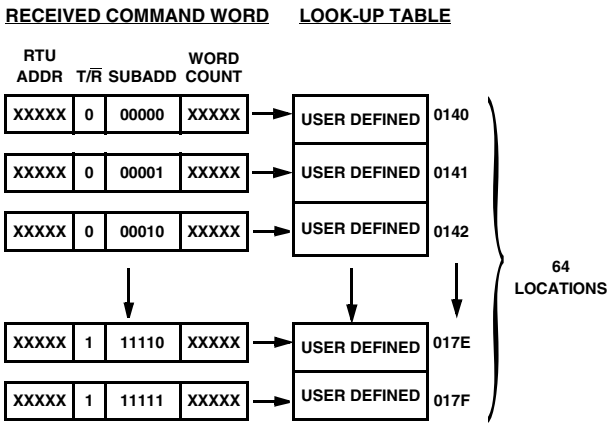


Figure 16 – RTU Look-up Table

MT Operation

The MT mode is selected by setting bit 15 of the Configuration Register to logic "0" and bit 14 to a logic "1" along with issuing a Controller Start Command.

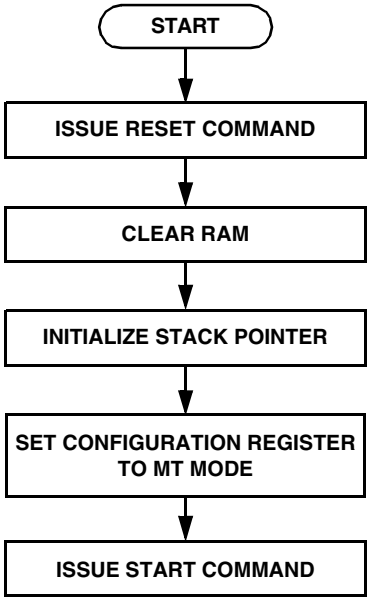


Figure 18 – MT Initialize (under user control)

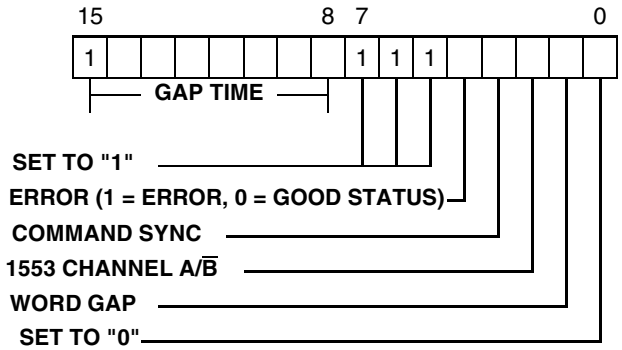
MT Initialization

For MT operations, the entire RAM is used as the MT Stack (See Table 5) and the setups shown in Figure 18 are followed. The user instructs the CT2566 where to store the first received 1553 word by loading the starting word address in the Stack Pointer. Once a Controller Start command is issued, the CT2566 will store this value in the internal Address Register.

The identification Word provides the CPU with additional information regarding the received 1553 word, its format is shown in Figure 19. This information allows the user to develop algorithms to restructure the message transfers. External Logic can be used for triggering on specific commands or subaddresses. For further information, consult factory.

The 1553 device will generate an Identification Word for every word that is transferred across the 1553 Data Bus. The CT2566 stores the received 1553 word in the RAM location indicated by the internal Address Register. The contents of this register are incremented by one so that it points to the next word in RAM, and the Identification Word is stored at that location. The internal Address Register is then incremented by one again, in preparation for storing the next Identification Word. The RAM automatically wraps around (from location FFFF to location 0000), shown in Figure 20.

Bit 7 of the Identification Word can be reset by the CPU each time it reads the associated data word into CPU memory. This provides a simple method of keeping track of words that have been processed by the CPU.



Note: Each bit of the GAP TIME field represents .5µs.

Figure 19 – MT Identification Word

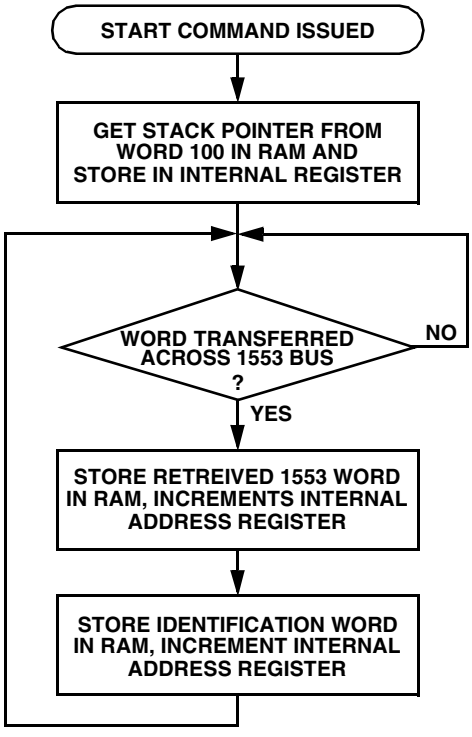


Figure 20 – MT Sequence of Operation (under CT2566 control)

Table 5 – Typical MT memory map (4K memory)

HEX ADDRESS	FUNCTION
0000	First Received 1553 Word
0001	First Identification Word
0002	Second Received 1553 Word
0003	Second Identification Word
0004	•
0005	•
0006	•
0007	•
0008	•
•	•
•	•
0100	Stack Pointer A (Fixed location)*
0104	Stack Pointer B
•	•
•	•
FFFF	Word stored at FFFF will be followed by the word stored at 0000.

* The Stack Pointer is loaded into an internal Address Register upon receipt of a Controller Start command. This location is overwritten by data once monitor operation begins.

MODE CODES

All mode codes applicable to dual redundant systems are recognized by the CT2566. Mode codes can be illegalized by the 1553 BC or RTU device. Refer to the CT2565 or CT2512 data sheets for more information.

CT2566 Timing Clock in at 12 MHz

Figures 21 through 37 illustrate the timing for the CT2566 and its operation. All timing definitions are listed in the tables below and the appropriate definitions are repeated with each diagram.

Delay Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	$\overline{\text{READYD}}$ low delay (CPU Handshake)	-	200	ns
td2	$\overline{\text{IOEN}}$ high delay (CPU Handshake)	-	20	ns
td3	CPU $\overline{\text{MEMWR}}$ low delay	-	120	ns
td4	CPU $\overline{\text{MEMOE}}$ low delay	-	115	ns
td5	$\overline{\text{EXTLD}}$ low delay	-	130	ns
td6	$\overline{\text{RESET}}$ low delay	-	30	ns
td7	Internal Register delay (read)	-	60	ns
td8	Internal Register delay (write)	-	60	ns
td9	Register Data/Address set-up time	-	40	ns
td10	Register Data/Address hold time	-	0	ns

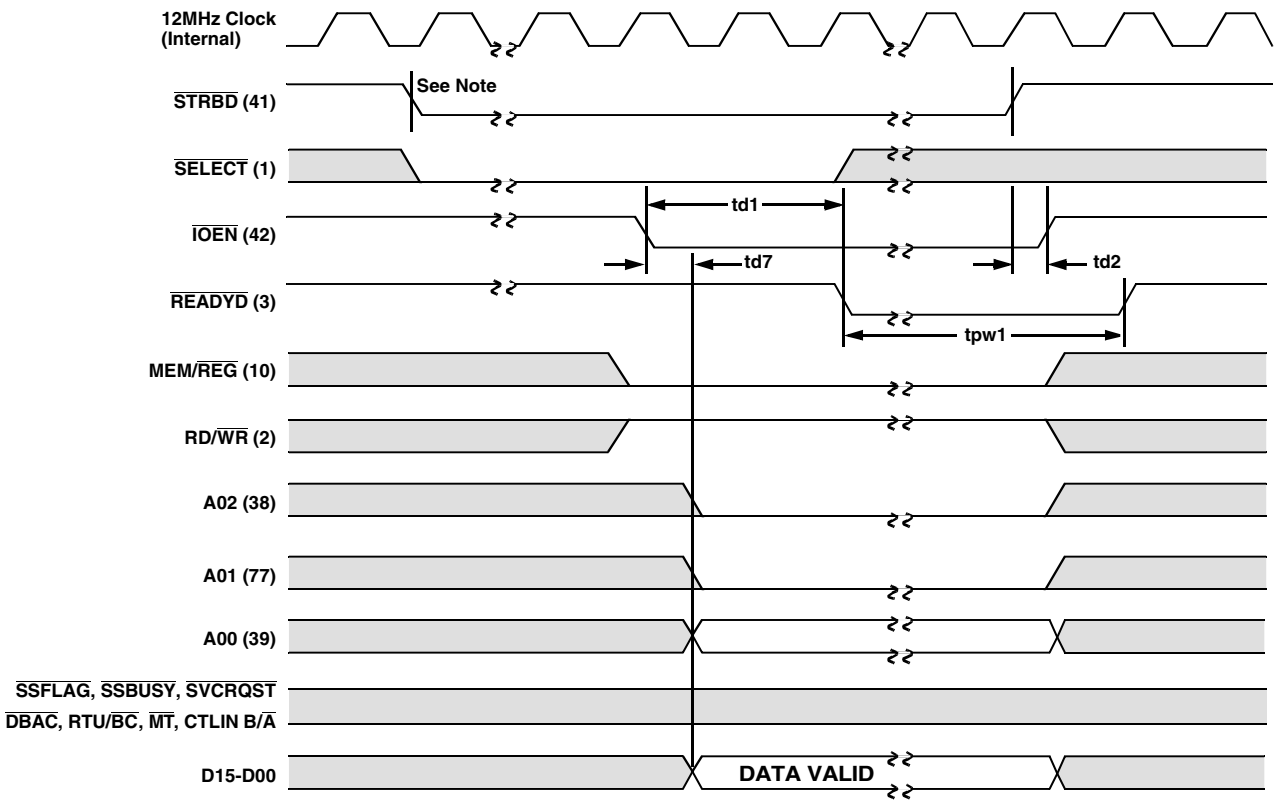
Delay Timing (Cont.)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td11	BC SOM Cycle DMA delay	-	120	ns
td12	$\overline{INT}$ low delay	-	50	ns
td13	RTU SOM Cycle DMA delay	-	200	ns
td14	1553 Command Word set-up time	60	-	ns
td15	1553 Command Word hold time	60	-	ns
td16	MT SOM Cycle DMA delay	-	120	ns
td17	$\overline{CS}$ low to $\overline{MEMCS}$ low delay	-	30	ns
td18	$\overline{OE}$ low to $\overline{MEMOE}$ low delay	-	30	ns
td19	$\overline{WR}$ low to $\overline{MEMWR}$ low delay	-	30	ns
td20	$\overline{BUSGRNT}$ high delay	-	25	ns
td21	$\overline{BUSACK}$ low Address delay	-	45	ns
td22	$\overline{BUSACK}$ high Address delay	-	25	ns
td23	Address increment delay	-	200	ns

Pulse Width Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
tpw1	$\overline{READYD}$ pulse width (CPU Handshake)	70	-	ns
tpw2	CPU $\overline{MEMWR}$ low pulse width	70	-	ns
tpw3	CPU $\overline{MEMCS}$ low pulse width	70	-	ns
tpw4	$\overline{EXTLD}$ low pulse width	70	-	ns
tpw5	$\overline{RESET}$ low pulse width	70	-	ns
tpw6	DMA $\overline{MEMWR}$ low pulse width	70	-	ns
tpw7	DMA $\overline{MEMCS}$ low pulse width	70	-	ns
tpw8	$\overline{BCSTART}$ low pulse width	70	-	ns
tpw9	$\overline{EOM}$ low pulse width	50	200	ns
tpw10	$\overline{INT}$ low pulse width	*	tpw9	ns
tpw11	$\overline{INT}$ low (BCEOM) pulse width	60	-	ns
tpw12	$\overline{SOM}$ low pulse width	50	200	ns
tpw13	$\overline{NBGRNT}$ low pulse width	50	200	ns
tpw14	$\overline{ADRINC}$ low pulse width	50	200	ns
tpw15	$\overline{MSTRCLR}$ low pulse width	150	-	ns

*The min value of tpw10 equals tpw9 minus 30 ns.

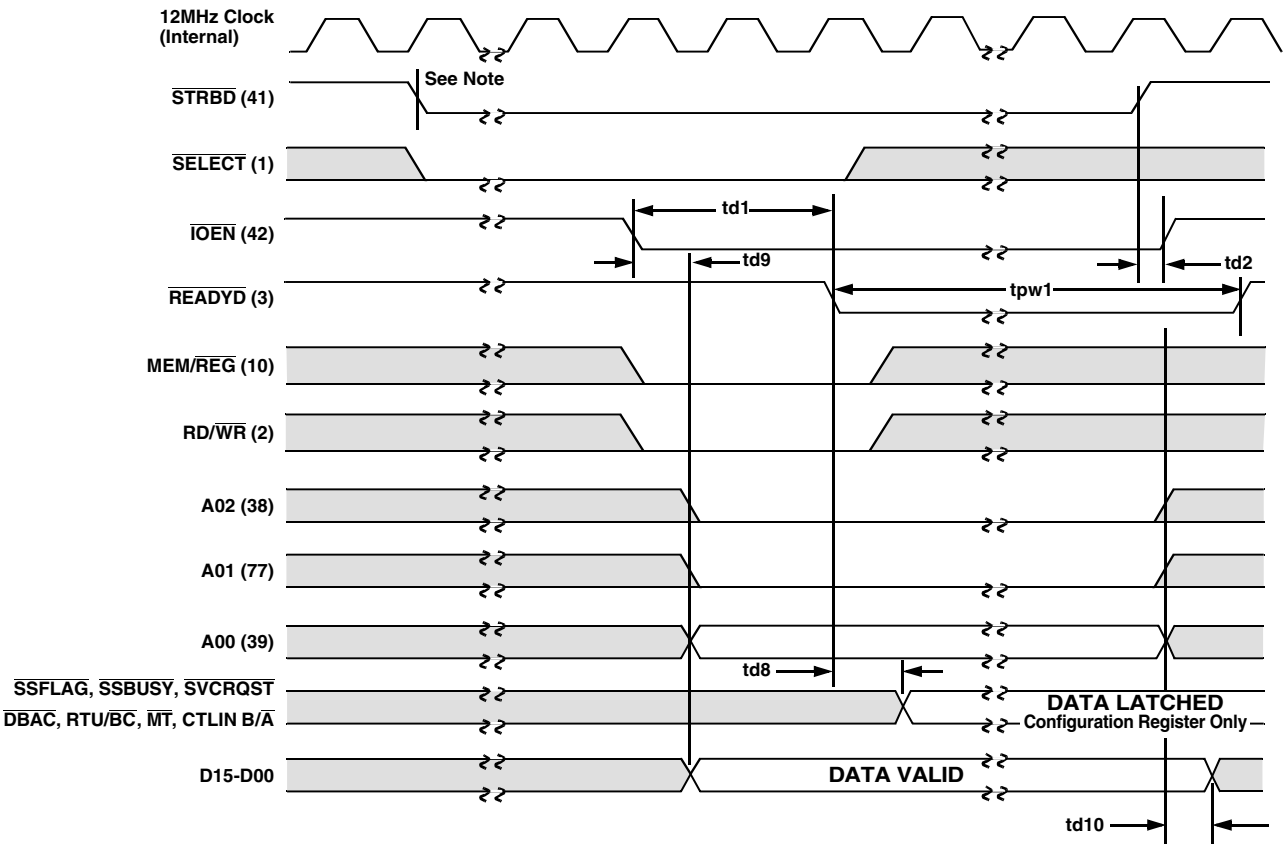


NOTE: STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus.

CPU Reads from Internal Register

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	READYD low delay (CPU Handshake)	-	200	ns
td2	IOEN high delay (CPU Handshake)	-	20	ns
tpw1	READYD pulse width (CPU Handshake)	70	-	ns
td7	Internal Register delay (read)	-	60	ns

Figure 21 – CPU reads from internal register

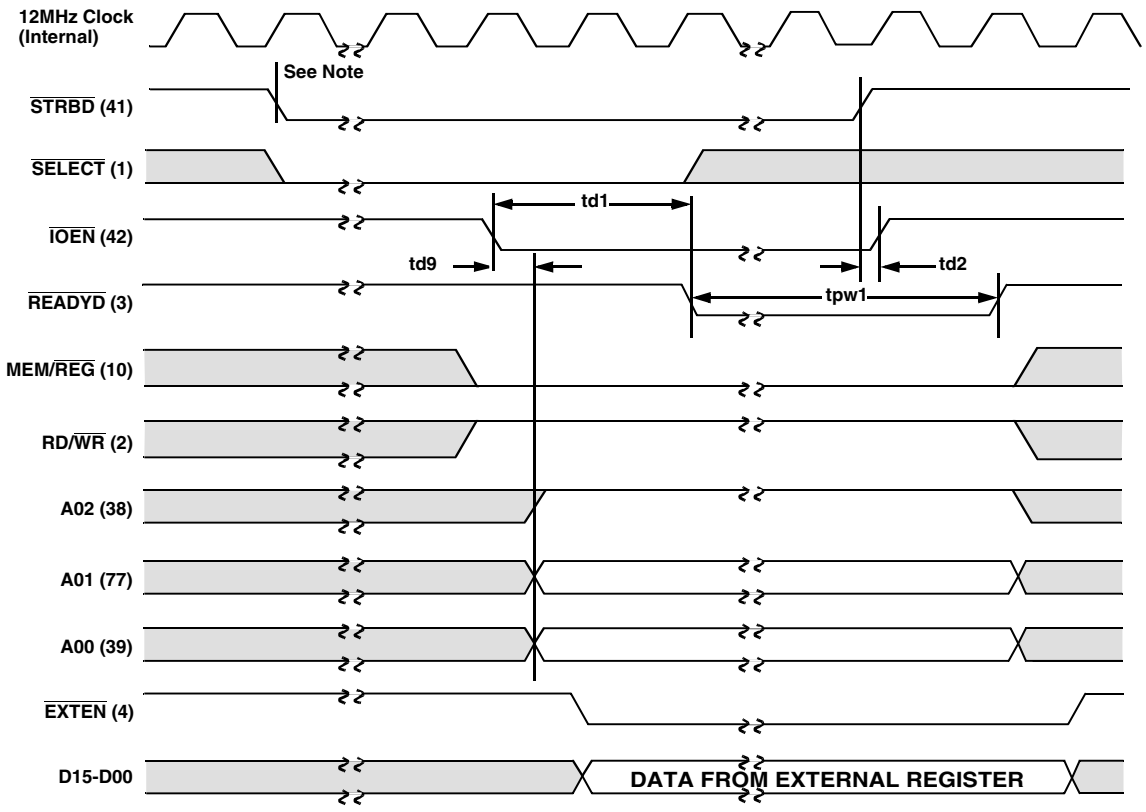


NOTE: STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus.

CPU Writes to Internal Register

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	READYD low delay (CPU Handshake)	-	200	ns
td2	IOEN high delay (CPU Handshake)	-	20	ns
tpw1	READYD pulse width (CPU Handshake)	70	-	ns
td8	Internal Register delay (write)	-	60	ns
td9	Register Data/Address set-up time	-	40	ns
td10	Register Data/Address hold time	-	0	ns

Figure 22 – CPU writes to internal register

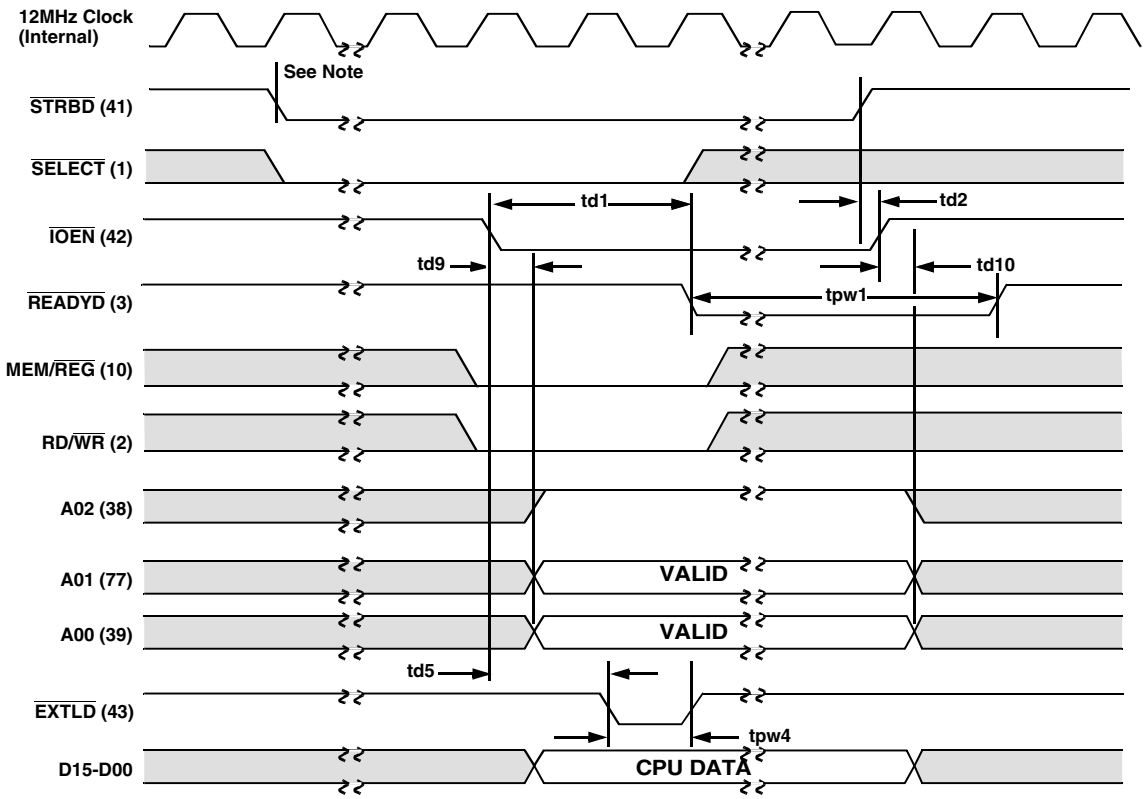


NOTE: STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus.

CPU Reads from External Register Timing

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	READYD low delay (CPU Handshake)	-	200	ns
td2	IOEN high delay (CPU Handshake)	-	20	ns
tpw1	READYD pulse width (CPU Handshake)	70	-	ns
td9	Register Data/Address set-up time	-	40	ns

Figure 23 – CPU reads from external register

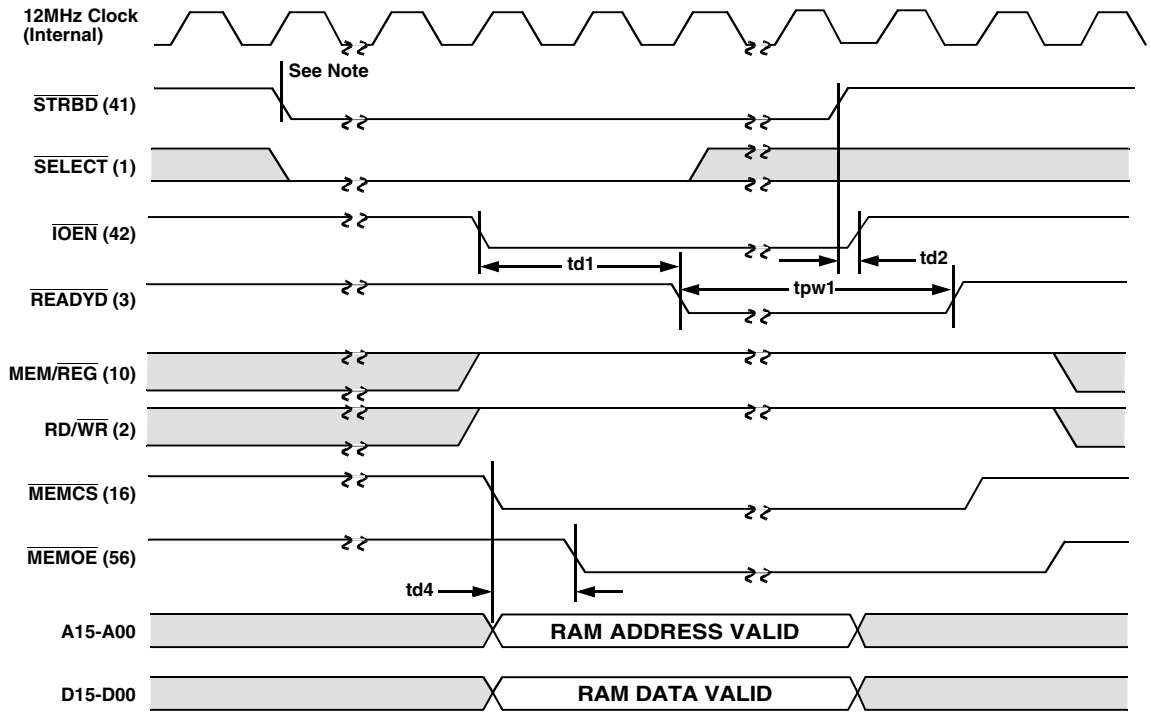


NOTE: STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus.

CPU Writes to External Register

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	READYD low delay (CPU Handshake)	-	200	ns
td2	IOEN high delay (CPU Handshake)	-	20	ns
tpw1	READYD pulse width (CPU Handshake)	70	-	ns
td5	EXTLD low delay	-	130	ns
td9	Register Data/Address set-up time	-	40	ns
td10	Register Data/Address set-up time	-	0	ns
tpw4	EXTLD low pulse width	70	-	ns

Figure 24 – CPU writes to external register

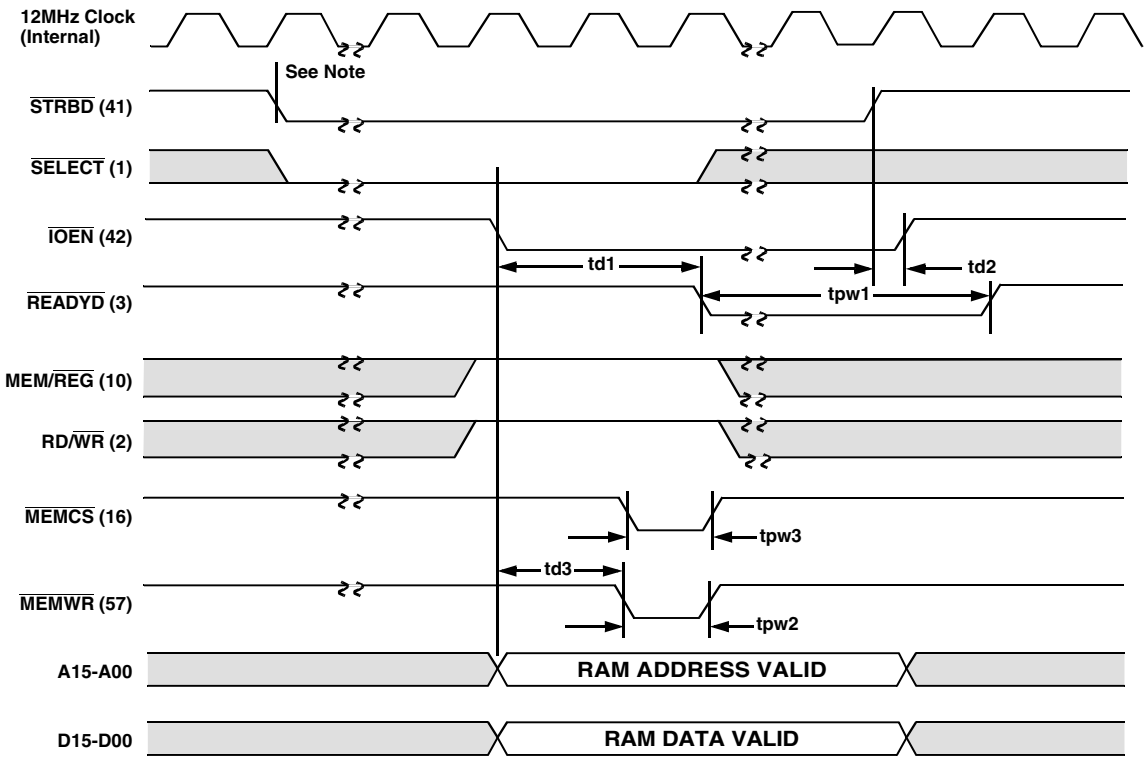


NOTE: STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus.

CPU Reads from Ram

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	READYD low delay (CPU Handshake)	-	200	ns
td2	IOEN high delay (CPU Handshake)	-	20	ns
tpw1	READYD pulse width (CPU Handshake)	70	-	ns
td9	CPU MEMOE low delay	-	115	ns

Figure 25 – CPU reads from RAM

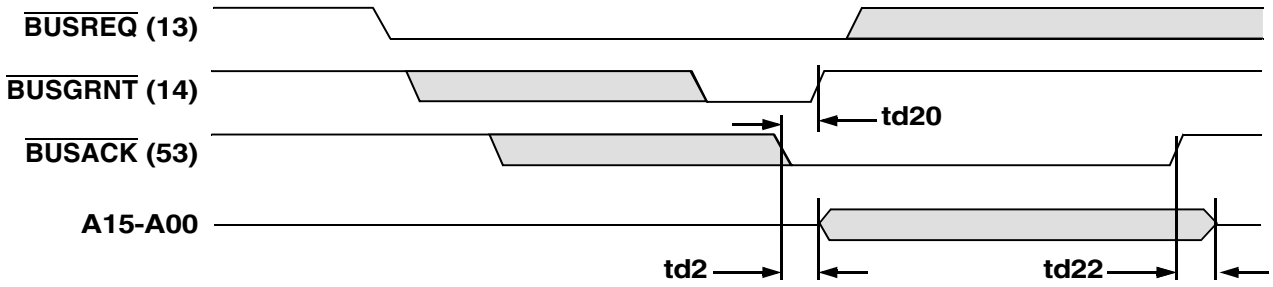


NOTE: STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus.

CPU Writes To Ram

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	READYD low delay (CPU Handshake)	-	200	ns
td2	IOEN high delay (CPU Handshake)	-	20	ns
tpw1	READYD pulse width (CPU Handshake)	70	-	ns
td3	CPU MEMWR low delay	-	120	ns
tpw2	CPU MEMWR low pulse width	70	-	ns
tpw3	CPU MEMCS low pulse width	70	-	ns

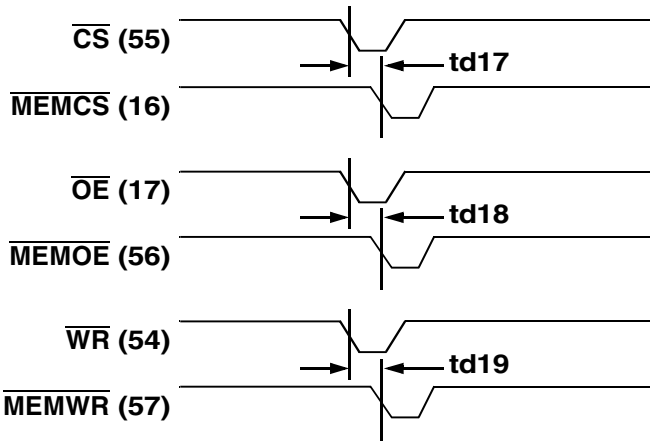
Figure 26 – CPU writes to RAM



MIL-STD-1553 TO CT2566 Handshaking

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td20	$\overline{\text{BUSGRNT}}$ high delay	-	25	ns
td21	$\overline{\text{BUSACK}}$ low Address delay	-	45	ns
td22	$\overline{\text{BUSACK}}$ high Address delay	-	25	ns

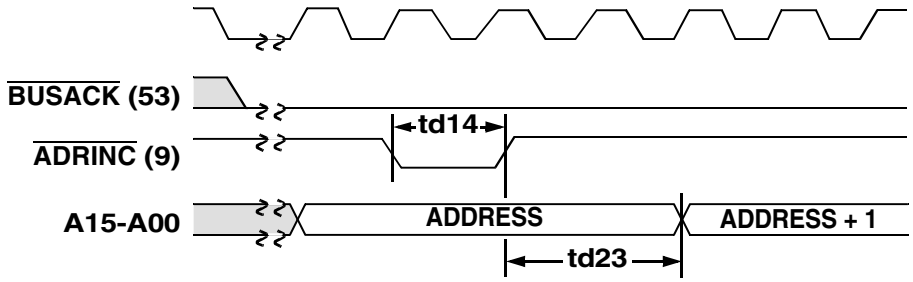
Figure 27 – MIL-STD-1553 to CT2566 Handshaking



MIL-STD-1553 Terminal to Delay

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td17	$\overline{\text{CS}}$ low to $\overline{\text{MEMCS}}$ low delay	-	30	ns
td18	$\overline{\text{OE}}$ low to $\overline{\text{MEMOE}}$ low delay	-	30	ns
td19	$\overline{\text{WR}}$ low to $\overline{\text{MEMWR}}$ low delay	-	30	ns

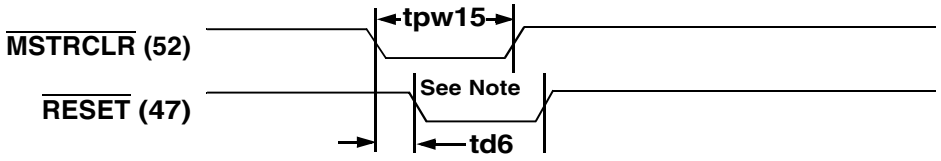
Figure 28 – MIL-STD-1553 terminal I/O delay



CT2566 Address Increment

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
tpw14	$\overline{\text{ADRINC}}$ low pulse width	50	200	ns
td23	Address increment delay	-	200	ns

Figure 29 – CT2566 Unit Address Increment

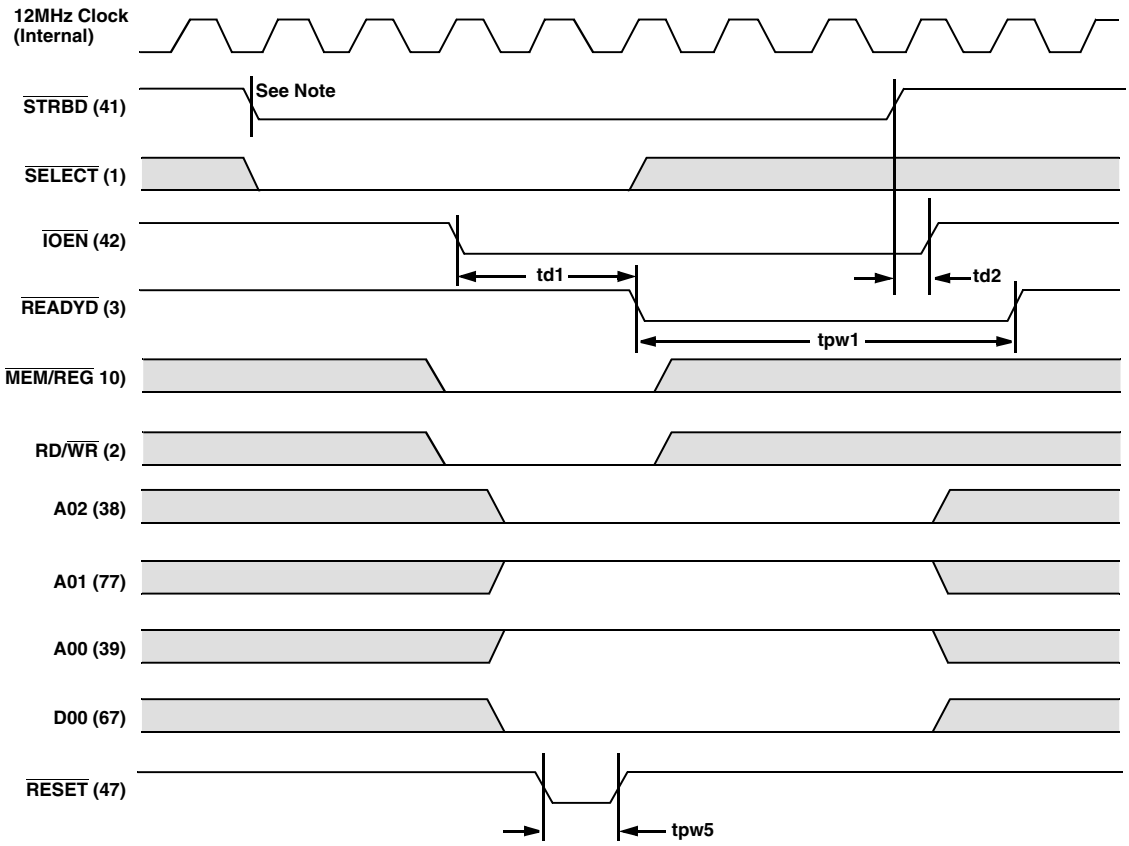


CT2566 Direct Increment

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td6	$\overline{\text{RESET}}$ low delay	-	30	ns
tpw15	$\overline{\text{MSTRCLR}}$ low pulse width	150	-	ns

NOTE: The $\overline{\text{RESET}}$ (low) pulse width will be approximately equal to that of $\overline{\text{MSTRCLR}}$ (low).

Figure 30 – CT2566 direct reset

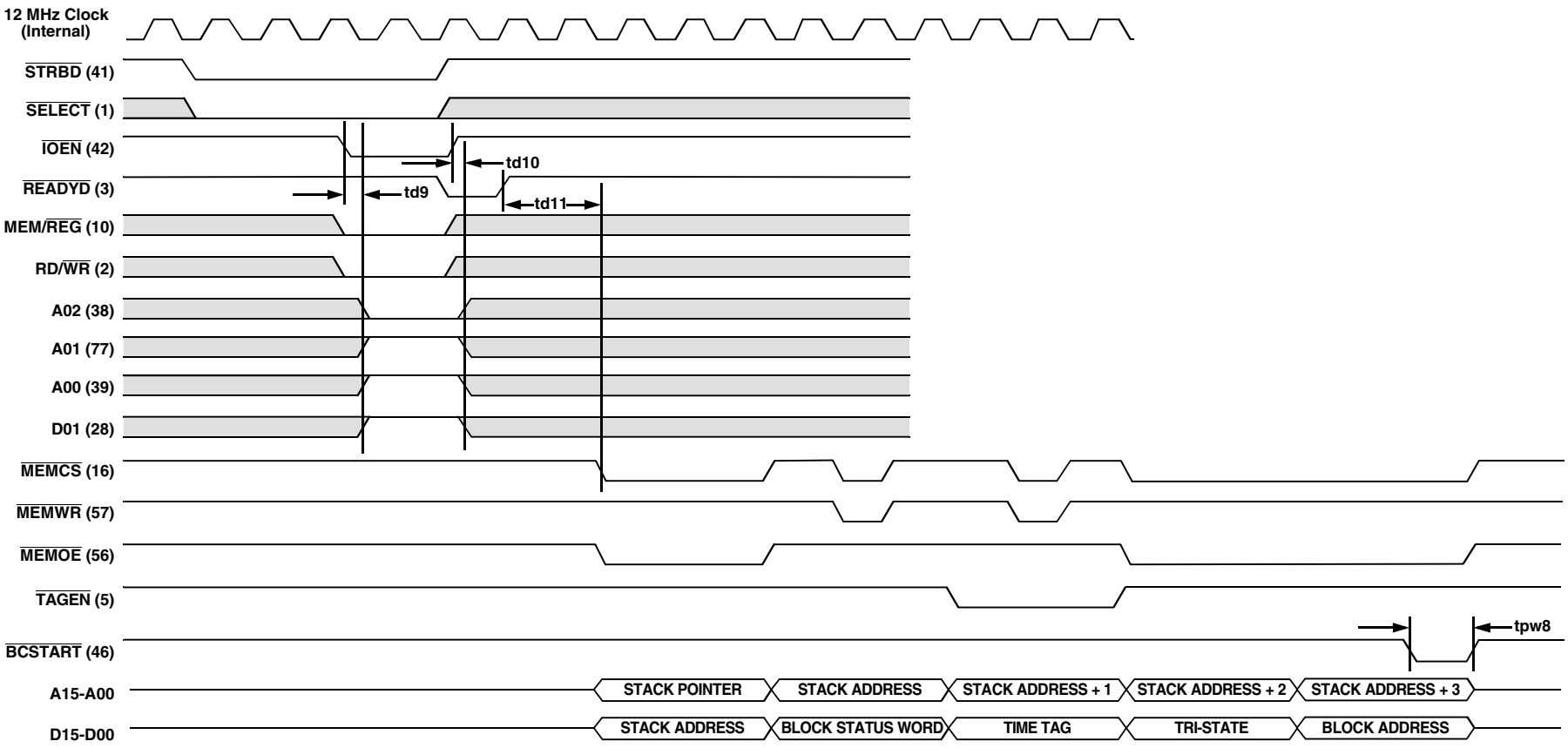


NOTE: STRBD to IOEN (low) delay is two clock cycles. If contention occurs, delay is two clock cycles following release of bus.

Programmed CT2566 Reset

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td1	READYD low delay (CPU Handshake)	-	200	ns
td2	IOEN high delay (CPU Handshake)	-	20	ns
tpw1	READYD pulse width (CPU Handshake)	70	-	ns
tpw5	RESET low pulse width	70	-	ns

Figure 31 – Programmed CT2566 reset



BC SOM Timing (No Contention)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td9	Register Data/Address set-up time	-	40	ns
td10	Register Data/Address hold time	-	0	ns
td11	BC SOM Cycle DMA delay	-	120	ns
tpw8	$\overline{\text{BCSTART}}$ low pulse width	70	-	ns

Figure 32 – BC SOM timing (no contention)

BC EOM Timing (No Contention)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td9	$\overline{INT}$ low delay	-	50	ns
tpw9	$\overline{INT}$ low pulse width	50	200	ns
tpw10	$\overline{INT}$ low pulse width	*	tpw9	ns
tpw11	$\overline{INT}$ low delay	60	-	ns
* The min value of tpw10 equals tpw9 minus 30ns.				

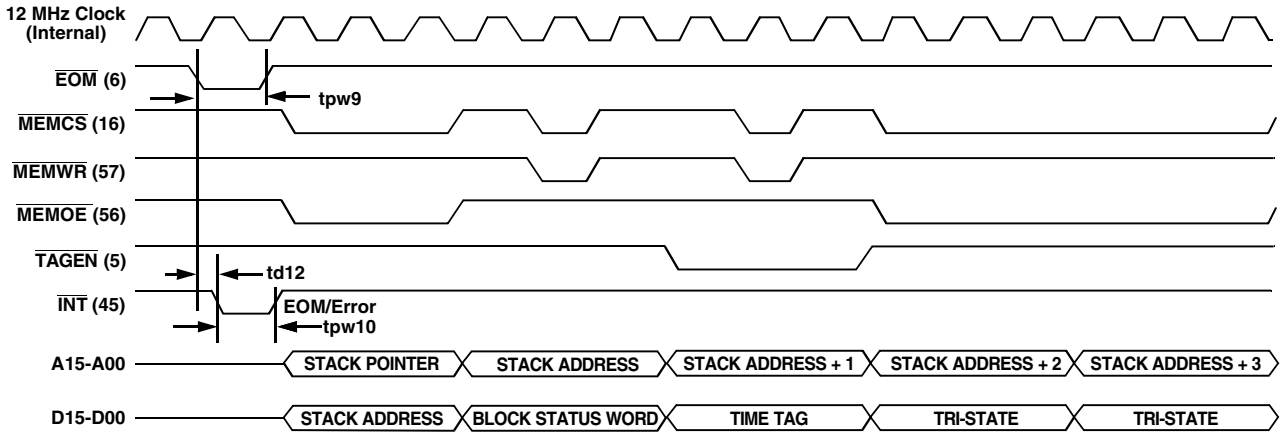


Figure 33 – BC EOM timing (no contention)

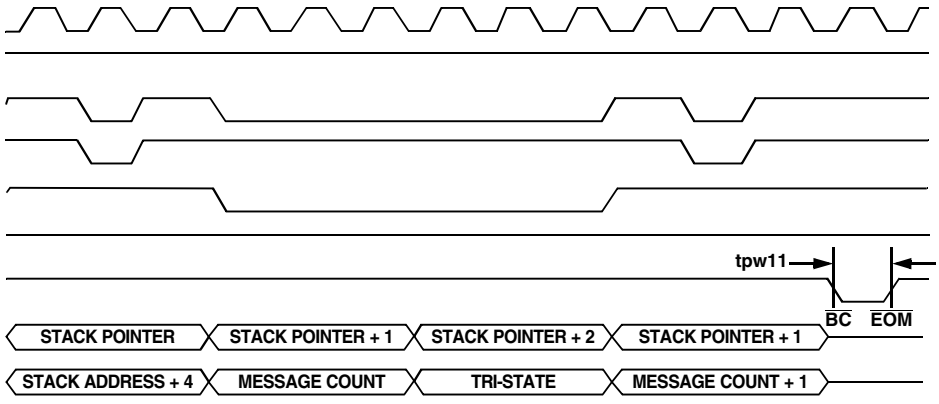
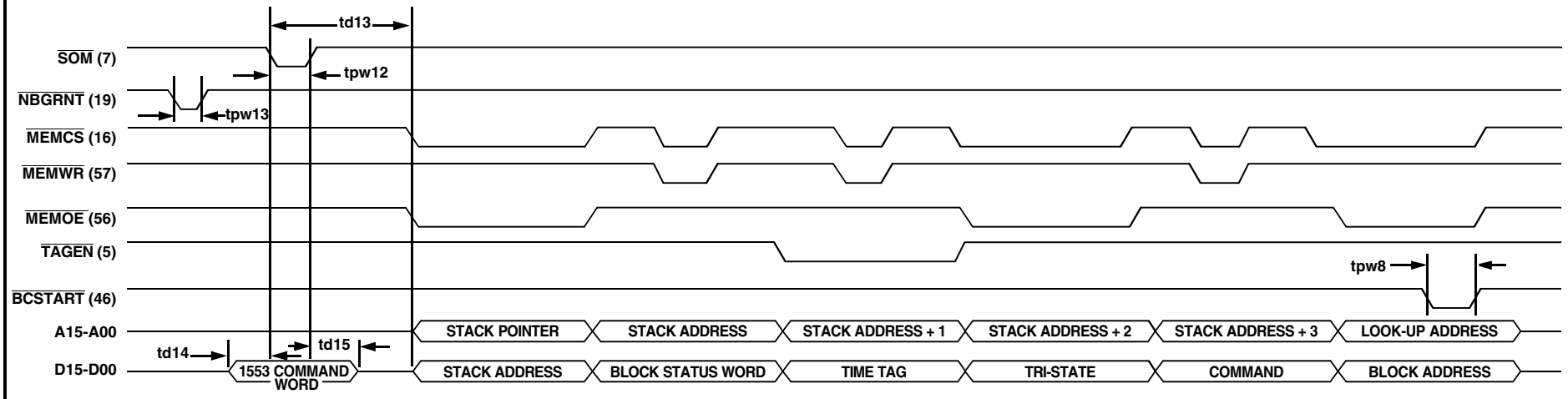


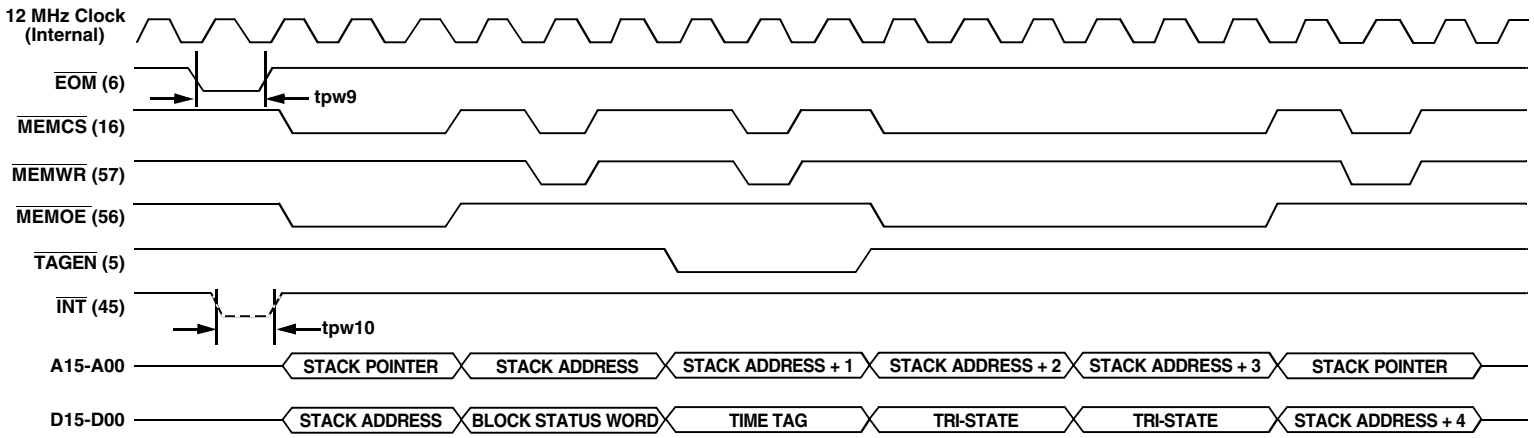
Figure 33 – BC EOM timing (no contention) con't



RTU SOM Timing (No Contention)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td13	RTU SOM Cycle DMA delay	-	200	ns
td14	1553 Command Word set-up time	60	-	ns
td15	1553 Command Word hold time	60	-	ns
tpw8	$\overline{\text{BCSTART}}$ low pulse width	70	-	ns
tpw12	SOM low pulse width	50	200	ns
tpw13	$\overline{\text{NBGRNT}}$ low pulse width	50	200	ns

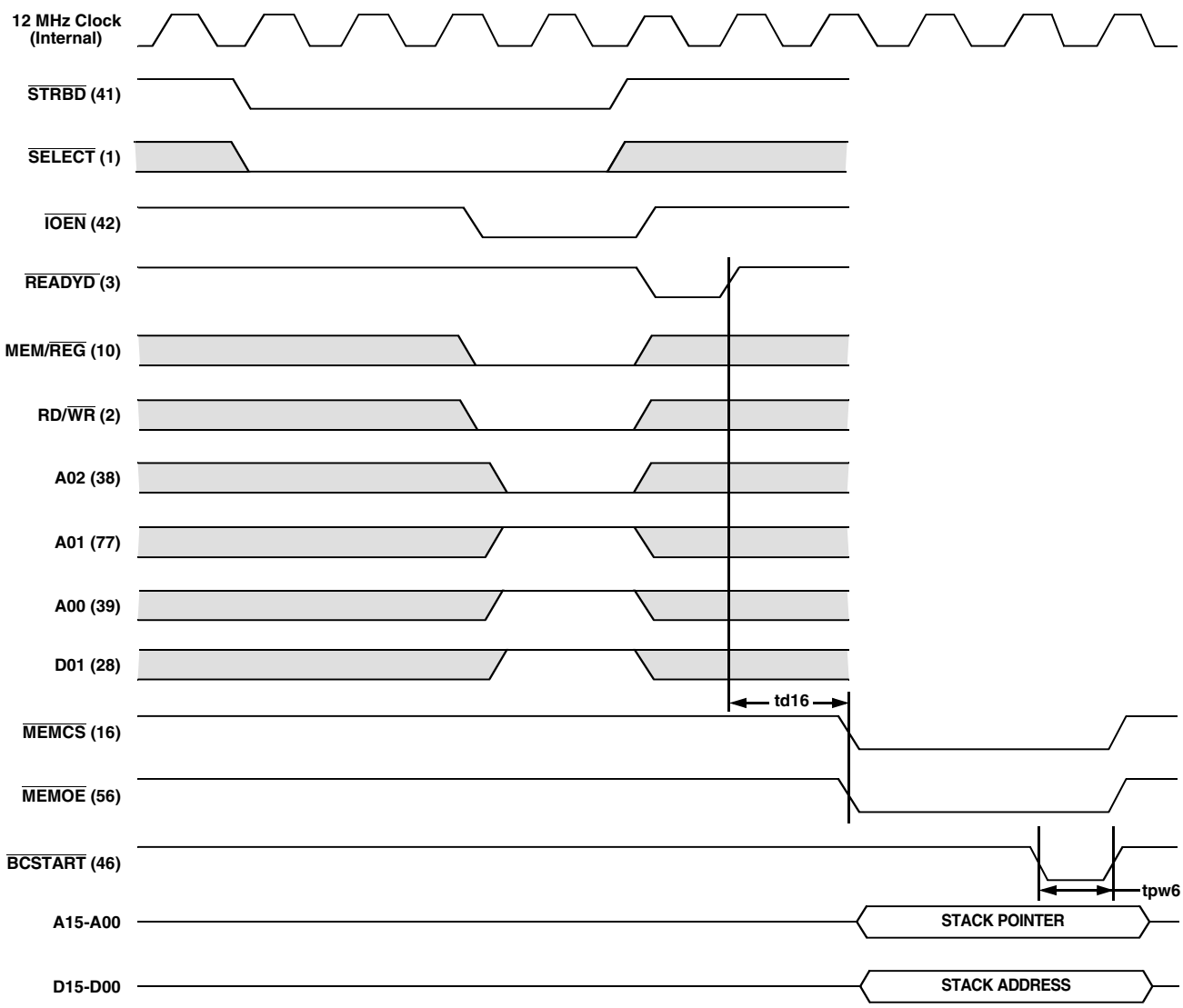
Figure 34 – RTU SOM (no contention)



RTU EOM Timing (No Contention)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
tpw9	$\overline{\text{RESET}}$ low delay	50	200	ns
tpw10	$\overline{\text{MSTRCLR}}$ low pulse width	*	tpw9	ns
* The min value of tpw10 equals tpw9 minus 30ns.				

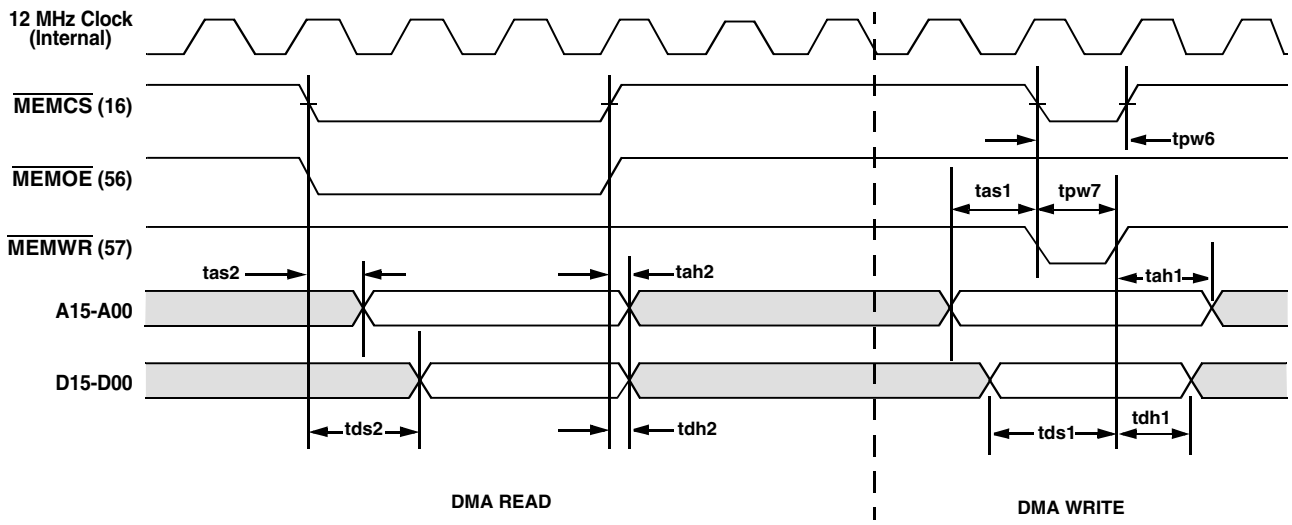
Figure 35 – RTU EOM timing (no contention)



MT SOM Timing (No Contention)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
td16	MT SOM Cycle DMA delay	-	120	ns
tpw6	$\overline{\text{BCSTART}}$ low pulse width	70	-	ns

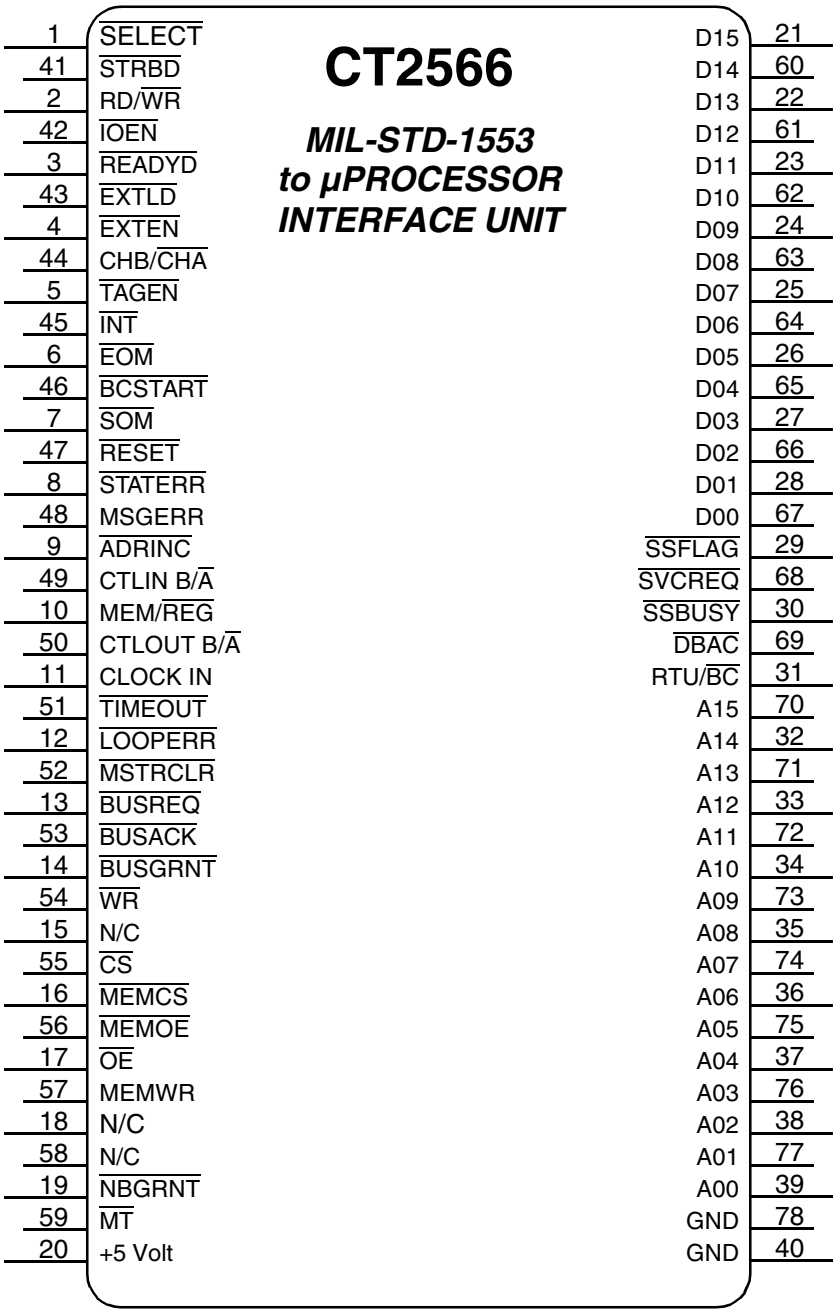
Figure 36 – MT SOM timing (no contention)



DMA Read/Write Timing (SOM/EOM Cycles)

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
tas1	DMA Address set-up time	40	-	ns
tah1	DMA Address hold time	60	-	ns
tds1	DMA Address set-up time	83	-	ns
tdh1	DMA Address hold time	30	-	ns
tas2	DMA Address set-up time	-	45	ns
tah2	DMA Address hold time	0	-	ns
tds2	DMA Address set-up time	-	83	ns
tdh2	DMA Address hold time	0	-	ns
tpw6	DMA $\overline{\text{MEMWR}}$ low pulse width	70	-	ns
tpw7	DMA $\overline{\text{MEMCS}}$ low pulse width	70	-	ns

Figure 37 – DMA Read/Write timing (SOM/EOM cycles)



DDIP Pin Connection Diagram, CT2566 and Pinout

Table 6 – CT2566 Pin Out Description (DDIP)

Pin #	Function	Pin #	Function
1	$\overline{\text{SELECT}}$	40	GND
2	RD/$\overline{\text{WR}}$	41	$\overline{\text{STRBD}}$
3	$\overline{\text{READYD}}$	42	$\overline{\text{IOEN}}$
4	$\overline{\text{EXTEN}}$	43	$\overline{\text{EXTLD}}$
5	$\overline{\text{TAGEN}}$	44	CHB/$\overline{\text{CHA}}$
6	$\overline{\text{EOM}}$	45	$\overline{\text{INT}}$
7	$\overline{\text{SOM}}$	46	$\overline{\text{BCSTART}}$
8	$\overline{\text{STATERR}}$	47	$\overline{\text{RESET}}$
9	$\overline{\text{ADRINC}}$	48	MSGERR
10	MEM/$\overline{\text{REG}}$	49	CTLIN B/$\overline{\text{A}}$
11	CLOCK IN	50	CTLOUT B/$\overline{\text{A}}$
12	$\overline{\text{LOOPERR}}$	51	$\overline{\text{TIMEOUT}}$
13	$\overline{\text{BUSREQ}}$	52	$\overline{\text{MSTRCLR}}$
14	$\overline{\text{BUSGRNT}}$	53	$\overline{\text{BUSACK}}$
15	N/C	54	$\overline{\text{WR}}$
16	$\overline{\text{MEMCS}}$	55	$\overline{\text{CS}}$
17	$\overline{\text{OE}}$	56	$\overline{\text{MEMOE}}$
18	N/C	57	MEMWR
19	$\overline{\text{NBGRNT}}$	58	N/C
20	+ 5 Volt	59	$\overline{\text{MT}}$
21	D15	60	D14
22	D13	61	D12
23	D11	62	D10
24	D09	63	D08
25	D07	64	D06
26	D05	65	D04
27	D03	66	D02
28	D01	67	D00
29	$\overline{\text{SSFLAG}}$	68	$\overline{\text{SVCREQ}}$
30	$\overline{\text{SSBUSY}}$	69	$\overline{\text{DBAC}}$
31	RTU/$\overline{\text{BC}}$	70	A15
32	A14	71	A13
33	A12	72	A11
34	A10	73	A09
35	A08	74	A07
36	A06	75	A05
37	A04	76	A03
38	A02	77	A01
39	A00	78	GND

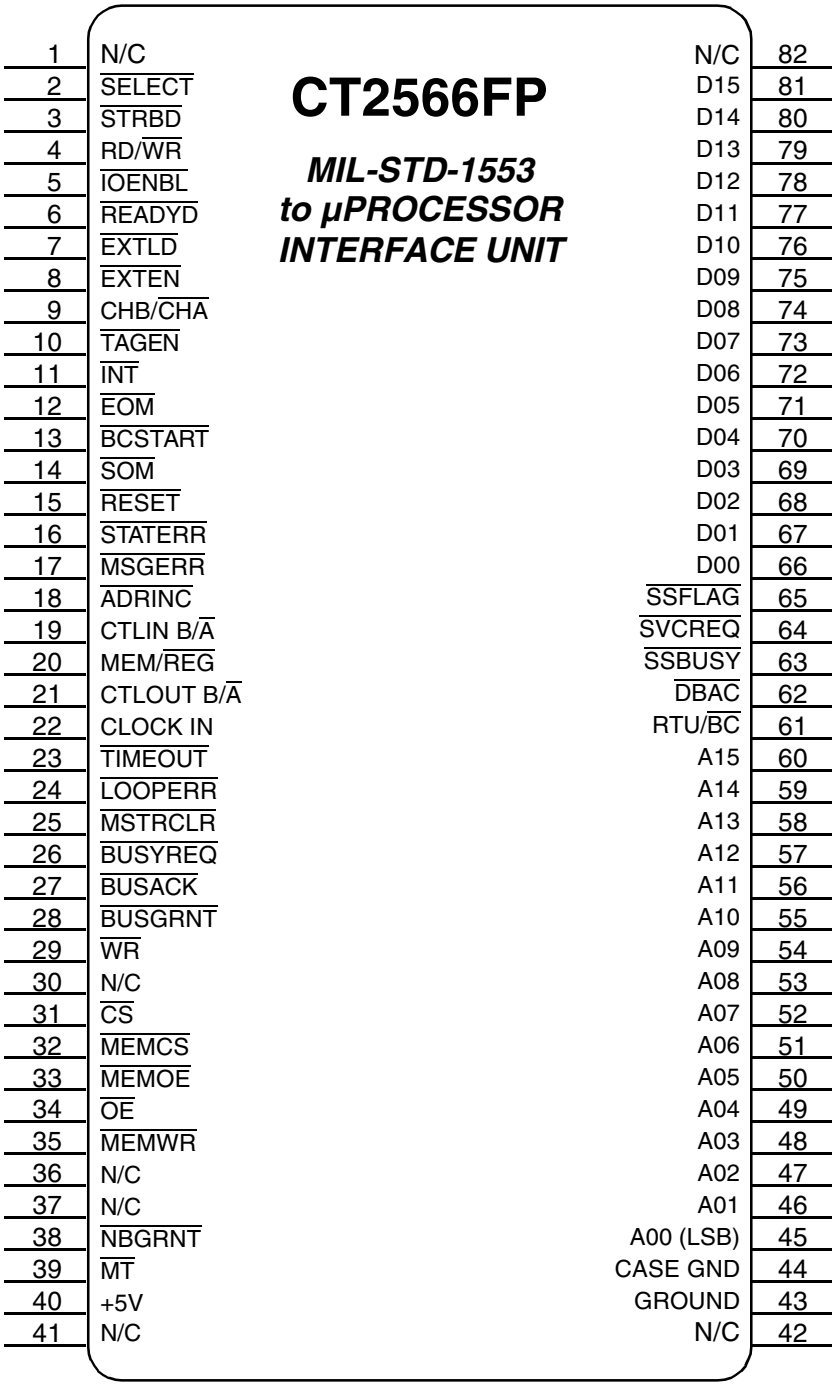
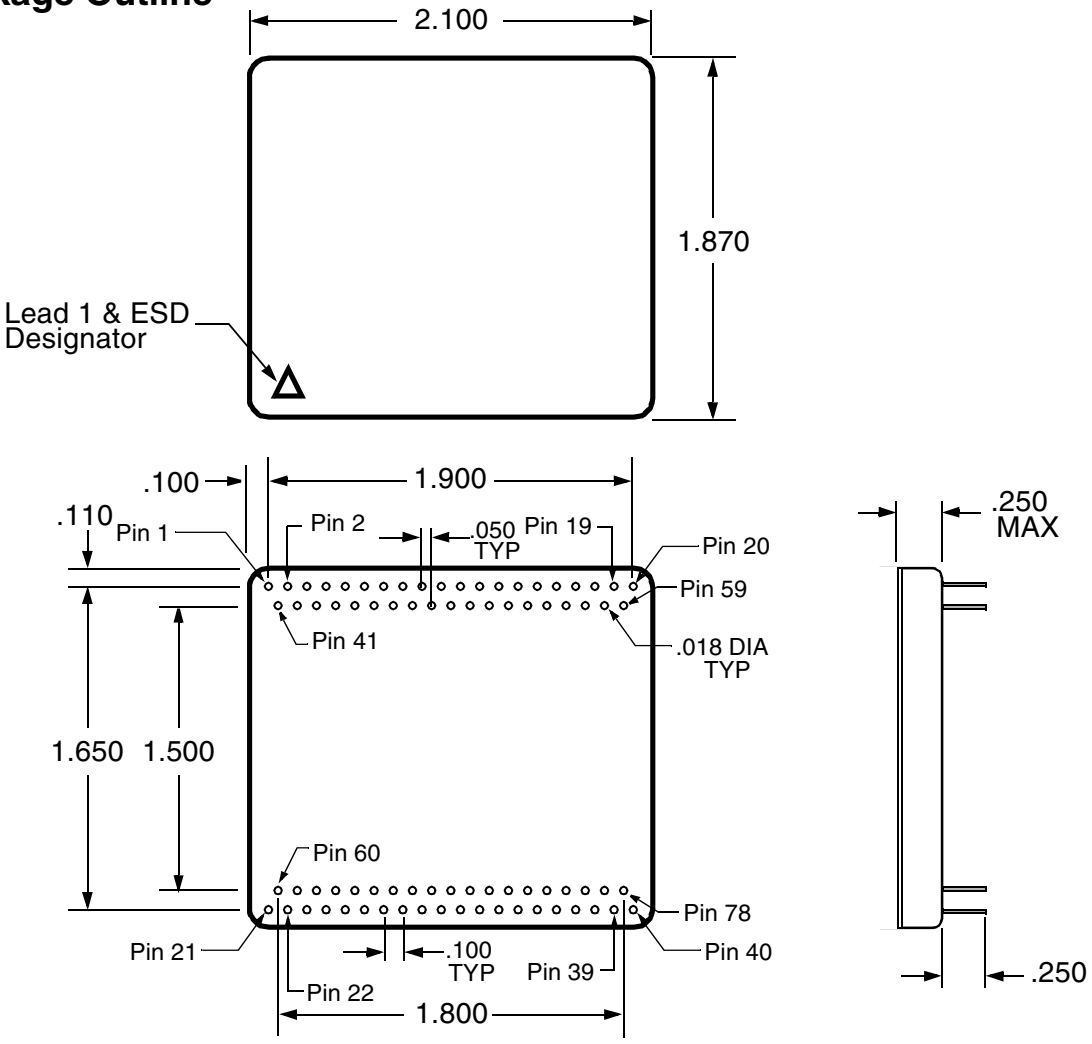


Table 7 – CT2566 Pin Out Description (FP)

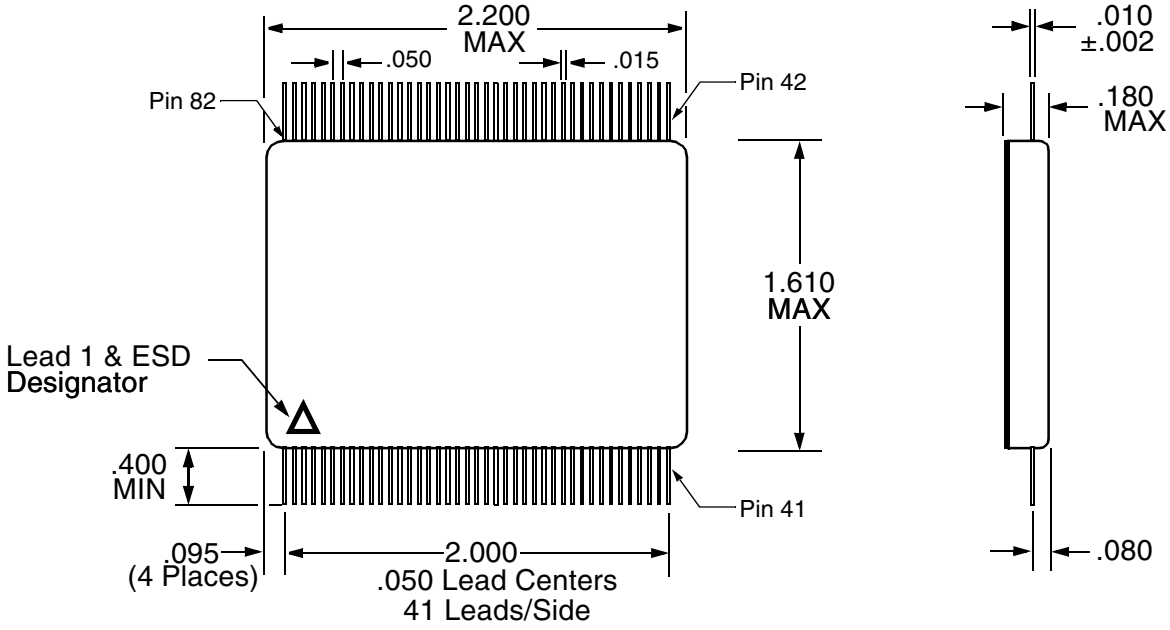
Pin #	Function	Pin #	Function
1	N/C	42	N/C
2	$\overline{\text{SELECT}}$	43	GROUND
3	$\overline{\text{STRBD}}$	44	CASE GND
4	RD/$\overline{\text{WR}}$	45	A00 (LSB)
5	$\overline{\text{IOENBL}}$	46	A01
6	$\overline{\text{READYD}}$	47	A02
7	$\overline{\text{EXTLD}}$	48	A03
8	$\overline{\text{EXTEN}}$	49	A04
9	CHB/$\overline{\text{CHA}}$	50	A05
10	$\overline{\text{TAGEN}}$	51	A06
11	$\overline{\text{INT}}$	52	A07
12	$\overline{\text{EOM}}$	53	A08
13	$\overline{\text{BCSTART}}$	54	A09
14	$\overline{\text{SOM}}$	55	A10
15	$\overline{\text{RESET}}$	56	A11
16	$\overline{\text{STATERR}}$	57	A12
17	$\overline{\text{MSGERR}}$	58	A13
18	$\overline{\text{ADRINC}}$	59	A14
19	CTLIN B/$\overline{\text{A}}$	60	A15
20	MEM/$\overline{\text{REG}}$	61	RTU/$\overline{\text{BC}}$
21	CTLOUT B/$\overline{\text{A}}$	62	$\overline{\text{DBAC}}$
22	CLOCK IN	63	$\overline{\text{SSBUSY}}$
23	$\overline{\text{TIMEOUT}}$	64	$\overline{\text{SVCREQ}}$
24	$\overline{\text{LOOPERR}}$	65	$\overline{\text{SSFLAG}}$
25	$\overline{\text{MSTRCLR}}$	66	D00
26	$\overline{\text{BUSYREQ}}$	67	D01
27	$\overline{\text{BUSACK}}$	68	D02
28	$\overline{\text{BUSGRNT}}$	69	D03
29	$\overline{\text{WR}}$	70	D04
30	N/C	71	D05
31	$\overline{\text{CS}}$	72	D06
32	$\overline{\text{MEMCS}}$	73	D07
33	$\overline{\text{MEMOE}}$	74	D08
34	$\overline{\text{OE}}$	75	D09
35	$\overline{\text{MEMWR}}$	76	D10
36	N/C	77	D11
37	N/C	78	D12
38	$\overline{\text{NBGRNT}}$	79	D13
39	$\overline{\text{MT}}$	80	D14
40	+5V	81	D15
41	N/C	82	N/C

Flat Package Pin Connection Diagram, CT2566 and Pinout

Plug In Package Outline



Flat Package Outline



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Ordering Information

Model Number	Screening	DESC SMD #	Package
CT2566	Military Temperature, -55°C to +125°C, Screened to the individual test methods of MIL-STD-883	-	Plug in
CT2566-FP		-	Flat Package

Specifications subject to change without notice

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