

ACT-S512K32V High Speed 3.3Volt 16 Megabit SRAM Multichip Module

Features

- 4 Low Power CMOS 512K x 8 SRAMs in one MCM
- Overall configuration as 512K x 32
- Input and Output TTL Compatible
- 17, 20, 25, 35 & 45ns Access Times, 15ns Available by Special Order
- Full Military (-55°C to +125°C) Temperature Range
- +3.3V Power Supply
- Choice of Surface Mount or PGA Type Co-fired Packages:
 - 68-Lead, Dual-Cavity CQFP (F2), .88"SQ x .20"max (.18"max thickness available, contact factory for details) (*Drops into the 68 Lead JEDEC .99"SQ CQFJ footprint*)
 - 66-Pin, PGA-Type (P1), 1.38"SQ x .245"max
 - 66-Pin, PGA-Type (P7), 1.08"SQ x .185"max
- Internal Decoupling Capacitors
- DESC SMD# Pending



General Description

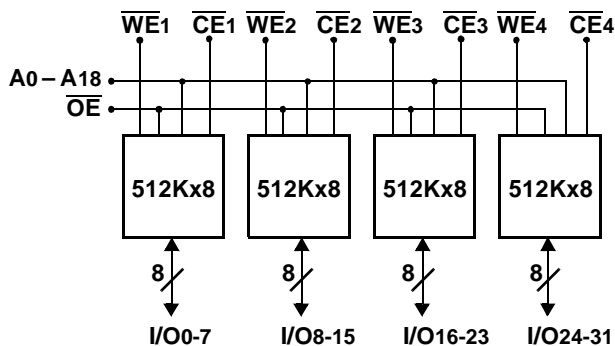
The ACT-S512K32V is a High Speed 4 megabit CMOS SRAM Multichip Module (MCM) designed for full temperature range, 3.3V Power Supply, military, space, or high reliability mass memory and fast cache applications.

The MCM can be organized as a 512K x 32 bits, 1M x 16 bits or 2M x 8 bits device and is input and output TTL compatible. Writing is executed when the write enable (\overline{WE}) and chip enable (\overline{CE}) inputs are low. Reading is accomplished when \overline{WE} is high and \overline{CE} and output enable (\overline{OE}) are both low. Access time grades of 17ns, 20ns, 25ns, 35ns and 45ns maximum are standard.

The products are designed for operation over the temperature range of -55°C to +125°C and screened under the full military environment. DESC Standard Military Drawing (SMD) part numbers are pending.

The ACT-S512K32V is manufactured in Aeroflex's 80,000ft² MIL-PRF-38534 certified facility in Plainview, N.Y.

Block Diagram – PGA Type Package(P1,P7) & CQFP(F2)



Pin Description

I/O0-31	Data I/O
A0-18	Address Inputs
$\overline{WE}1-4$	Write Enables
$\overline{CE}1-4$	Chip Enables
\overline{OE}	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

Absolute Maximum Ratings

Symbol	Rating	Range	Units
T _C	Case Operating Temperature	Speed 15ns	-40 to +85
		Speed 17ns to 45ns	-55 to +125
T _{STG}	Storage Temperature		-65 to +150
P _D	Maximum Package Power Dissipation P1,P7 Package F2 Package		3.0 W
			2.7 W
∅ _{J-C}	Hottest Die, Max Thermal Resistance - Junction to Case P1,P7 Package F2 Package		2.0 °C/W
			8.0 °C/W
V _G	Maximum Signal Voltage to Ground		-0.5 to +4.6 V
T _L	Maximum Lead Temperature (10 seconds)		300 °C

Normal Operating Conditions

Symbol	Parameter	Minimum	Maximum	Units
V _{CC}	Power Supply Voltage	+3.0	+3.6	V
V _{IH}	Input High Voltage	+2.0	V _{CC} + 0.3	V
V _{IL}	Input Low Voltage	-0.3	+0.8	V

Capacitance

(f = 1MHz, T_C = 25°C)

Symbol	Parameter	Maximum	Units
C _{AD}	A ₀ – A ₁₈ Capacitance	50	pF
C _{OE}	\overline{OE} Capacitance	50	pF
C _{WE}	Write Enable Capacitance	20	pF
C _{CE}	Chip Enable Capacitance	20	pF
C _{I/O}	I/O ₀ – I/O ₃₁ Capacitance	20	pF

Capacitance is guaranteed by design but not tested.

DC Characteristics

(3.0Vdc ≤ V_{CC} ≤ 3.6Vdc, V_{SS} = 0V, T_C = -55°C to +125°C, Unless otherwise specified)

Parameter	Sym	Conditions	ALL Speeds		Units
			Min	Max	
Input Leakage Current	I _{LI}	V _{CC} = Max, V _{IN} = 0 or V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$, V _{OUT} = 0 or V _{CC}		10	μA
Operating Supply Current 32 Bit Mode	I _{CC1} x32	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 5 MHz, V _{CC} = Max, CMOS Compatible		600	mA
Standby Current	I _{SB1}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$, f = 5 MHz, V _{CC} = Max, CMOS Compatible		80	mA
Operating Supply Current 32 Bit Mode	I _{CC2} x32	$\overline{CE} = V_{IL}$, $\overline{OE} = V_{IH}$, f = 50 MHz, V _{CC} = Max, CMOS Compatible		750	mA
Standby Current	I _{SB2}	$\overline{CE} = V_{CC}$, $\overline{OE} = V_{IH}$, f = 50 MHz, V _{CC} = Max, CMOS Compatible		240	mA
Output Low Voltage	V _{OL}	I _{OL} = 8 mA, V _{CC} = Min		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0 mA, V _{CC} = Min	2.4		V

AC Characteristics

(V_{CC} = 3.3V, V_{SS} = 0V, T_c = -55°C to +125°C)

Read Cycle

Parameter	Sym	<u>-017</u>		<u>-020</u>		<u>-025</u>		<u>-035</u>		<u>-045</u>		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t _{RC}	17		20		25		35		45		ns
Address Access Time	t _{AA}		17		20		25		35		45	ns
Chip Enable Access Time	t _{ACS}		17		20		25		35		45	ns
Output Hold from Address Change	t _{OH}	0		0		0		0		0		ns
Output Enable to Output Valid	t _{OE}		9		10		12		25		35	ns
Chip Enable to Output in Low Z *	t _{CLZ}	3		3		3		3		3		ns
Output Enable to Output in Low Z *	t _{OLZ}	0		0		0		0		0		ns
Chip Deselect to Output in High Z *	t _{CHZ}		8		8		10		15		15	ns
Output Disable to Output in High Z *	t _{OHZ}		8		8		10		15		15	ns

* Parameters guaranteed by design but not tested

Write Cycle

Parameter	Sym	<u>-017</u>		<u>-020</u>		<u>-025</u>		<u>-035</u>		<u>-045</u>		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Write Cycle Time	t _{WC}	17		20		25		35		45		ns
Chip Enable to End of Write	t _{CW}	15		15		20		30		35		ns
Address Valid to End of Write	t _{AW}	15		15		20		30		35		ns
Data Valid to End of Write	t _{DW}	12		12		15		20		30		ns
Write Pulse Width	t _{WP}	13		13		15		25		35		ns
Address Setup Time	t _{AS}	0		0		0		0		0		ns
Output Active from End of Write *	t _{OW}	0		0		0		0		0		ns
Write to Output in High Z *	t _{WHZ}		8		11		13		15		15	ns
Data Hold from Write Time	t _{DH}	0		0		0		0		0		ns
Address Hold Time	t _{AH}	0		1		2		2		2		ns

* Parameters guaranteed by design but not tested

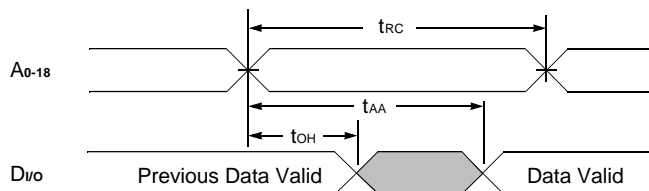
Truth Table

Mode	CE	OE	WE	Data I/O	Power
Standby	H	X	X	High Z	Standby (deselect/power down)
Read	L	L	H	Data Out	Active
Read	L	H	H	High Z	Active (deselected)
Write	L	X	L	Data In	Active

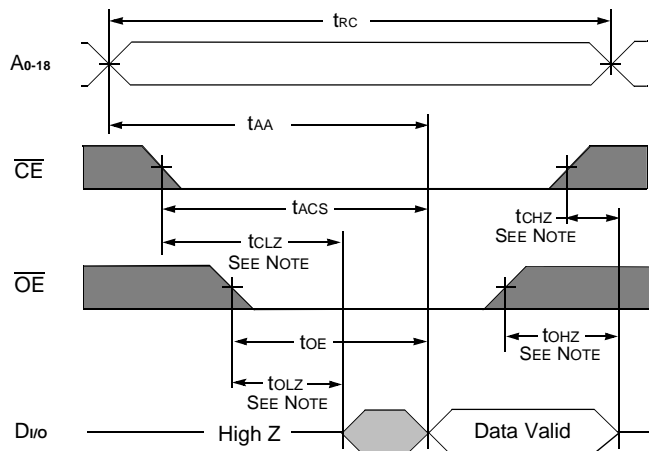
Timing Diagrams

Read Cycle Timing Diagrams

Read Cycle 1 ($\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$)



Read Cycle 2 ($\overline{WE} = V_{IH}$)



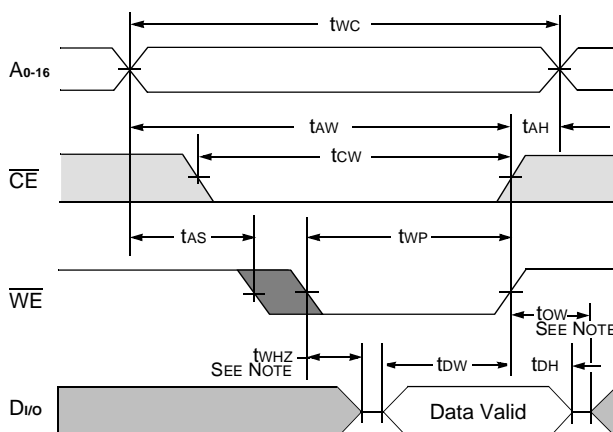
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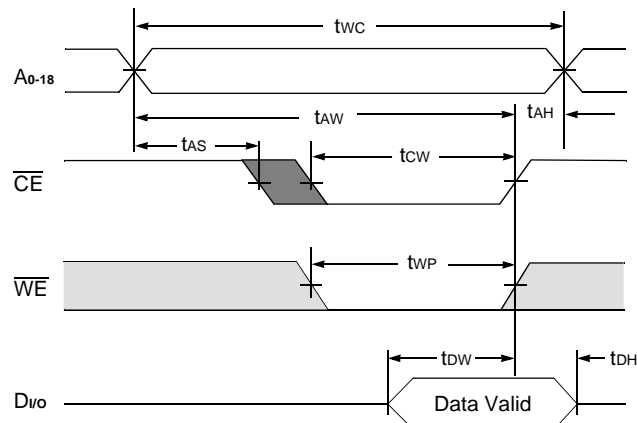
DON'T CARE

Write Cycle Timing Diagrams

Write Cycle 1 (\overline{WE} Controlled, $\overline{OE} = V_{IL}$)

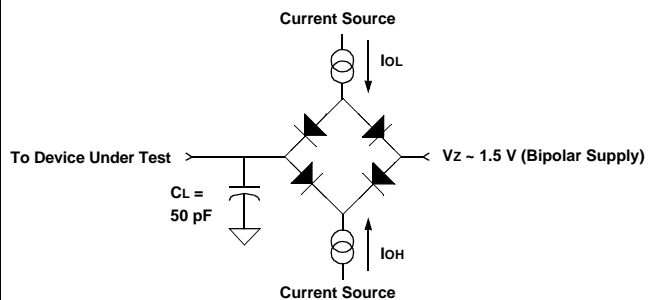


Write Cycle 2 (\overline{CE} Controlled, $\overline{OE} = V_{IH}$)



Note: Guaranteed by design, but not tested.

AC Test Circuit



Parameter	Typical	Units
Input Pulse Level	0 – 3.0	V
Input Rise and Fall	5	ns
Input and Output Timing Reference Level	1.5	V

Notes:

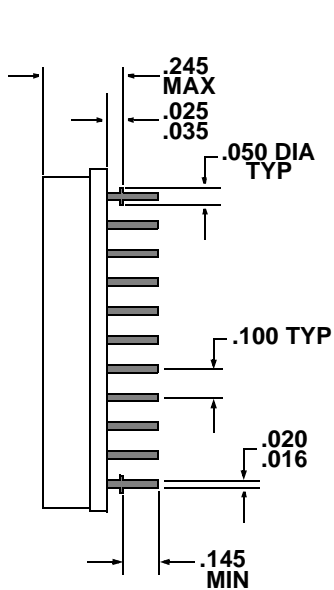
- 1) Vz is programmable from -2V to +4.6V.
- 2) IoL and IoH programmable from 0 to 16 mA.
- 3) Tester Impedance Zo = 75Ω.
- 4) Vz is typically the midpoint of VOH and VOL.
- 5) IoL and IoH are adjusted to simulate a typical resistance load circuit.
- 6) ATE Tester includes jig capacitance.

Pin Numbers & Functions

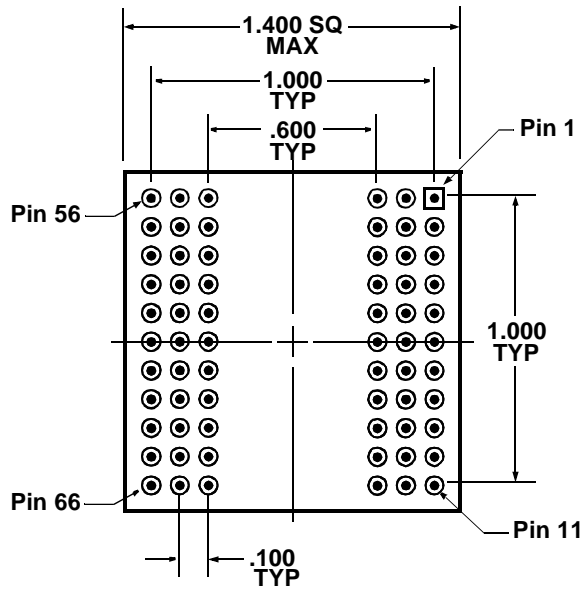
66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O8	18	A12	35	I/O25	52	$\overline{WE}3$
2	I/O9	19	V _{cc}	36	I/O26	53	$\overline{CS}3$
3	I/O10	20	$\overline{CS}1$	37	A6	54	GND
4	A13	21	NC	38	A7	55	I/O19
5	A14	22	I/O3	39	NC	56	I/O31
6	A15	23	I/O15	40	A8	57	I/O30
7	A16	24	I/O14	41	A9	58	I/O29
8	A17	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A0
10	I/O1	27	\overline{OE}	44	I/O18	61	A1
11	I/O2	28	A18	45	V _{cc}	62	A2
12	$\overline{WE}2$	29	$\overline{WE}1$	46	$\overline{CS}4$	63	I/O23
13	$\overline{CS}2$	30	I/O7	47	$\overline{WE}4$	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A3	66	I/O20
16	A10	33	I/O4	50	A4		
17	A11	34	I/O24	51	A5		

"P1" — 1.40" SQ PGA Type Package

Side View



Bottom View

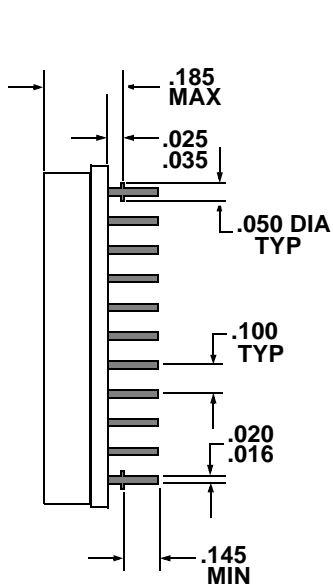


Pin Numbers & Functions

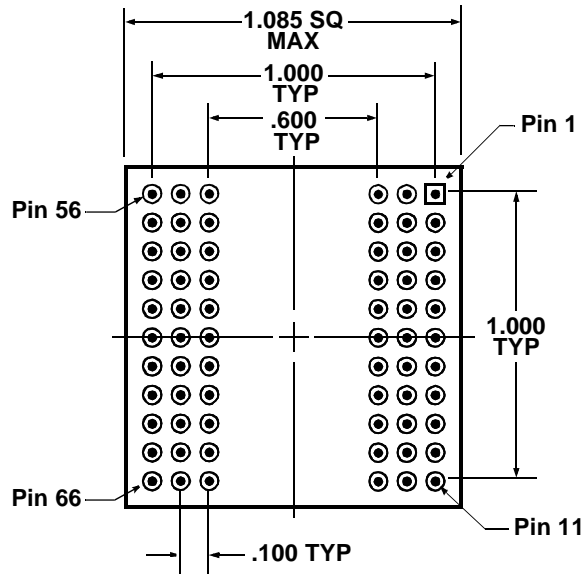
66 Pins — PGA-Type							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	I/O8	18	A12	35	I/O25	52	\overline{WE}_3
2	I/O9	19	V _{cc}	36	I/O26	53	\overline{CE}_3
3	I/O10	20	\overline{CE}_1	37	A6	54	GND
4	A13	21	NC	38	A7	55	I/O19
5	A14	22	I/O3	39	NC	56	I/O31
6	A15	23	I/O15	40	A8	57	I/O30
7	A16	24	I/O14	41	A9	58	I/O29
8	A17	25	I/O13	42	I/O16	59	I/O28
9	I/O0	26	I/O12	43	I/O17	60	A0
10	I/O1	27	\overline{OE}	44	I/O18	61	A1
11	I/O2	28	A18	45	V _{cc}	62	A2
12	\overline{WE}_2	29	\overline{WE}_1	46	\overline{CE}_4	63	I/O23
13	\overline{CE}_2	30	I/O7	47	\overline{WE}_4	64	I/O22
14	GND	31	I/O6	48	I/O27	65	I/O21
15	I/O11	32	I/O5	49	A3	66	I/O20
16	A10	33	I/O4	50	A4		
17	A11	34	I/O24	51	A5		

"P7" — 1.08" SQ PGA Type Package

Side View



Bottom View



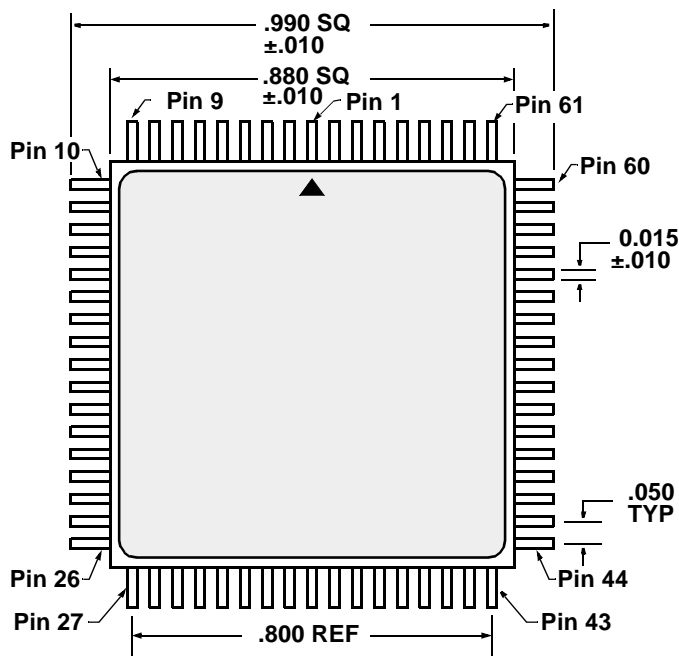
All dimensions in inches

Pin Numbers & Functions

68 Pins — Dual-Cavity CQFP							
Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	GND	18	GND	35	\overline{OE}	52	GND
2	$\overline{CE3}$	19	I/O8	36	$\overline{CE2}$	53	I/O23
3	A5	20	I/O9	37	A17	54	I/O22
4	A4	21	I/O10	38	$\overline{WE2}$	55	I/O21
5	A3	22	I/O11	39	$\overline{WE3}$	56	I/O20
6	A2	23	I/O12	40	$\overline{WE4}$	57	I/O19
7	A1	24	I/O13	41	A18	58	I/O18
8	A0	25	I/O14	42	NC	59	I/O17
9	NC	26	I/O15	43	NC	60	I/O16
10	I/O0	27	V _{CC}	44	I/O31	61	V _{CC}
11	I/O1	28	A11	45	I/O30	62	A10
12	I/O2	29	A12	46	I/O29	63	A9
13	I/O3	30	A13	47	I/O28	64	A8
14	I/O4	31	A14	48	I/O27	65	A7
15	I/O5	32	A15	49	I/O26	66	A6
16	I/O6	33	A16	50	I/O25	67	$\overline{WE1}$
17	I/O7	34	$\overline{CE1}$	51	I/O24	68	$\overline{CE4}$

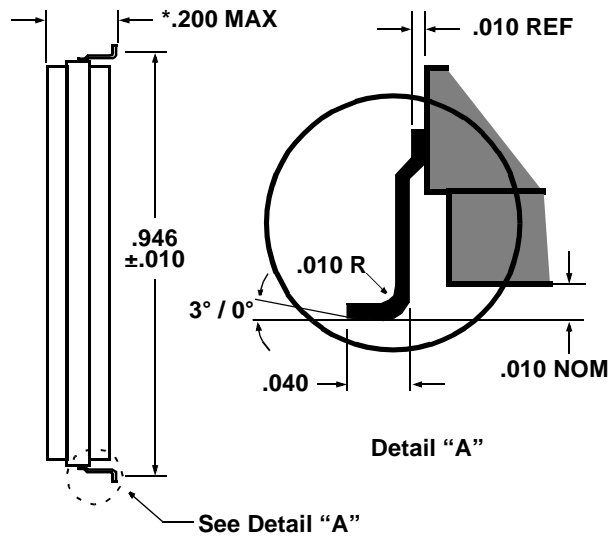
Package Outline "F2" — Dual-Cavity CQFP

Top View



All dimensions in inches

(* .180 MAX available, call factory for details)



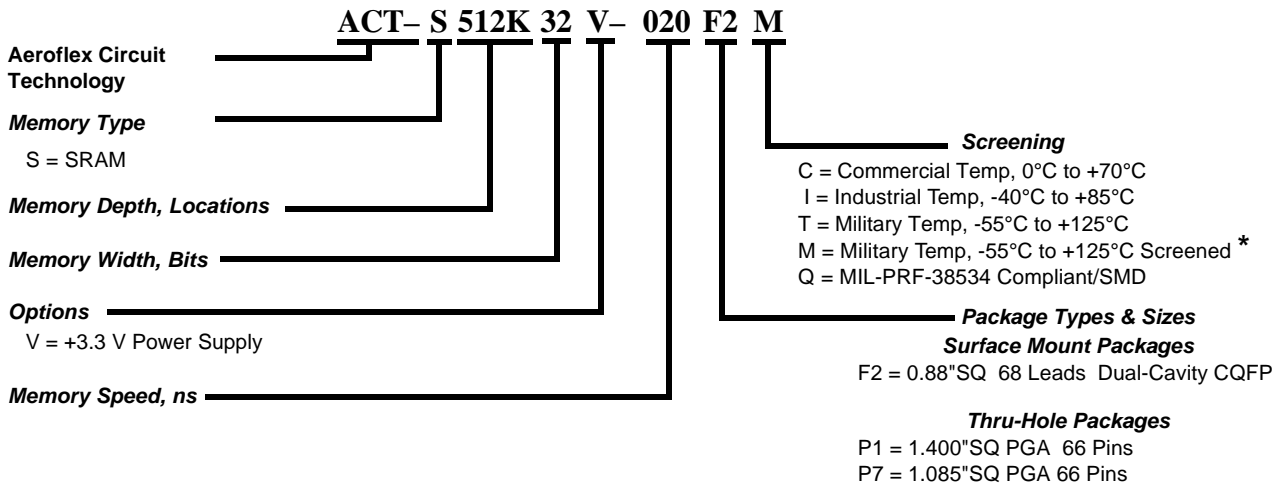
Note: Metallic lids and walls - both sides



Ordering Information

Model Number	DESC Part Number	Speed	Package
ACT-S512K32V-017F2Q	(Pending)	17ns	.88"sq CQFP
ACT-S512K32V-020F2Q	(Pending)	20ns	.88"sq CQFP
ACT-S512K32V-025F2Q	(Pending)	25ns	.88"sq CQFP
ACT-S512K32V-035F2Q	(Pending)	35ns	.88"sq CQFP
ACT-S512K32V-045F2Q	(Pending)	45ns	.88"sq CQFP
ACT-S512K32V-017P1Q	(Pending)	17ns	1.38"sq PGA-Type
ACT-S512K32V-020P1Q	(Pending)	20ns	1.38"sq PGA-Type
ACT-S512K32V-025P1Q	(Pending)	25ns	1.38"sq PGA-Type
ACT-S512K32V-035P1Q	(Pending)	35ns	1.38"sq PGA-Type
ACT-S512K32V-045P1Q	(Pending)	45ns	1.38"sq PGA-Type
ACT-S512K32V-017P7Q	(Pending)	17ns	1.08"sq PGA-Type
ACT-S512K32V-020P7Q	(Pending)	20ns	1.08"sq PGA-Type
ACT-S512K32V-025P7Q	(Pending)	25ns	1.08"sq PGA-Type
ACT-S512K32V-035P7Q	(Pending)	35ns	1.08"sq PGA-Type
ACT-S512K32V-045P7Q	(Pending)	45ns	1.08"sq PGA-Type

Part Number Breakdown



* Screened to the individual test methods of MIL-STD-883

Specifications subject to change without notice

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