Low-Cost, 300 MHz Rail-to-Rail Amplifiers

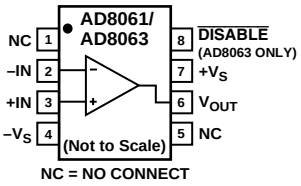
AD8061/AD8062/AD8063

FEATURES
Low Cost
Single (AD8061), Dual (AD8062)
Single with Disable (AD8063)
Rail-to-Rail Output Swing
6 mV V_{OS}
High Speed
300 MHz, –3 dB Bandwidth (G = 1)
800 V/μs Slew Rate
8.5 nV/√Hz @ 5 V
35 ns Settling Time to 0.1% with 1 V Step
Operates on 2.7 V to 8 V Supplies
Input Voltage Range = –0.2 V to +3.2 V with V_S = 5
Excellent Video Specs (R_L = 150 Ω, G = 2)
Gain Flatness 0.1 dB to 30 MHz
0.01% Differential Gain Error
0.04° Differential Phase Error
35 ns Overload Recovery
Low Power
6.8 mA/Amplifier Typical Supply Current
AD8063 400 μA when Disabled
Small Packaging
AD8061 Available in SOIC-8 and SOT-23-5
AD8062 Available in SOIC-8 and μSOIC
AD8063 Available in SOIC-8 and SOT-23-6

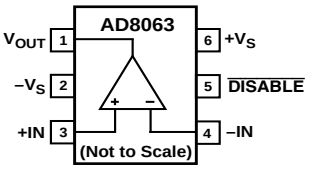
APPLICATIONS
Imaging
Photodiode Preamp
Professional Video and Cameras
Hand Sets
DVD/CD
Base Stations
Filters
A-to-D Driver

CONNECTION DIAGRAMS
(Top Views)

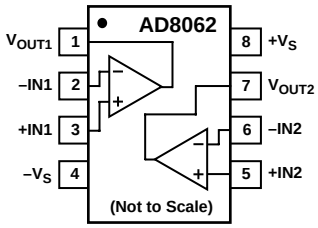
SOIC-8 (R)



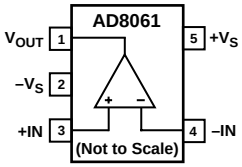
SOT-23-6 (RT)



SOIC-8 (R) and μSOIC (RM)



SOT-23-5 (RT)



The AD8061, AD8062, and AD8063 offer a typical low power of 6.8 mA/amplifier, while being capable of delivering up to 50 mA of load current. The AD8063 has a power-down disable feature that reduces the supply current to 400 μA. These features make the AD8063 ideal for portable and battery-powered applications where size and power is critical.

PRODUCT DESCRIPTION

The AD8061, AD8062, and AD8063 are rail-to-rail output voltage feedback amplifiers offering ease of use and low cost. They have bandwidth and slew rate typically found in current feedback amplifiers. All have a wide input common-mode voltage range and output voltage swing, making them easy to use on single supplies as low as 2.7 V.

Despite being low cost, the AD8061, AD8062, and AD8063 provide excellent overall performance. For video applications their differential gain and phase errors are 0.01% and 0.04° into a 150 Ω load, along with 0.1 dB flatness out to 30 MHz. Additionally, they offer wide bandwidth to 300 MHz along with 800 V/μs slew rate.

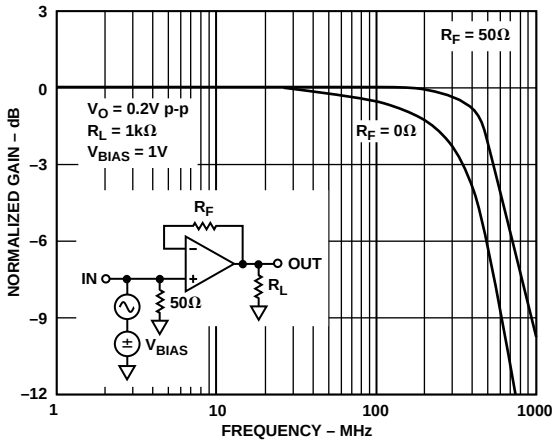


Figure 1. Small Signal Response, R_F = 0 Ω, 50 Ω

REV. A

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AD8061/AD8062/AD8063–SPECIFICATIONS (T_A = 25°C, V_S = 5 V, R_L = 1 kΩ, V_O = 1 V, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = 1, V_O = 0.2 V p-p	150	320		MHz
	G = –1, +2, V_O = 0.2 V p-p	60	115		MHz
–3 dB Large Signal Bandwidth	G = 1, V_O = 1 V p-p		280		MHz
Bandwidth for 0.1 dB Flatness	G = 1, V_O = 0.2 V p-p		30		MHz
Slew Rate	G = 1, V_O = 2 V Step, R_L = 2 kΩ	500	650		V/µs
	G = 2, V_O = 2 V Step, R_L = 2 kΩ	300	500		V/µs
Settling Time to 0.1%	G = 2, V_O = 2 V Step		35		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–77		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–50		dBc
Crosstalk, Output to Output	f = 5 MHz, G = 2, AD8062		–90		dBc
Input Voltage Noise	f = 100 kHz		8.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.2		pA/√Hz
Differential Gain Error (NTSC)	G = 2, R_L = 150 Ω		0.01		%
Differential Phase Error (NTSC)	G = 2, R_L = 150 Ω		0.04		Degree
Third Order Intercept	f = 10 MHz		28		dBc
SFDR	f = 5 MHz		62		dB
DC PERFORMANCE					
Input Offset Voltage			1	6	mV
	T_{MIN} to T_{MAX}		2	6	mV
Input Offset Voltage Drift			3.5		µV/°C
Input Bias Current			3.5	9	µA
	T_{MIN} to T_{MAX}		4	9	µA
Input Offset Current			0.3	4.5	±µA
Open-Loop Gain	V_O = 0.5 V to 4.5 V, R_L = 150 Ω	68	70		dB
	V_O = 0.5 V to 4.5 V, R_L = 2 kΩ	74	90		dB
INPUT CHARACTERISTICS					
Input Resistance			13		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range			–0.2 to +3.2		V
Common-Mode Rejection Ratio	V_{CM} = –0.2 V to +3.2 V	62	80		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing—Load Resistance	R_L = 150 Ω	0.3	0.1 to 4.5	4.75	V
Is Terminated at Midsupply	R_L = 2 kΩ	0.25	0.1 to 4.9	4.85	V
Output Current	V_O = 0.5 V to 4.5 V	25	50		mA
Capacitive Load Drive, V_{OUT} = 0.8 V	30% Overshoot: G = 1, R_S = 0 Ω		25		pF
	G = 2, R_S = 4.7 Ω		300		pF
POWER-DOWN DISABLE					
Turn-On Time			40		ns
Turn-Off Time			300		ns
$\overline{\text{DISABLE}}$ Voltage—Off			2.8		V
$\overline{\text{DISABLE}}$ Voltage—On			3.2		V
POWER SUPPLY					
Operating Range		2.7	5	8	V
Quiescent Current per Amplifier			6.8	9.5	mA
Supply Current when Disabled (AD8063 Only)			0.4		mA
Power Supply Rejection Ratio	ΔV_S = 2.7 V to 5 V	72	80		dB

Specifications subject to change without notice.

SPECIFICATIONS (T_A = 25°C, V_S = 3 V, R_L = 1 kΩ, V_O = 1 V, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = 1, V_O = 0.2 V p-p	150	300		MHz
	G = –1, +2, V_O = 0.2 V p-p	60	115		MHz
–3 dB Large Signal Bandwidth	G = 1, V_O = 1 V p-p		250		MHz
Bandwidth for 0.1 dB Flatness	G = 1, V_O = 0.2 V p-p		30		MHz
Slew Rate	G = 1, V_O = 1 V Step, R_L = 2 kΩ	190	280		V/µs
	G = 2, V_O = 1.5 V Step, R_L = 2 kΩ	180	230		V/µs
Settling Time to 0.1%	G = 2, V_O = 1 V Step		40		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–60		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–44		dBc
Crosstalk, Output to Output	f = 5 MHz, G = 2		–90		dBc
Input Voltage Noise	f = 100 kHz		8.5		$nV/\sqrt{Hz}$
Input Current Noise	f = 100 kHz		1.2		$pA/\sqrt{Hz}$
DC PERFORMANCE					
Input Offset Voltage			1	6	mV
	T_{MIN} to T_{MAX}		2	6	mV
Input Offset Voltage Drift			3.5		µV/°C
Input Bias Current			3.5	8.5	µA
	T_{MIN} to T_{MAX}		4	8.5	µA
Input Offset Current			0.3	4.5	±µA
Open-Loop Gain	V_O = 0.5 V to 2.5 V, R_L = 150 Ω	66	70		dB
	V_O = 0.5 V to 2.5 V, R_L = 2 kΩ	74	90		dB
INPUT CHARACTERISTICS					
Input Resistance			13		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range			–0.2 to +1.2		V
Common-Mode Rejection Ratio	V_{CM} = –0.2 V to +1.2 V		80		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	0.3	0.1 to 2.87	2.85	V
	R_L = 2 kΩ	0.3	0.1 to 2.9	2.90	V
Output Current	V_O = 0.5 V to 2.5 V		25		mA
Capacitive Load Drive, V_{OUT} = 0.8 V	30% Overshoot, G = 1, R_S = 0 Ω,		25		pF
	G = 2, R_S = 4.7 Ω		300		pF
POWER-DOWN DISABLE					
Turn-On Time			40		ns
Turn-Off Time			300		ns
$\overline{\text{DISABLE}}$ Voltage—Off			0.8		V
$\overline{\text{DISABLE}}$ Voltage—On			1.2		V
POWER SUPPLY					
Operating Range		2.7		3	V
Quiescent Current per Amplifier			6.8	9	mA
Supply Current when Disabled (AD8063 Only)			0.4		mA
Power Supply Rejection Ratio		72	80		dB

Specifications subject to change without notice.

AD8061/AD8062/AD8063–SPECIFICATIONS (T_A = 25°C, V_S = 2.7 V, R_L = 1 kΩ, V_O = 1 V, unless otherwise noted)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Small Signal Bandwidth	G = 1, V_O = 0.2 V p-p	150	300		MHz
	G = –1, +2, V_O = 0.2 V p-p	60	115		MHz
	G = 1, V_O = 1 V p-p		230		MHz
Bandwidth for 0.1 dB Flatness	G = 1, V_O = 0.2 V p-p, V_O DC = 1 V		30		MHz
Slew Rate	G = 1, V_O = 0.7 V Step, R_L = 2 kΩ	110	150		V/µs
	G = 2, V_O = 1.5 V Step, R_L = 2 kΩ	95	130		V/µs
Settling Time to 0.1%	G = 2, V_O = 1 V Step		40		ns
NOISE/DISTORTION PERFORMANCE					
Total Harmonic Distortion	f_C = 5 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–60		dBc
	f_C = 20 MHz, V_O = 2 V p-p, R_L = 1 kΩ		–44		dBc
Crosstalk, Output to Output	f = 5 MHz, G = 2		–90		dBc
Input Voltage Noise	f = 100 kHz		8.5		nV/√Hz
Input Current Noise	f = 100 kHz		1.2		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			1	6	mV
	T_{MIN} to T_{MAX}		2	6	mV
Input Offset Voltage Drift			3.5		µV/°C
Input Bias Current			3.5		µA
	T_{MIN} to T_{MAX}		4	8.5	µA
Input Offset Current			0.3	4.5	±µA
Open-Loop Gain	V_O = 0.5 V to 2.2 V, R_L = 150 Ω	63	70		dB
	V_O = 0.5 V to 2.2 V, R_L = 2 kΩ	74	90		dB
INPUT CHARACTERISTICS					
Input Resistance			13		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage Range			–0.2 to +0.9		V
Common-Mode Rejection Ratio	V_{CM} = –0.2 V to +0.9 V		80		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	R_L = 150 Ω	0.3	0.1 to 2.55	2.55	V
	R_L = 2 kΩ	0.25	0.1 to 2.6	2.6	V
Output Current	V_O = 0.5 V to 2.2 V		25		mA
Capacitive Load Drive, V_{OUT} = 0.8 V	30% Overshoot: G = 1, R_S = 0 Ω,		25		pF
	G = 2, R_S = 4.7 Ω	300			pF
POWER-DOWN DISABLE					
Turn-On Time			40		ns
Turn-Off Time			300		ns
$\overline{\text{DISABLE}}$ Voltage—Off			0.5		V
$\overline{\text{DISABLE}}$ Voltage—On			0.9		V
POWER SUPPLY					
Operating Range		2.7		8	V
Quiescent Current per Amplifier			6.8	8.5	mA
Supply Current when Disabled (AD8063 Only)			0.4		mA
Power Supply Rejection Ratio			80		dB

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 8 V
Internal Power Dissipation[2]
Plastic Package (N) . . . . . 1.3 W
Small Outline Package (R) . . . . . 0.8 W
SOT-23-5 Package . . . . . 0.5 W
SOT-23-6 Package . . . . . 0.5 W
μSOIC Package . . . . . 0.6 W
Input Voltage (Common-Mode) ($-V_S$ – 0.2 V) to ($+V_S$ – 1.8 V)
Differential Input Voltage . . . . . $\pm V_S$
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range R, RM, SOT-23-5,
SOT-23-6 . . . . . –65°C to +125°C
Operating Temperature Range . . . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . 300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Lead SOIC Package: θ_{JA} = 160°C/W; θ_{JC} = 56°C/W
5-Lead SOT-23-5 Package: θ_{JA} = 240°C/W; θ_{JC} = 92°C/W
6-Lead SOT-23-6 Package: θ_{JA} = 230°C/W; θ_{JC} = 92°C/W
8-Lead μSOIC Package: θ_{JA} = 200°C/W; θ_{JC} = 44°C/W.

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD806x is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately 150°C. Temporarily exceeding this limit may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of 175°C for an extended period can result in device failure. While the AD806x is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (150°C) is not exceeded under all conditions.

To ensure proper operation, it is necessary to observe the maximum power derating curves.

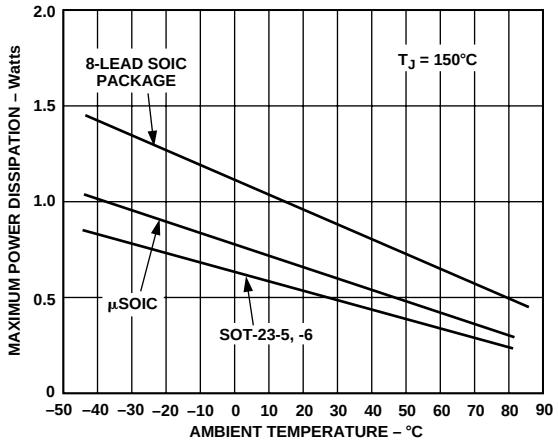


Figure 2. Plot of Maximum Power Dissipation vs. Temperature for AD8061/AD8062/AD8063

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD8061AR	–40°C to +85°C	8-Lead SOIC	R-8
AD8061ART	–40°C to +85°C	5-Lead SOT-23-5	RT-5
AD8062AR	–40°C to +85°C	8-Lead SOIC	R-8
AD8062ARM	–40°C to +85°C	8-Lead μSOIC	RM-8
AD8063AR	–40°C to +85°C	8-Lead SOIC	R-8
AD8063ART	–40°C to +85°C	6-Lead SOT-23-6	RT-6
AD806x-EB		Evaluation Board for AD806xAR	

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8061/AD8062/AD8063 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

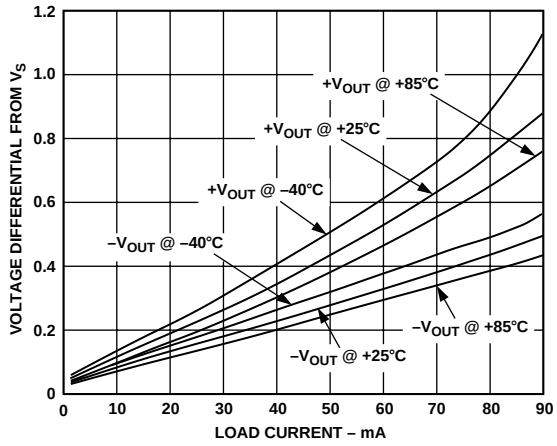


Figure 3. Output Saturation Voltage vs. Load Current

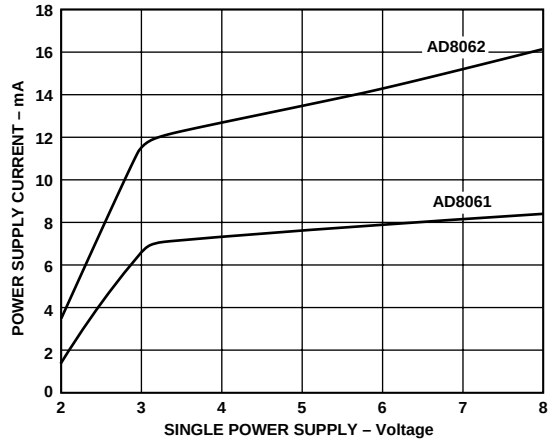


Figure 4. I_{SUPPLY} vs. V_{SUPPLY}

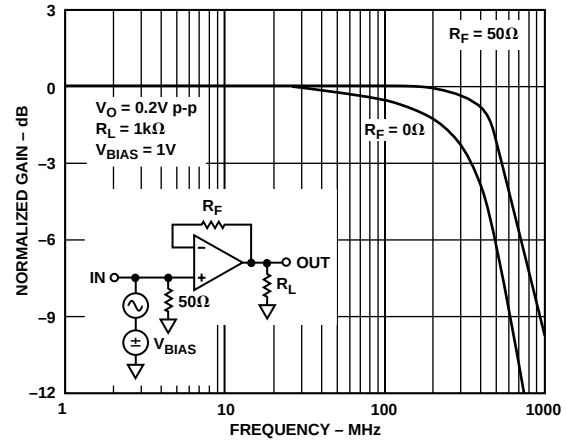


Figure 5. Small Signal Response, R_F = 0 Ω, 50 Ω

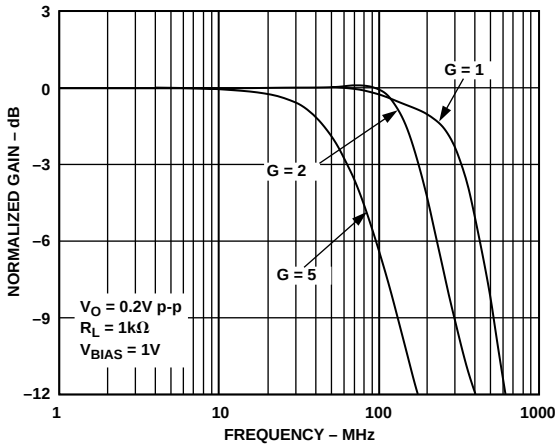


Figure 6. Small Signal Frequency Response

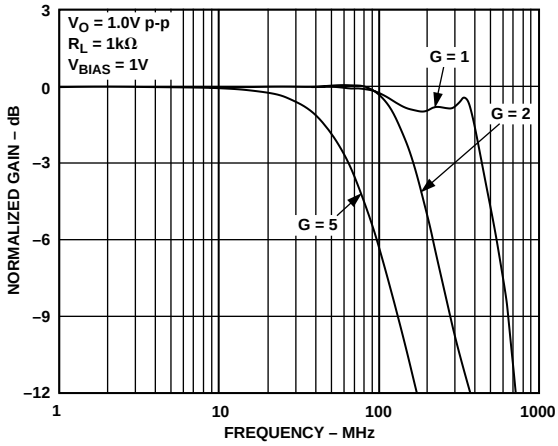


Figure 7. Large Signal Frequency Response

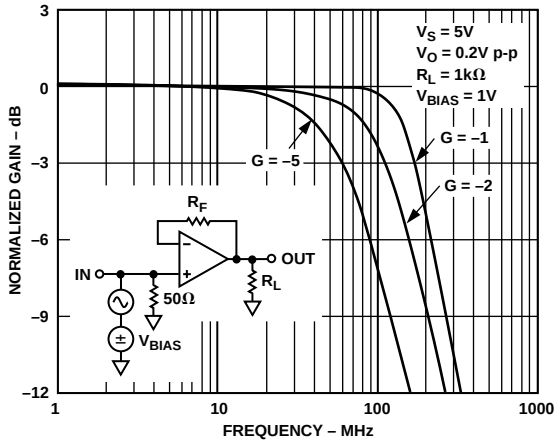


Figure 8. Small Signal Frequency Response

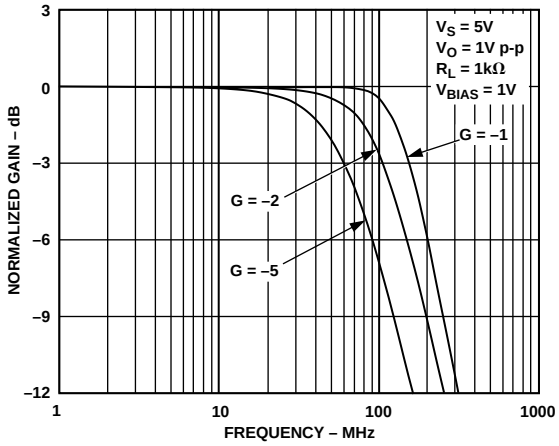


Figure 9. Large Signal Frequency Response

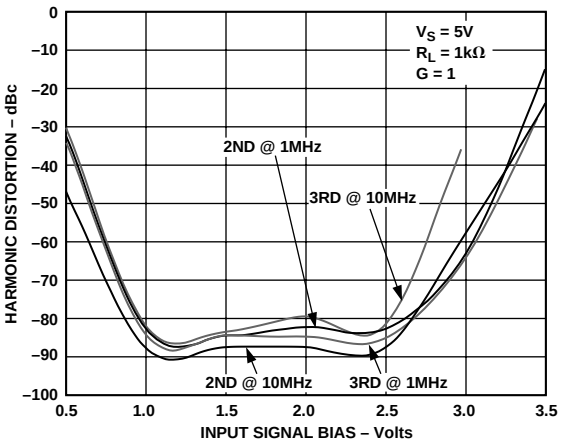


Figure 12. Harmonic Distortion for a 1 V p-p Signal vs. Input Signal DC Bias

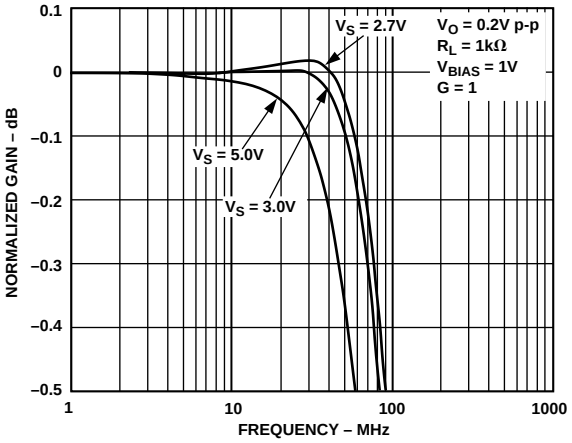


Figure 10. 0.1 dB Flatness

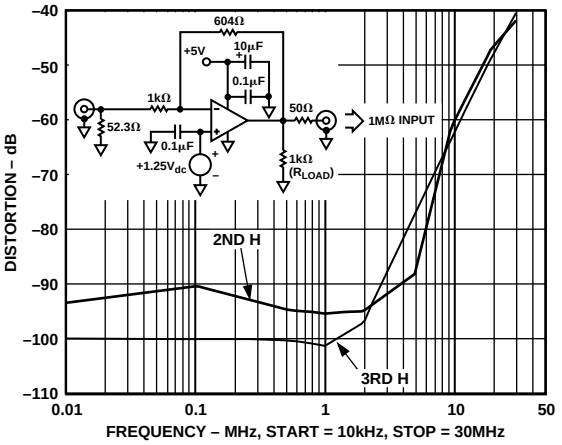


Figure 13. Harmonic Distortion for a 1 V p-p Output Signal vs. Input Signal DC Bias

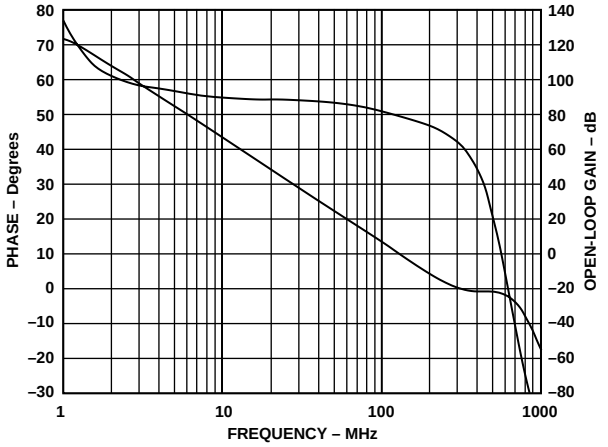


Figure 11. Open-Loop Gain and Phase vs. Frequency, V_S = 5 V, R_L = 1 kΩ

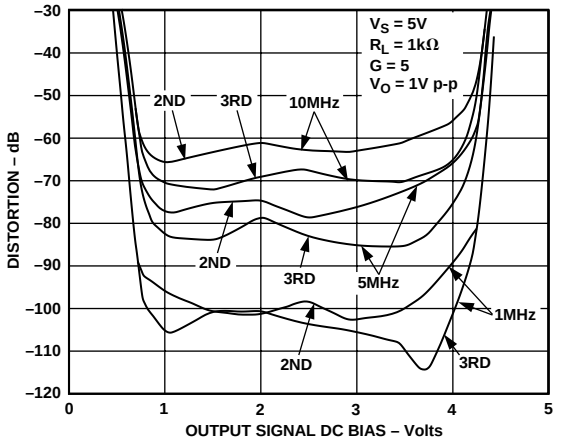


Figure 14. Harmonic Distortion vs. Output Signal DC Bias

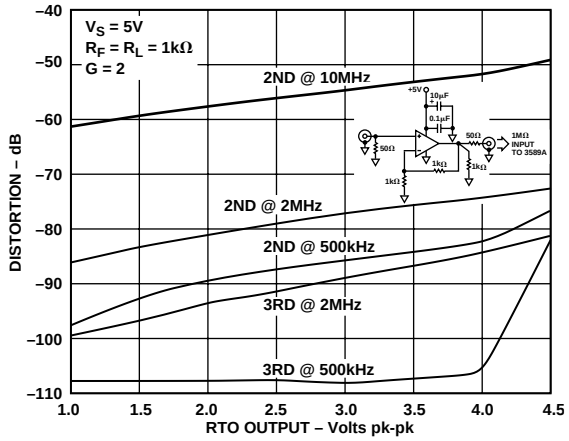


Figure 15. Harmonic Distortion vs. Output Signal Amplitude

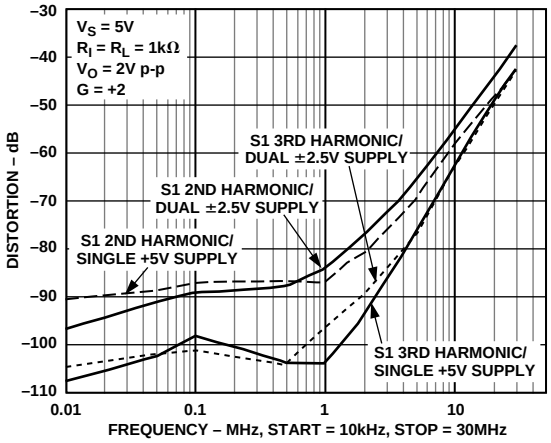


Figure 16. Harmonic Distortion vs. Frequency

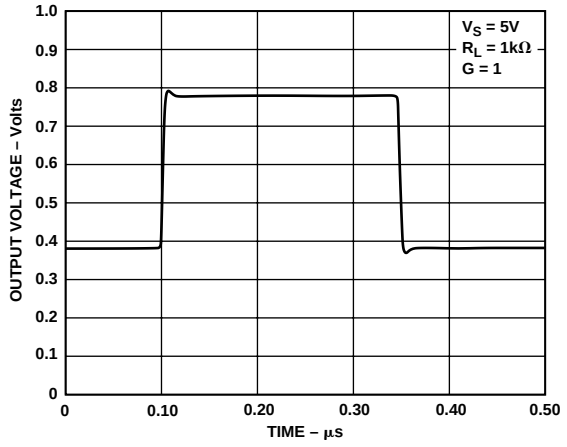


Figure 17. 400 mV Pulse Response

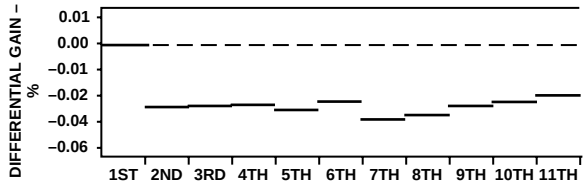


Figure 18. Differential Gain and Phase Error, G = 2, NTSC Input Signal, R_L = 1 kΩ, V_S = 5 V

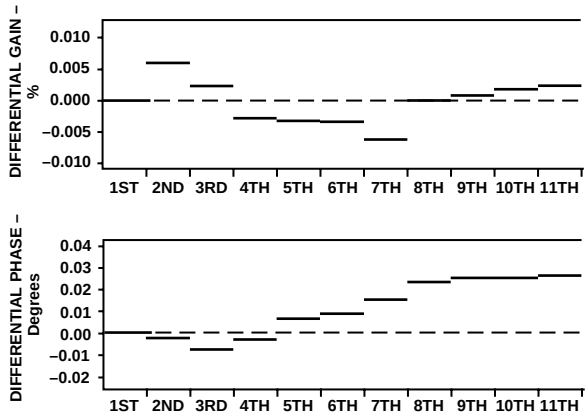


Figure 19. Differential Gain and Phase Error, G = 2, NTSC Input Signal, R_L = 150 Ω, V_S = 5 V

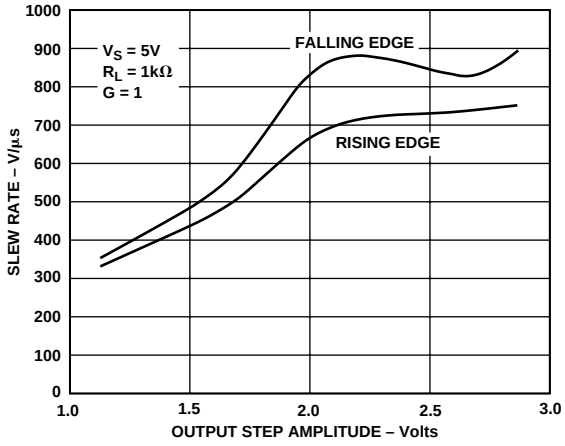


Figure 20. Slew Rate vs. Output Step Amplitude

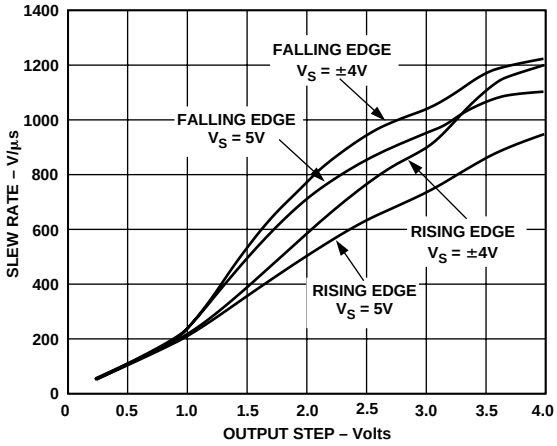


Figure 21. Slew Rate vs. Output Step Amplitude, G = 2, R_L = 1 kΩ, V_S = 5 V

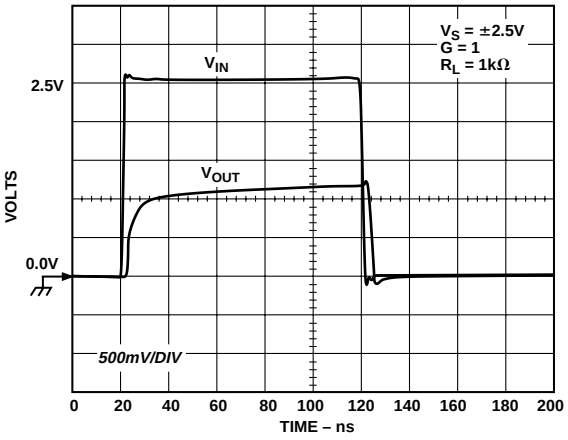


Figure 24. Input Overload Recovery, Input Step = 0 V to 2 V

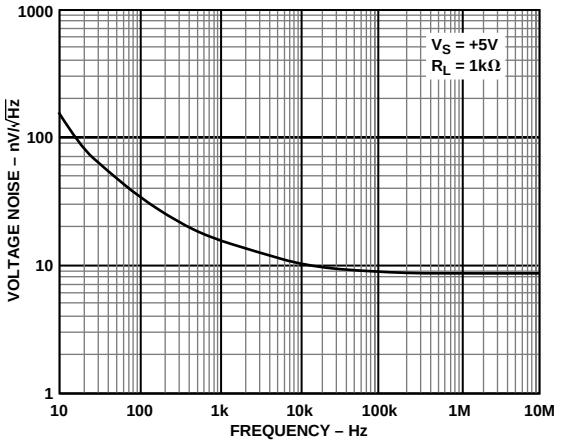


Figure 22. Voltage Noise vs. Frequency

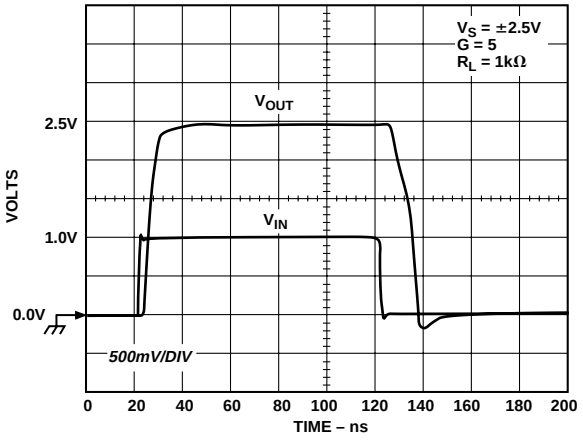


Figure 25. Output Overload Recovery, Input Step = 0 V to 1 V

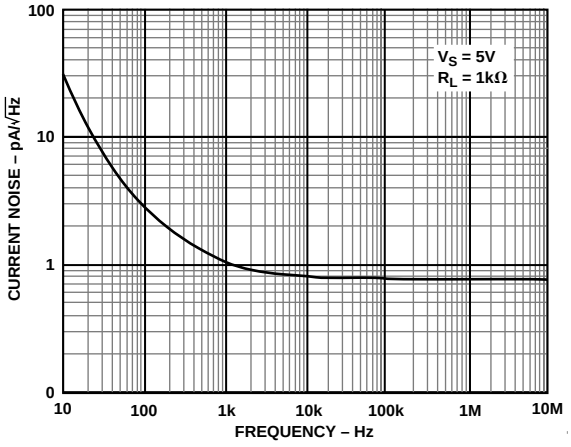


Figure 23. Current Noise vs. Frequency

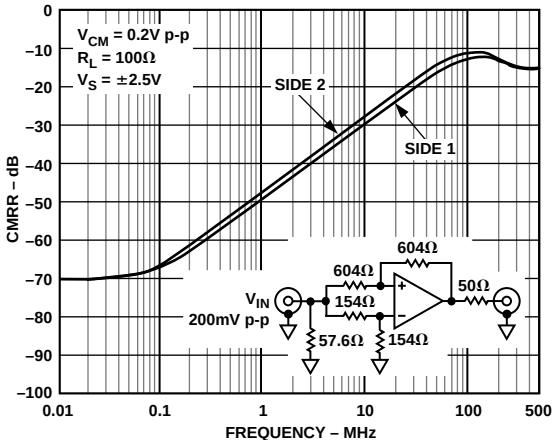


Figure 26. CMRR vs. Frequency

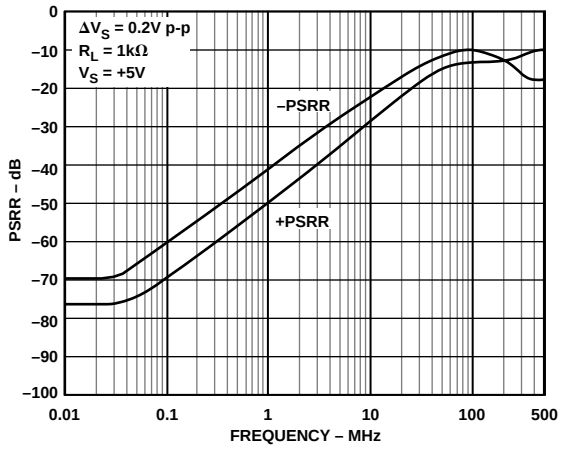


Figure 27. ±PSRR vs. Frequency Delta

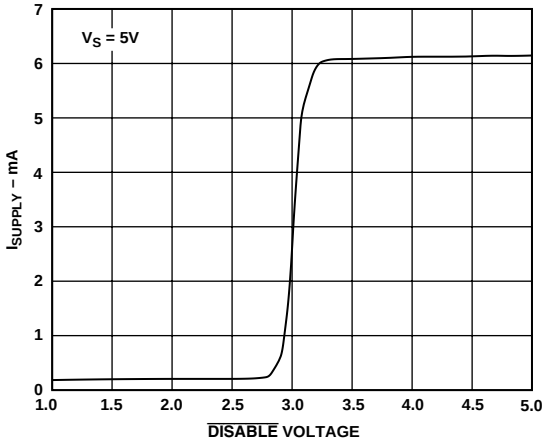


Figure 30. $\overline{DISABLE}$ Voltage vs. Supply Current

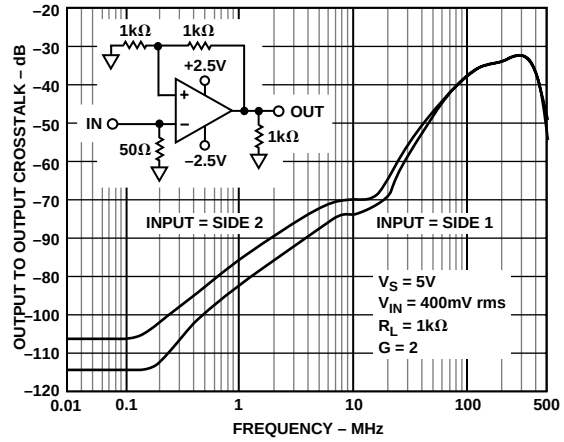


Figure 28. AD8062 Crosstalk, V_{OUT} = 2.0 V p-p, R_L = 1 kΩ, G = 1, V_S = 5 V

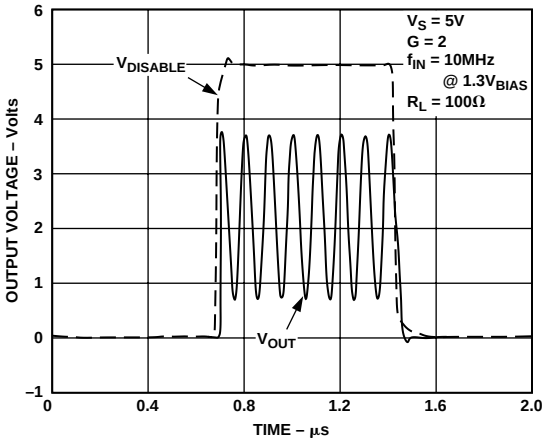


Figure 31. $\overline{DISABLE}$ Function, Voltage = 0 V to 5 V

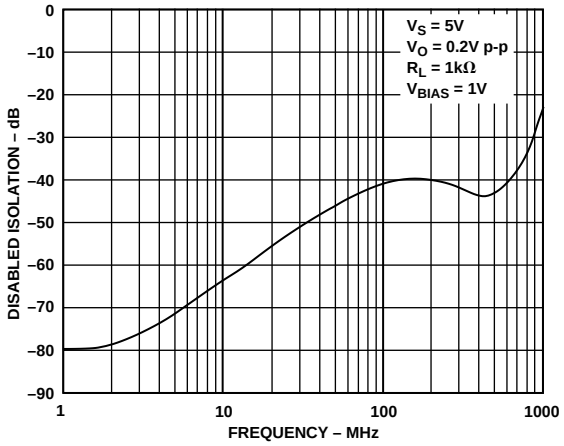


Figure 29. Disabled Output Isolation Frequency Response

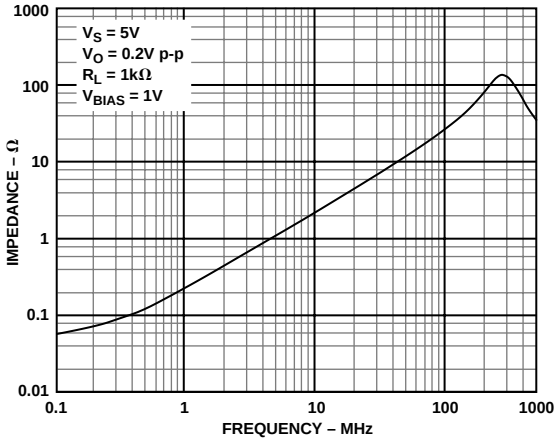


Figure 32. Output Impedance vs. Frequency, V_{OUT} = 0.2 V p-p, R_L = 1 kΩ, V_S = 5 V

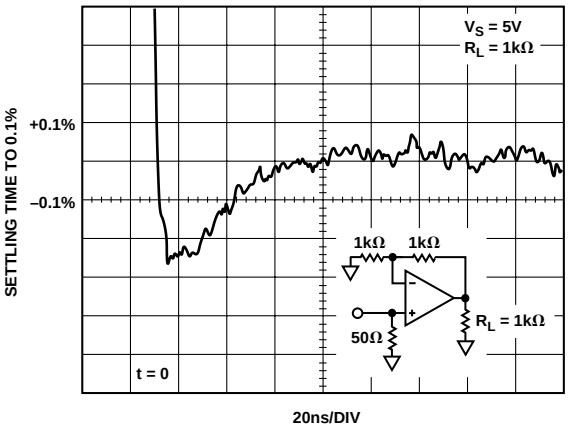


Figure 33. Output Settling Time to 0.1%

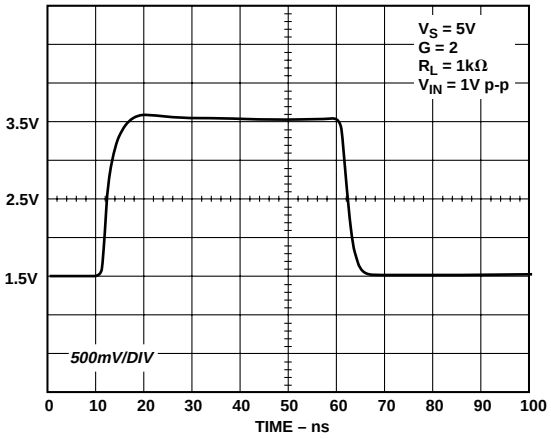


Figure 36. 1 V Step Response

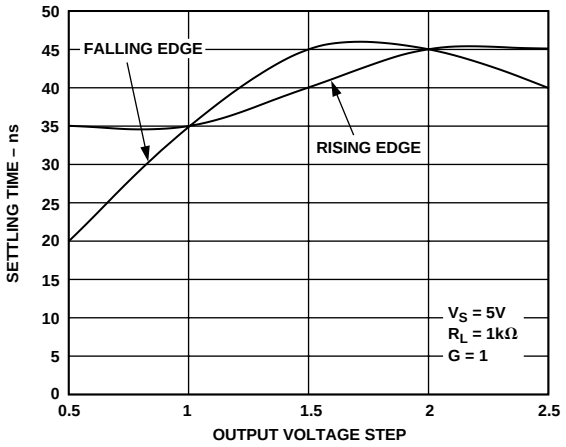


Figure 34. Settling Time vs. V_{OUT}

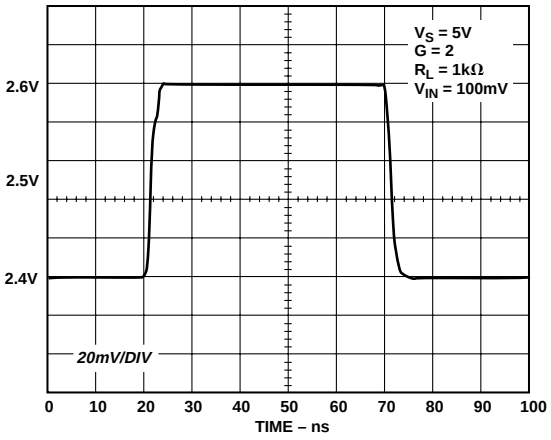


Figure 37. 100 mV Step Response

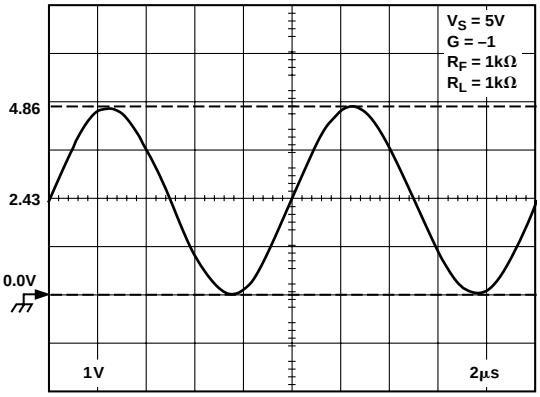


Figure 35. Output Swing

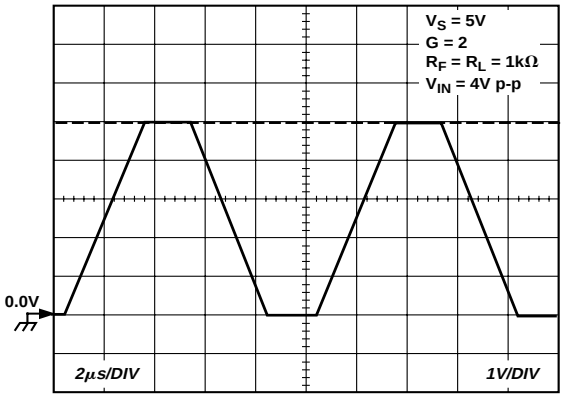


Figure 38. Output Rail-to-Rail Swing

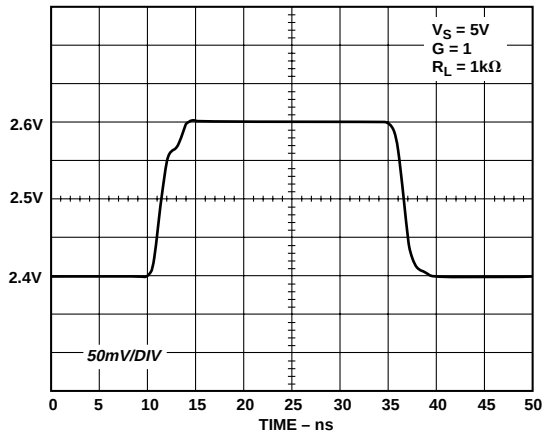


Figure 39. 200 mV Step Response

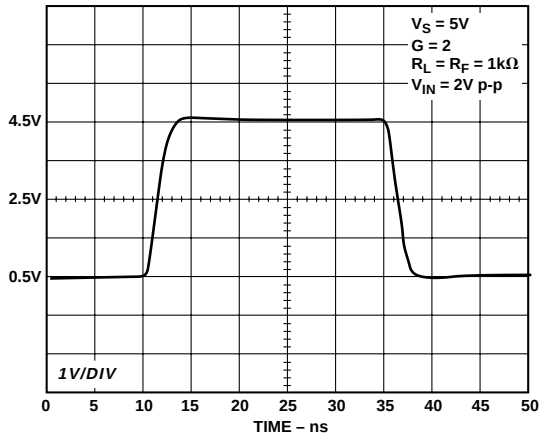


Figure 40. 2 V Step Response

CIRCUIT DESCRIPTION

The AD8061/AD8062/AD8063 family are very high-speed voltage feedback op amps. The high slew rate input stage is a true single-supply topology, capable of sensing signals at or below the minus supply rail. The rail-to-rail output stage can pull within 30 mV of either supply rail when driving light loads and within 0.3 V when driving 150 Ω. High-speed performance is maintained at supply voltages as low as 2.7 V.

Headroom Considerations

These amplifiers are designed for use in low-voltage systems. To obtain optimum performance, it is useful to understand the behavior of the amplifier as input and output signals approach the amplifier's headroom limits.

The AD806x's input common-mode voltage range extends from the negative supply voltage (actually 200 mV below this), or "ground" for single supply operation, to within 1.8 V of the positive supply voltage. Thus, at a gain of 2, the AD806x can provide full "rail-to-rail" output swing for supply voltage as low as 3.6 V, assuming the input signal swing from $-V_S$ (or ground) to $+V_S/2$. At a gain of 3, the AD806x can provide a rail-to-rail output range down to 2.7 V total supply voltage.

Exceeding the headroom limit is not a concern for any inverting gain on any supply voltage, as long as the reference voltage at the amplifier's positive input lies within the amplifier's input common-mode range.

The input stage will be the headroom limit for signals when the amplifier is used in a gain of 1 for signals approaching the positive rail. Figure 41 shows a typical offset voltage versus input common-mode voltage for the AD806x amplifier on a 5 V supply. Accurate dc performance is maintained from about 200 mV below the minus supply to within 1.8 V of the positive supply. For high-speed signals, however, there are other considerations. Figure 42 shows –3 dB bandwidth versus dc input

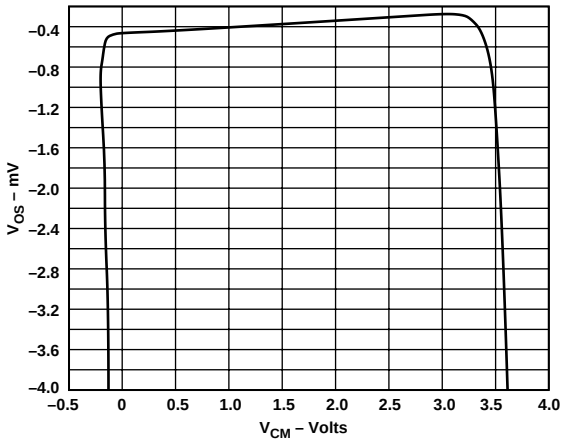


Figure 41. V_{OS} vs. Common-Mode Voltage, V_S = 5 V

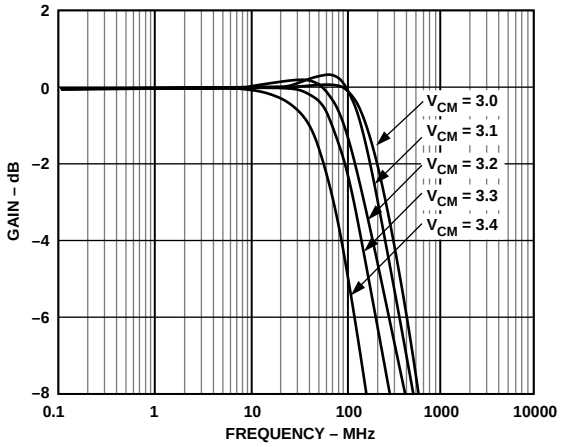


Figure 42. Unity Gain Follower Bandwidth vs. Input Common Mode, V_S = 5 V

voltage for a unity gain follower. As the common-mode voltage approaches the positive supply, the amplifier holds together well, but the bandwidth begins to drop at 1.9 V within $+V_S$.

This can manifest itself in increased distortion or settling time. Figure 12 plots the distortion of a 1 V p-p signal with the AD806x amplifier used as a follower on a 5 V supply versus signal common-mode voltage. Distortion performance is maintained until the input signal center voltage gets beyond 2.5 volts, as the peak of the input sine wave begins to run into the upper common-mode voltage limit. Higher frequency signals require more headroom than the lower frequencies to maintain distortion performance. Figure 43 illustrates how the rising edge settling time for the amplifier configured as a unity gain follower stretches out as the top of a 1 V step input approaches and exceeds the specified input common-mode voltage limit.

For signals approaching the minus supply and inverting gain and high positive gain configurations, the headroom limit will be the output stage. The AD806x amplifiers use a common emitter style output stage. This output stage maximizes the available output range, limited by the saturation voltage of the output transistors. The saturation voltage increases with the drive current the output transistor is required to supply, due to the output transistors' collector resistance. The saturation voltage can be estimated using the equation $V_{SAT} = 25\ mV + I_O \times 8\ \Omega$, where I_O is the output current, and 8 Ω is a typical value for the output transistors' collector resistance.

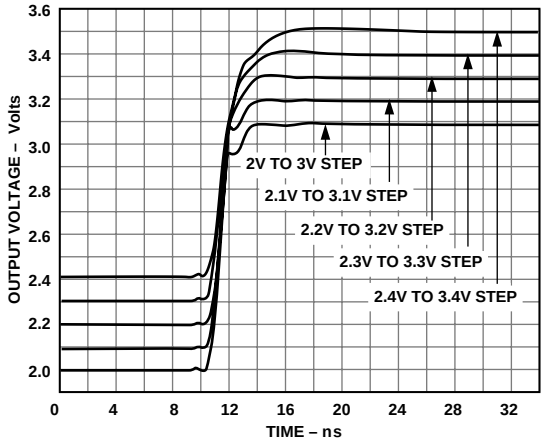


Figure 43. Output Rising Edge for 1 V Step at Input Headroom Limits, G = 1, V_S = 5 V, 0 V

As the saturation point of the output stage is approached, the output signal will show increasing amounts of compression and clipping. As in the input headroom case, the higher frequency signals require a bit more headroom than the lower frequency signals. Figures 13, 14, and 15 illustrate the point, plotting typical distortion versus output amplitude and bias for gains of 2 and 5.

Overload Behavior and Recovery

Input

The specified input common-mode voltage of the AD806x is –200 mV below the negative supply to within 1.8 V of the positive supply. Exceeding the top limit results in lower bandwidth and increased settling time as seen in the previous Figures 42 and 43. Pushing the input voltage of a unity gain follower beyond 1.6 V within the positive supply leads to the behavior shown in Figure 44—an increasing amount of output error as well as much increased settling time. Recovery time from input voltages 1.6 V or closer to the positive supply is about 35 ns, which is limited by the settling artifacts caused by transistors in the input stage coming out of saturation.

The AD806x family does not exhibit phase reversal, even for input voltages beyond the voltage supply rails. Going more than 0.6 V beyond the power supplies will turn on protection diodes at the input stage which will greatly increase the device's current draw.

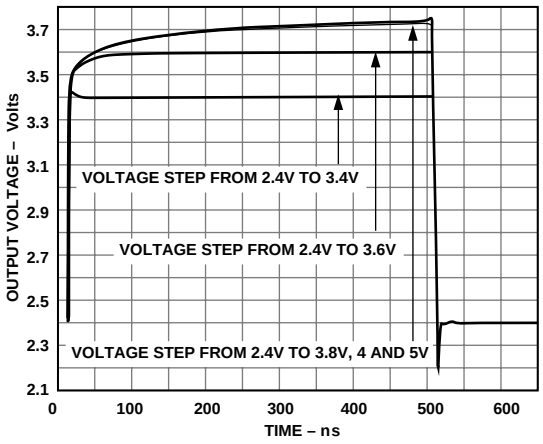


Figure 44. Pulse Response for G = 1 Follower, Input Step Overloading the Input Stage

Output

Output overload recovery is typically within 40 ns after the amplifier's input is brought to a nonoverloading value. Figure 45 shows output recovery transients for the amplifier recovering from a saturated output from the top and bottom supplies to a point at midsupply.

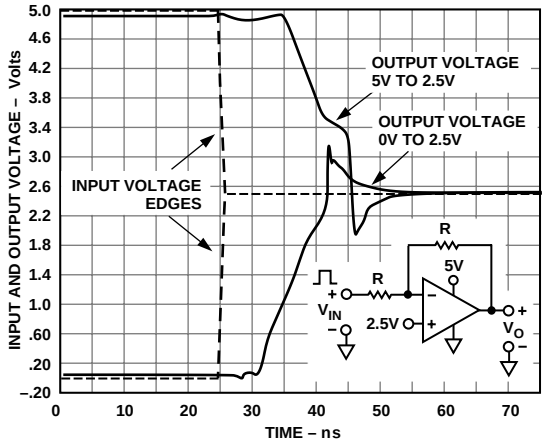


Figure 45. Overload Recovery, G = –1, V_S = 5 V

CAPACITIVE LOAD DRIVE

The AD806x family is optimized for bandwidth and speed, not for driving capacitive loads. Output capacitance will create a pole in the amplifier's feedback path, leading to excessive peaking and potential oscillation. If dealing with load capacitance is a requirement of the application, the two strategies to consider are (1) using a small resistor in series with the amplifier's output and the load capacitance and (2) reducing the bandwidth of the amplifier's feedback loop by increasing the overall noise gain.

Figure 46 shows a unity gain follower using the series resistor strategy. The resistor isolates the output from the capacitance and, more importantly, creates a zero in the feedback path that compensates for the pole created by the output capacitance.

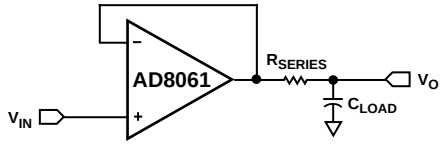


Figure 46. Series Resistor Isolating Capacitive Load

Voltage feedback amplifiers like those in AD806x family will be able to drive more capacitive load without excessive peaking when used in higher gain configurations. This is because the increased noise gain reduces the bandwidth of the overall feedback loop. Figure 47 plots the capacitance that produces 30% overshoot versus noise gain for a typical amplifier.

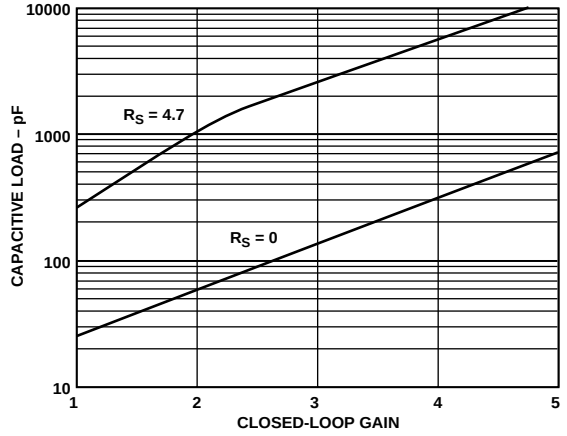


Figure 47. Capacitive Load vs. Closed-Loop Gain

DISABLE OPERATION

The internal circuit for the AD8063 disable function is shown in Figure 48. When the $\overline{\text{DISABLE}}$ node is pulled below 2 V from the positive supply, the supply current will decrease from typically 6.5 mA to under 400 μA, and the AD8063 output will enter a high impedance state. If the $\overline{\text{DISABLE}}$ node is not connected, and thus is allowed to float, the AD8063 will stay biased at full power.

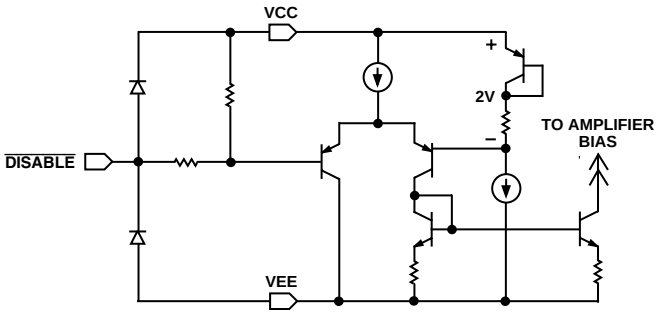


Figure 48. Disable Circuit of the AD8063

Figure 30 shows AD8063 supply current versus $\overline{\text{DISABLE}}$ voltage. Figure 31 plots the output seen when the AD8063 input is driven with a 10 MHz sine wave, and the $\overline{\text{DISABLE}}$ is toggled from 0 to +5 V, illustrating the part's turn on and turn off time. Figure 29 shows the input/output isolation response with the AD8063 shut off.

BOARD LAYOUT CONSIDERATIONS

Maintaining the high speed performance of the AD806x family requires the use of high speed board layout techniques and low parasitic components.

The PCB should have a ground plane covering unused portions of the component side of the board to provide a low impedance path. The ground plane should be removed near the package to reduce parasitic capacitance.

Proper bypassing is critical. A ceramic 0.1 μF chip capacitor should be used to bypass both supplies, and be located within 3 mm of each power pin. An additional 4.7 μF to 10 μF tantalum electrolytic capacitor should be connected in parallel to provide charge for fast, large signal changes at the output.

Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be located close to the inverting input pin. The value of the feedback resistor may come into play—for instance, 1 kΩ interacting with 1 pF of parasitic capacitance creates a pole at 159 MHz.

Stripline design techniques should be used for signal traces longer than 25 mm. These should be designed with either 50 Ω or 75 Ω characteristic impedance, and be properly terminated at each end.

APPLICATIONS

Single Supply Sync Stripper

When a video signal contains synchronization pulses, it is sometimes desirable to remove them prior to performing certain operations. In the case of A-to-D conversion, the sync pulses will consume some of the dynamic range, so removing them will increase the converter's available dynamic range for the video information.

Figure 49 shows a basic circuit for creating a sync stripper using the AD8061 powered by a single supply. When the negative supply is at ground potential, the lowest potential to which the output can go is ground. This feature is exploited to create a waveform whose lowest amplitude is the black level of the video and does not include the sync level.

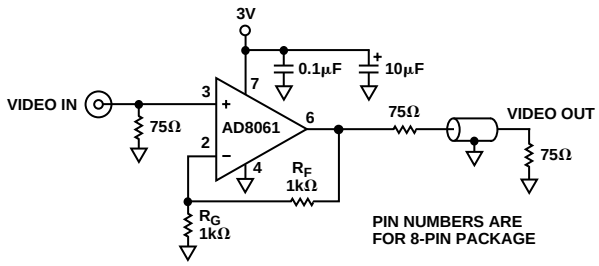


Figure 49. Single 3 V Sync Stripper Using AD8061

In this case, the input video signal has its black level at ground, so it comes out at ground at the input. Since the sync level is below the black level, it will not show up at the output. However, all of the active video portion of the waveform will be amplified by a gain of two and then be normalized to unity gain by the back-terminated transmission line. Figure 50 is an oscilloscope plot of the input and output waveforms.

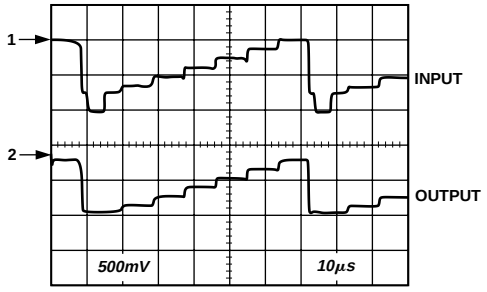


Figure 50. Input and Output Waveforms for a Single Supply Video Sync Stripper Using an AD8061

Some video signals with sync are derived from single supply devices, such as video DACs. These signals can contain sync, but the whole waveform is positive, and the black level is not at ground but at some positive voltage. The circuit can be modified to provide the sync stripping function for such a waveform. Instead of connecting RG to ground, it should be connected to a dc voltage that is two times the black-level of the input signal. The gain from the +input to the output is two, which means that the black level will be amplified by two to the output. However, the gain through RG is –unity to the output. It will take a dc level of twice the input black level to shift the black level to ground at the output. When this occurs, the sync will be stripped, and the active video will be passed as in the ground referenced case.

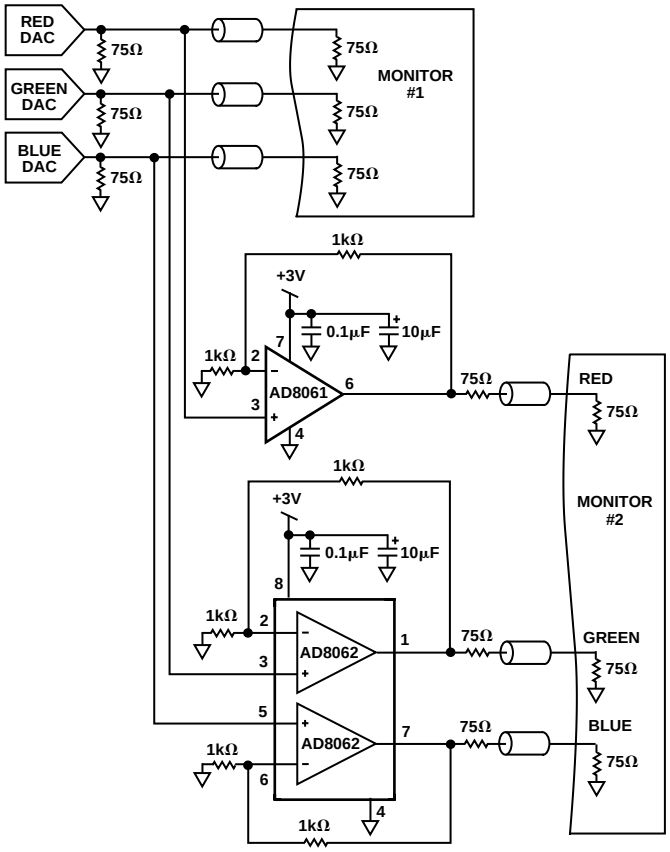


Figure 51. RGB Cable Driver Using AD8061 and AD8062

RGB Amplifier

Most RGB graphics signals are created by video-DAC outputs that drive a current through a resistor to ground. At the video black-level, the current goes to zero and thus the voltage of the video is also zero. Before the availability of high speed rail-to-rail op amps, it was essential that an amplifier have a negative supply to amplify such a signal. Such an amplifier is necessary if one wants to drive a second monitor with from the same DAC outputs.

However, high speed, rail-to-rail output amplifiers like the AD8061 and AD8062 can accept ground level input signals and output ground level signals, and thus be used as RGB signal amplifiers. A combination of the AD8061 (single) and AD8062 (dual) can amplify the three video channels of an RGB system. Figure 51 shows a circuit that performs this function.

Multiplexer

The AD8063 has a disable pin that can be used to power-down the amplifier to save power, or can be used to create a mux circuit. If two (or more) AD8063 outputs are connected together and only one is enabled, then only the signal of the enabled amplifier will appear at the output. This configuration can be used to select from various input-signal sources. Additionally, the same input signal can be applied to different gain stages or differently tuned filters to make a gain-step amplifier or a selectable-frequency amplifier.

Figure 52 shows a schematic of two AD8063s used to create a mux that selects between two inputs. One of these is a 1 V p-p, 3 MHz sine wave and the other is a 2 V p-p, 1 MHz sine wave.

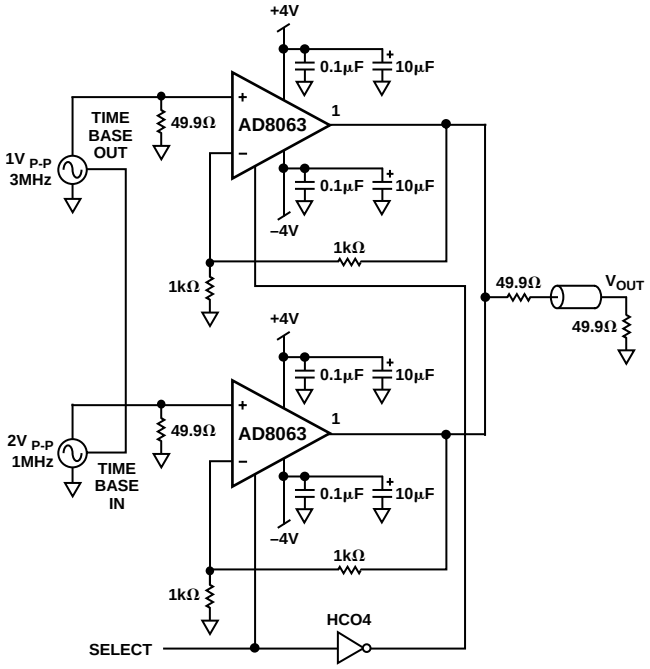


Figure 52. Two-to-One Multiplexer Using Two AD8063s

The SELECT signal and the output waveforms for this circuit are shown in Figure 53. For synchronization clarity, two different frequency synthesizers whose time bases are locked to each other generate the signals.

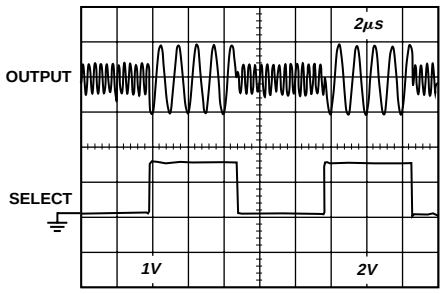


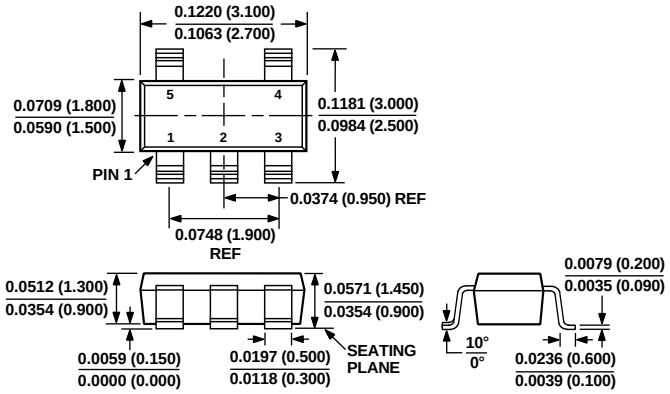
Figure 53. AD8063 Mux Output

C3702–0–2/00 (rev. A)

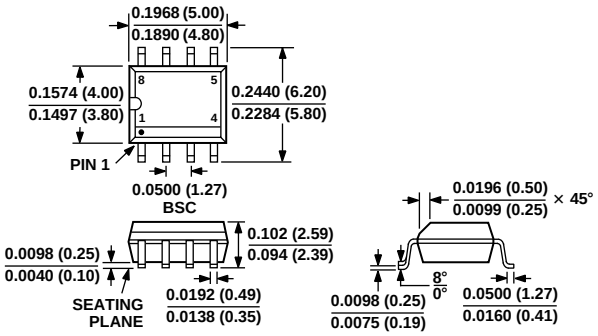
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

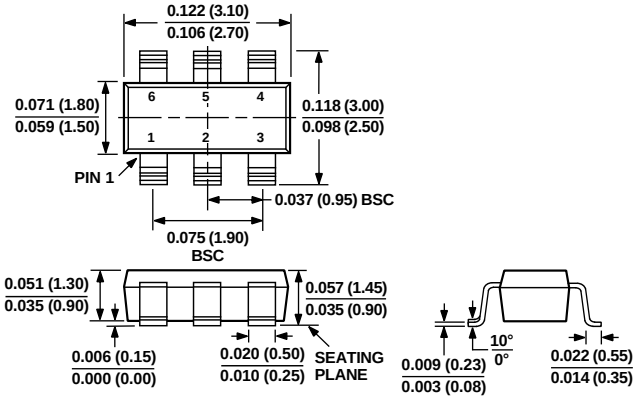
5-Lead SOT-23-5 (RT-5)



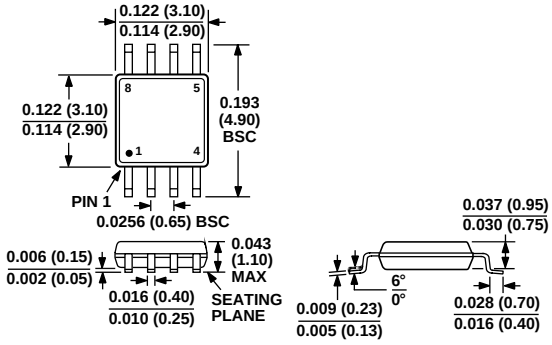
8-Lead SOIC (R-8)



6-Lead SOT-23-6 (RT-6)



8-Lead μSOIC (RM-8)



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