Precision CMOS Single Supply Rail-to-Rail Input/Output Wideband Operational Amplifiers

AD8601/AD8602

FEATURES
Low Offset Voltage: 500 μV Max
Single Supply Operation: 2.7 V to 6 V
Low Supply Current: 750 μA/Amplifier
Wide Bandwidth: 8 MHz
Slew Rate: 5 V/μs
Low Distortion
No Phase Reversal
Low Input Currents
Unity Gain Stable

APPLICATIONS
Barcode Scanners
Battery-Powered Instrumentation
Multipole Filters
Sensors
Current Sensing
ASIC Input or Output Amplifier
Audio

GENERAL DESCRIPTION

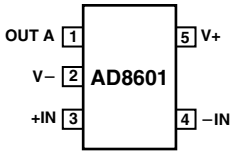
The AD8601 and AD8602 are single and dual rail-to-rail input and output single supply amplifiers featuring very low offset voltage and wide signal bandwidth. These amplifiers use a new, patented trimming technique that achieves superior performance without laser trimming. All are fully specified to operate from 3 V to 5 V single supply.

The combination of low offsets, very low input bias currents, and high speed make these amplifiers useful in a wide variety of applications. Filters, integrators, diode amplifiers, shunt current sensors, and high impedance sensors all benefit from the combination of performance features. Audio and other ac applications benefit from the wide bandwidth and low distortion. For the most cost-sensitive applications the D grades offer this ac performance with lower dc precision at a lower price point.

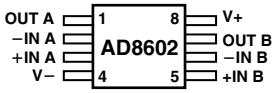
Applications for these amplifiers include audio amplification for portable devices, portable phone headsets, bar code scanners, portable instruments, and multipole filters.

FUNCTIONAL BLOCK DIAGRAMS

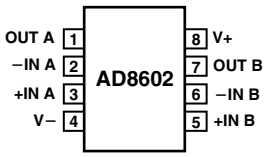
5-Lead SOT-23
(RT Suffix)



8-Lead μSOIC
(RM Suffix)



8-Lead SOIC
(R Suffix)



The ability to swing rail-to-rail at both the input and output enables designers to buffer CMOS ADCs, DACs, ASICs, and other wide output swing devices in single supply systems.

The AD8601 and AD8602 are specified over the extended industrial (–40°C to +125°C) temperature range. The AD8601, single, is available in the tiny 5-lead SOT-23 package. The AD8602, dual, is available in 8-lead MSOP and narrow SOIC surface-mount packages.

SOT and μSOIC versions are available in tape and reel only.

REV. 0

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AD8601/AD8602–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (V_S = 3 V, V_{CM} = V_S/2, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	A Grade Min	A Grade Typ	A Grade Max	D Grade Min	D Grade Typ	D Grade Max	Unit
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	0 V ≤ V_{CM} ≤ 1.3 V		80	500			6,000	µV
		–40°C ≤ T_A ≤ +85°C			700			7,000	µV
		–40°C ≤ T_A ≤ +125°C			1,100			7,000	µV
		0 V ≤ V_{CM} ≤ 3 V[1]		350	750			6,000	µV
		–40°C ≤ T_A ≤ +85°C			1,800			7,000	µV
		–40°C ≤ T_A ≤ +125°C			2,100			7,000	µV
Input Bias Current	I_B			0.2	60		0.2	200	pA
		–40°C ≤ T_A ≤ +85°C			100			200	pA
		–40°C ≤ T_A ≤ +125°C			1,000			1,000	pA
Input Offset Current	I_{OS}			0.1	30		0.1	100	pA
		–40°C ≤ T_A ≤ +85°C			50			100	pA
		–40°C ≤ T_A ≤ +125°C			500			500	pA
Input Voltage Range			0		3	0		3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 3 V	68	83		52	65		dB
Large Signal Voltage Gain	A_{VO}	V_O = 0.5 V to 2.5 V							
		R_L = 2 kΩ , V_{CM} = 0 V	30	100		20	60		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2			2		µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage High	V_{OH}	I_L = 1.0 mA	2.92	2.96		2.92	2.96		V
		–40°C ≤ T_A ≤ +125°C	2.88			2.88			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA		20	35		20	35	mV
		–40°C ≤ T_A ≤ +125°C			50			50	mV
Output Current	I_{OUT}			±30			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		12			12		Ω
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	67	80		56	72		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		680	1,000		680	1,000	µA
		–40°C ≤ T_A ≤ +125°C			1,300			1,300	µA
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		5.2			5.2		V/µs
Settling Time	t_S	To 0.01%		<0.5			<0.5		µs
Gain Bandwidth Product	GBP			8.2			8.2		MHz
Phase Margin	Φo			50			50		Degrees
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		33			33		nV/√Hz
	e_n	f = 10 kHz		18			18		nV/√Hz
Current Noise Density	i_n			0.05			0.05		pA/√Hz

NOTES

[1]For V_{CM} between 1.3 V and 1.8 V, V_{OS} may exceed specified value.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (V_S = 5.0 V, V_{CM} = V_S/2, T_A = 25°C unless otherwise noted)

Parameter	Symbol	Conditions	A Grade Min	A Grade Typ	A Grade Max	D Grade Min	D Grade Typ	D Grade Max	Unit
INPUT CHARACTERISTICS									
Offset Voltage	V_{OS}	0 V ≤ V_{CM} ≤ 5 V		80	500			6,000	µV
		–40°C ≤ T_A ≤ +125°C			1,300			7,000	µV
Input Bias Current	I_B			0.2	60		0.2	200	pA
		–40°C ≤ T_A ≤ +85°C			100			200	pA
		–40°C ≤ T_A ≤ +125°C			1,000			1,000	pA
Input Offset Current	I_{OS}			0.1	30		0.1	100	pA
		–40°C ≤ T_A ≤ +85°C			50			100	pA
		–40°C ≤ T_A ≤ +125°C			500			500	pA
Input Voltage Range			0		5	0		5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = 0 V to 5 V	74	89		56	67		dB
Large Signal Voltage Gain	A_{VO}	V_O = 0.5 V to 4.5 V R_L = 2 kΩ, V_{CM} = 0 V	30	100		20	60		V/mV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$			2			2		µV/°C
OUTPUT CHARACTERISTICS									
Output Voltage High	V_{OH}	I_L = 1.0 mA	4.925	4.975		4.925	4.975		V
		I_L = 10 mA	4.7	4.77		4.7	4.77		V
		–40°C ≤ T_A ≤ +125°C	4.6			4.6			V
Output Voltage Low	V_{OL}	I_L = 1.0 mA		15	30		15	30	mV
		I_L = 10 mA		125	175		125	175	mV
		–40°C ≤ T_A ≤ +125°C			250			250	mV
Output Current	I_{OUT}			±50			±50		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 MHz, A_V = 1		10			10		Ω
POWER SUPPLY									
Power Supply Rejection Ratio	PSRR	V_S = 2.7 V to 5.5 V	67	80		56	72		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		750	1,200		750	1,200	µA
		–40°C ≤ T_A ≤ +125°C			1,500			1,500	µA
DYNAMIC PERFORMANCE									
Slew Rate	SR	R_L = 2 kΩ		6			6		V/µs
Settling Time	t_S	To 0.01%		< 1.0			< 1.0		µs
Full Power Bandwidth	BWp	< 1% Distortion		360			360		kHz
Gain Bandwidth Product	GBP			8.4			8.4		MHz
Phase Margin	Φo			55			55		Degrees
NOISE PERFORMANCE									
Voltage Noise Density	e_n	f = 1 kHz		33			33		nV/√Hz
	e_n	f = 10 kHz		18			18		nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.05			0.05		pA/√Hz

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 6 V
Input Voltage . . . . . GND to V_S
Differential Input Voltage . . . . . ±6 V
Storage Temperature Range
R, RM, RT Packages . . . . . –65°C to +150°C
Operating Temperature Range
AD8601/AD8602 . . . . . –40°C to +125°C
Junction Temperature Range
R, RM, RT Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) . . . . . 300°C
ESD . . . . . 2 kV HBM

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}*	θ_{JC}	Unit
5-Lead SOT-23 (RT)	230	92	°C/W
8-Lead SOIC (R)	158	43	°C/W
8-Lead MSOP (RM)	210	45	°C/W

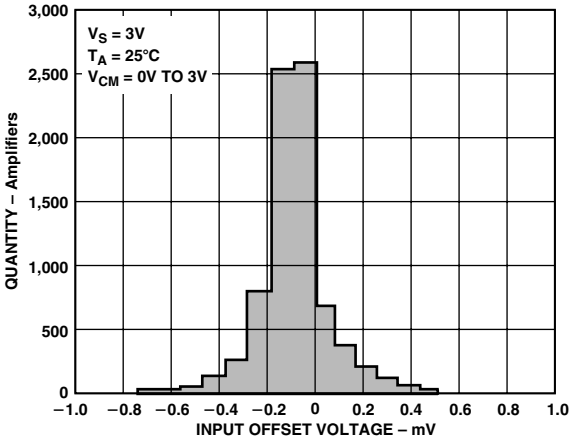
*θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device in socket for PDIP packages; θ_{JA} is specified for device soldered onto a circuit board for surface mount packages.

ORDERING GUIDE

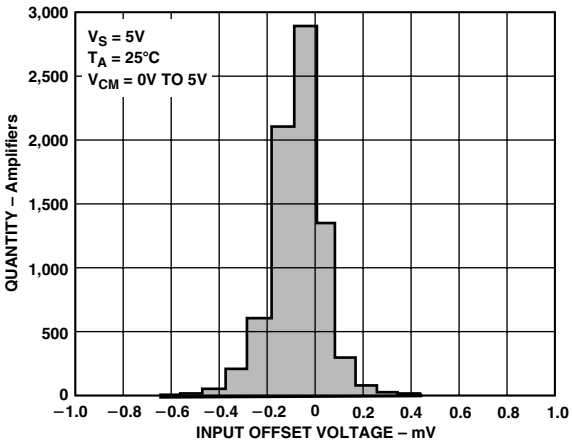
Model	Temperature Range	Package Description	Package Option	Branding Information
AD8601ART	–40°C to +125°C	5-Lead SOT-23	RT-5	AAA
AD8601DRT	–40°C to +125°C	5-Lead SOT-23	RT-5	AAD
AD8602AR	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8602DR	–40°C to +125°C	8-Lead SOIC	SO-8	
AD8602ARM	–40°C to +125°C	8-Lead MSOP	RM-8	ABA
AD8602DRM	–40°C to +125°C	8-Lead MSOP	RM-8	ABD

CAUTION

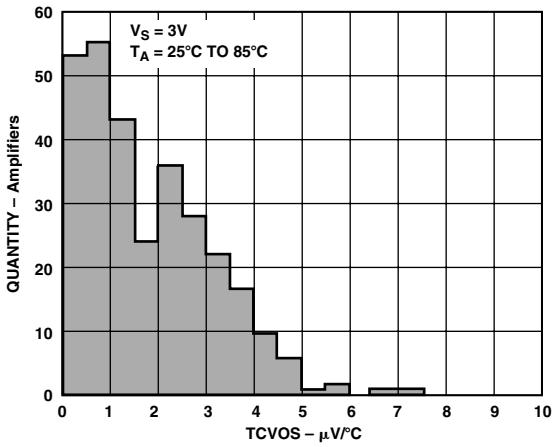
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8601/AD8602 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



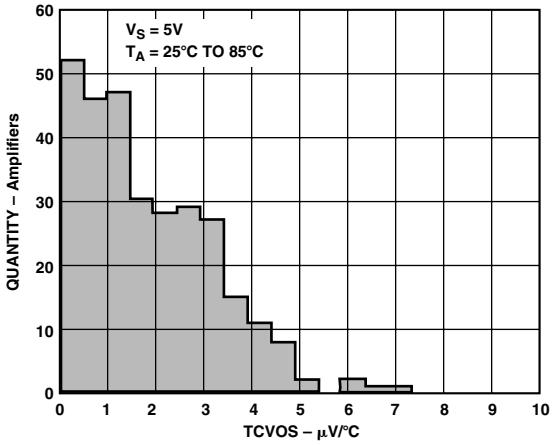
TPC 1. Input Offset Voltage Distribution



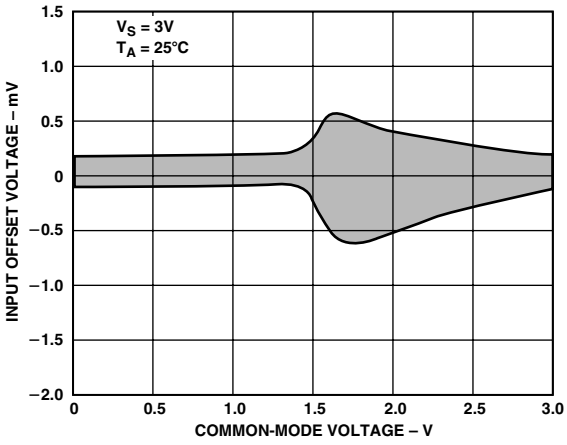
TPC 2. Input Offset Voltage Distribution



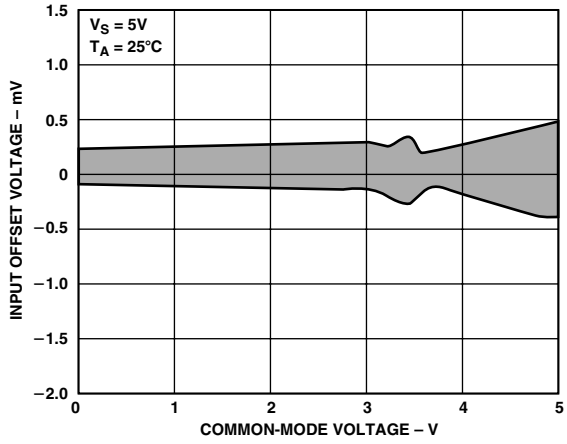
TPC 3. Input Offset Voltage Drift Distribution



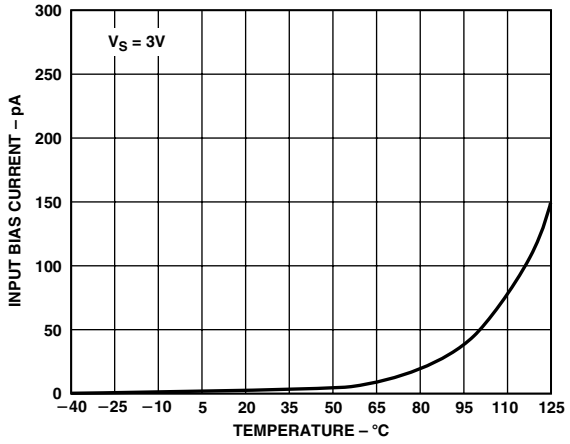
TPC 4. Input Offset Voltage Drift Distribution



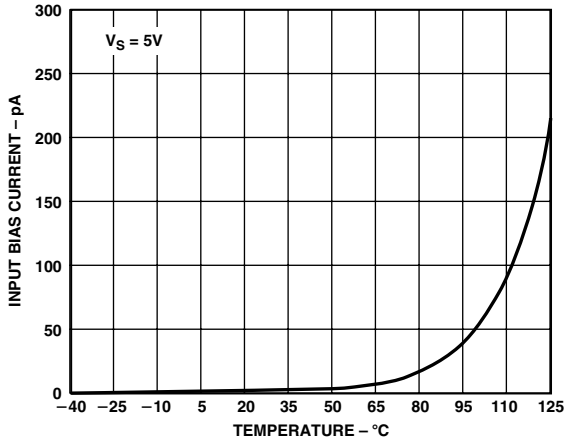
TPC 5. Input Offset Voltage vs. Common-Mode Voltage



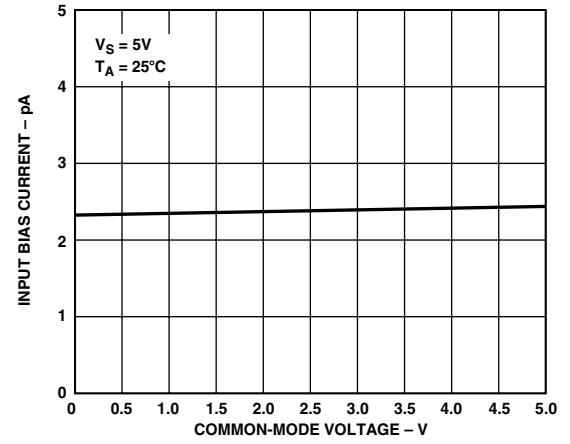
TPC 6. Input Offset Voltage vs. Common-Mode Voltage



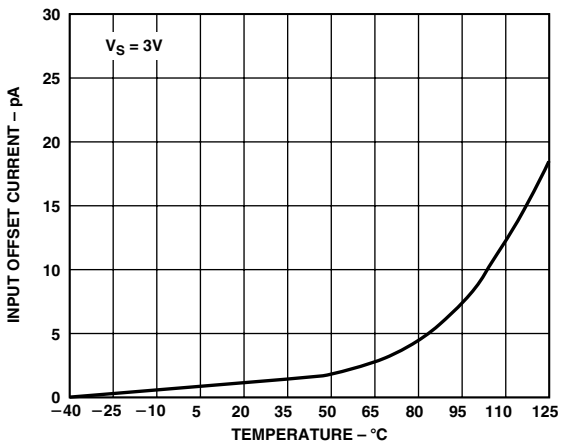
TPC 7. Input Bias Current vs. Temperature



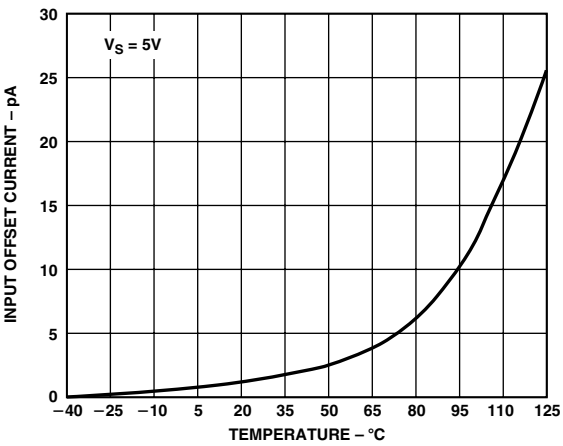
TPC 8. Input Bias Current vs. Temperature



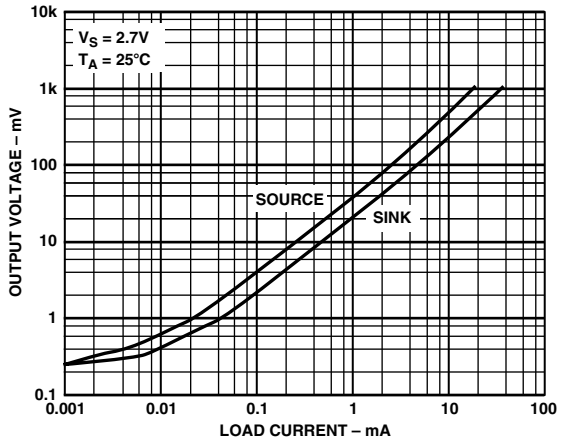
TPC 9. Input Bias Current vs. Common-Mode Voltage



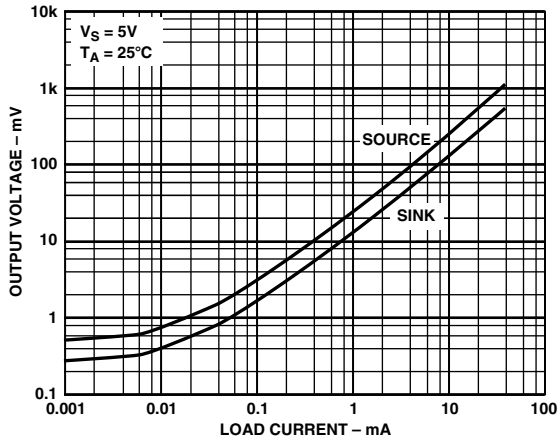
TPC 10. Input Offset Current vs. Temperature



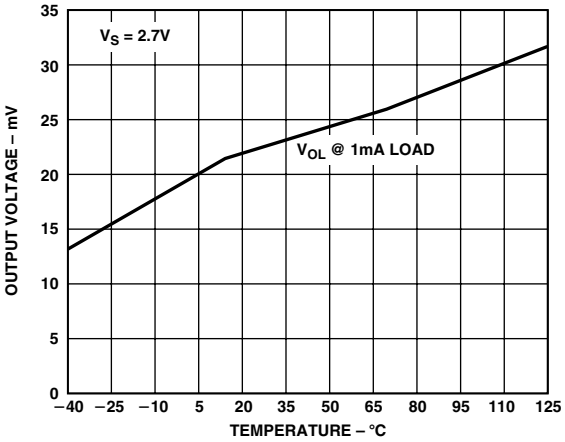
TPC 11. Input Offset Current vs. Temperature



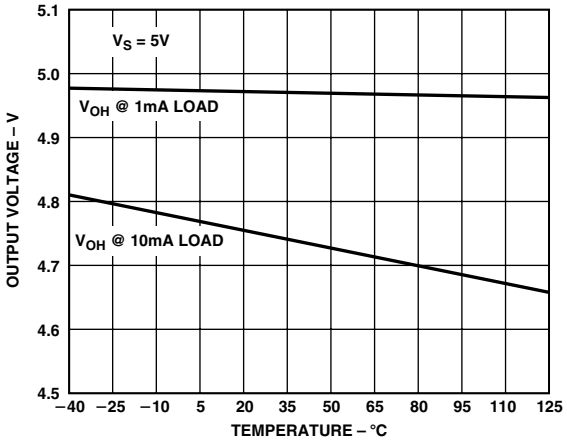
TPC 12. Output Voltage to Supply Rail vs. Load Current



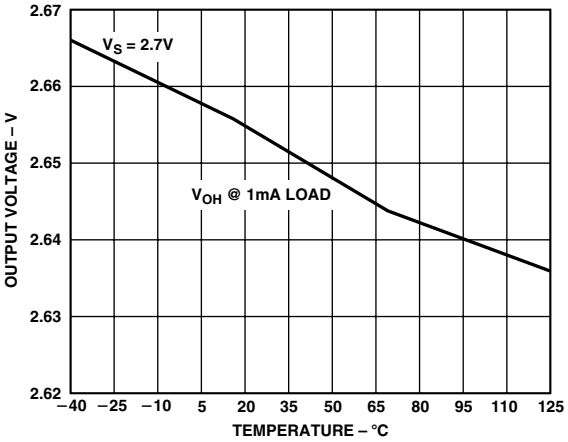
TPC 13. Output Voltage to Supply Rail vs. Load Current



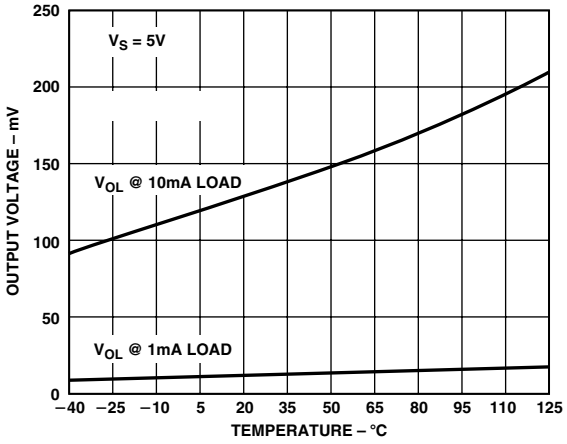
TPC 16. Output Voltage Swing vs. Temperature



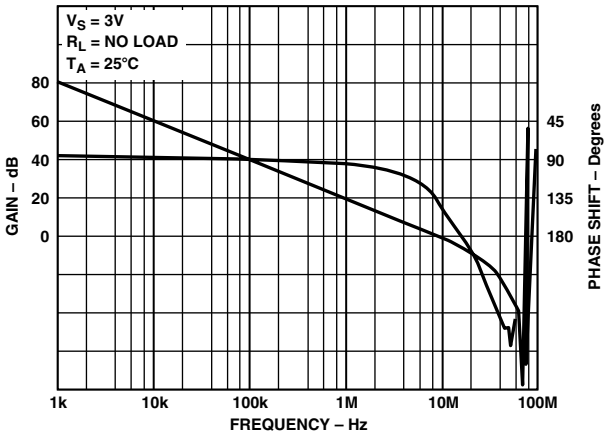
TPC 14. Output Voltage Swing vs. Temperature



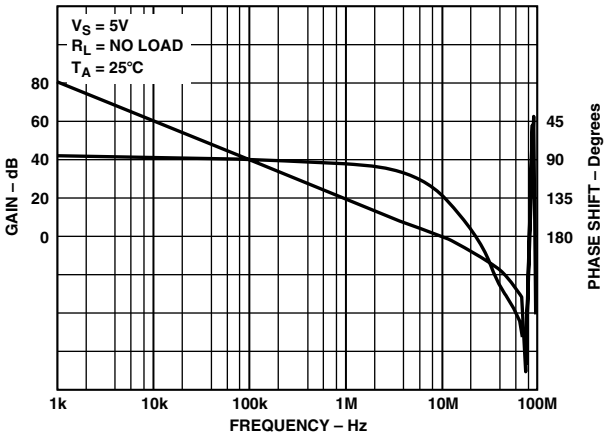
TPC 17. Output Voltage Swing vs. Temperature



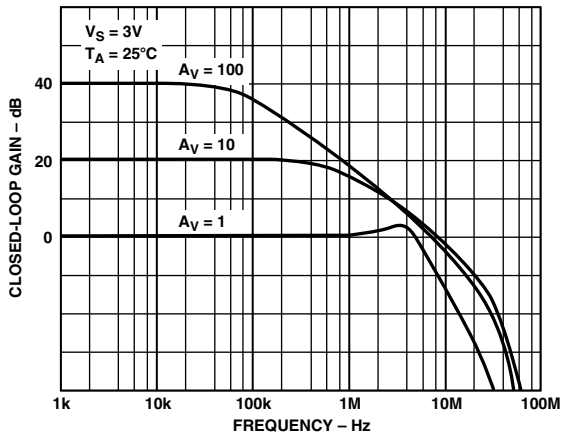
TPC 15. Output Voltage Swing vs. Temperature



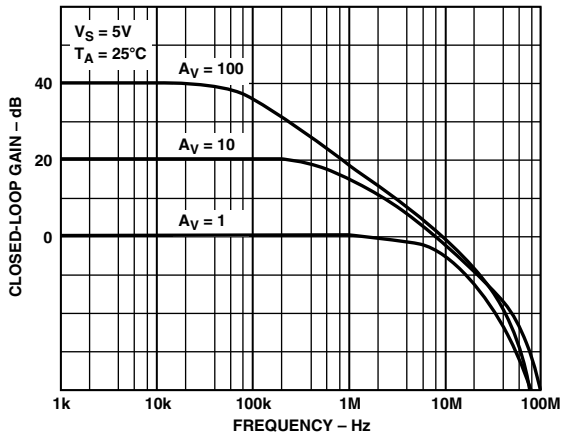
TPC 18. Open-Loop Gain and Phase vs. Frequency



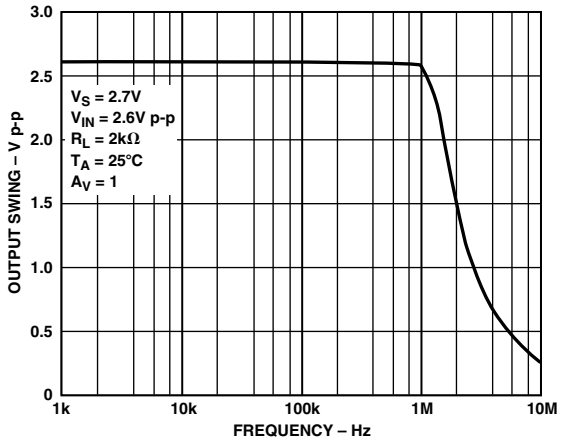
TPC 19. Open-Loop Gain and Phase vs. Frequency



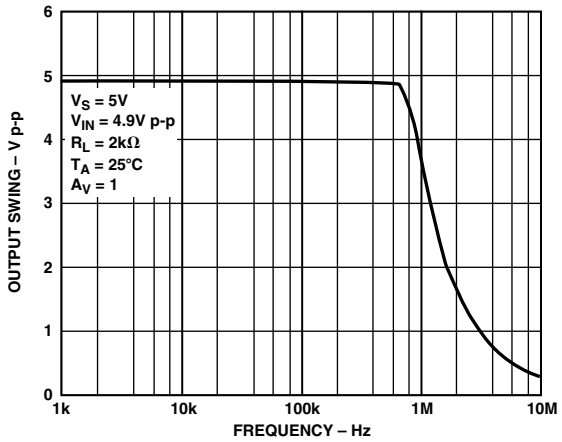
TPC 20. Closed-Loop Gain vs. Frequency



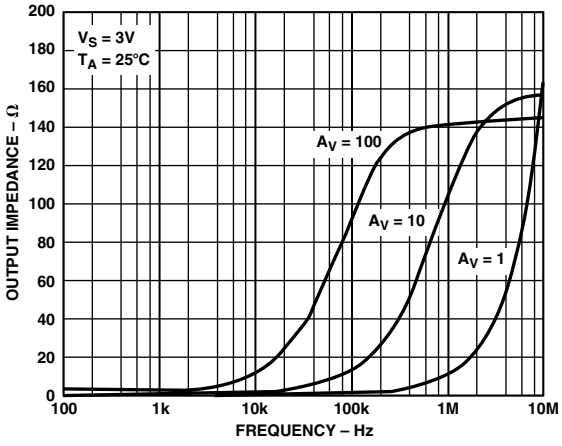
TPC 21. Closed-Loop Gain vs. Frequency



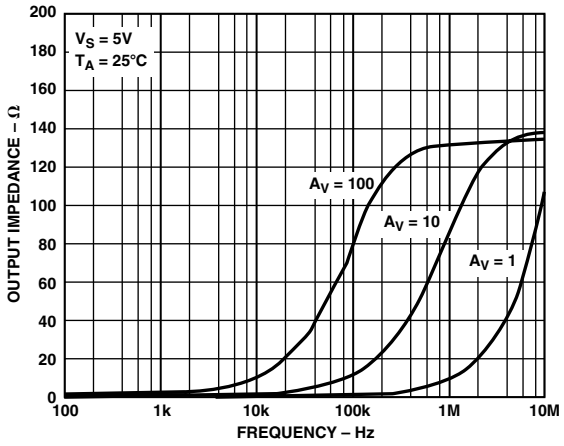
TPC 22. Closed-Loop Output Voltage Swing vs. Frequency



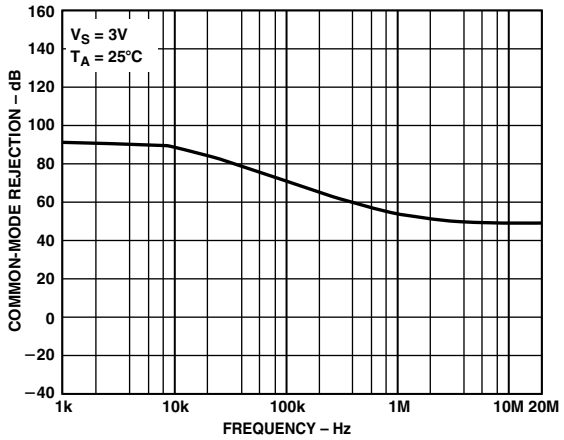
TPC 23. Closed-Loop Output Voltage Swing vs. Frequency



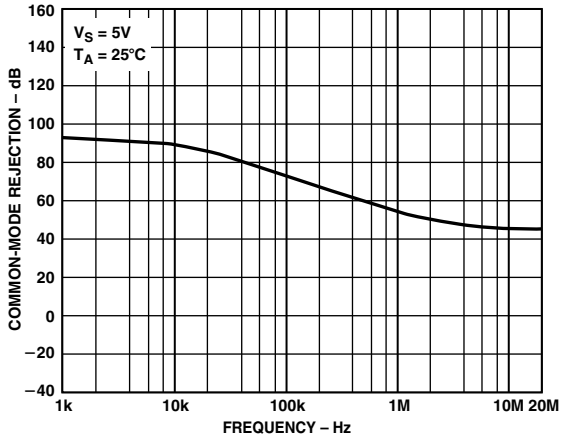
TPC 24. Output Impedance vs. Frequency



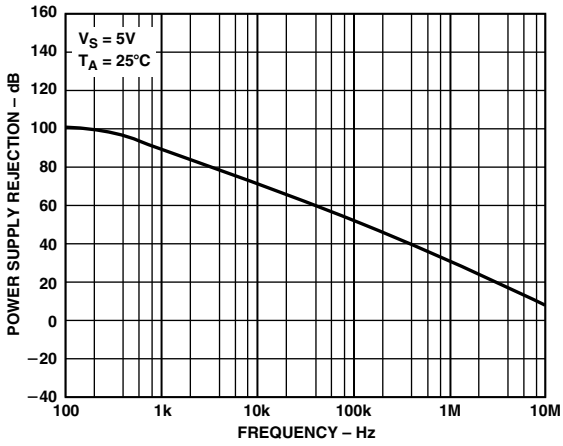
TPC 25. Output Impedance vs. Frequency



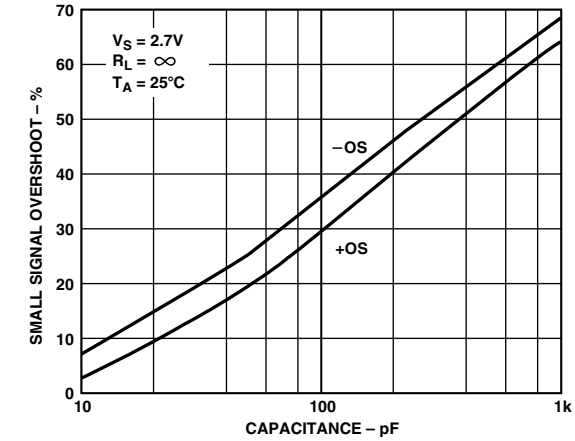
TPC 26. Common-Mode Rejection Ratio vs. Frequency



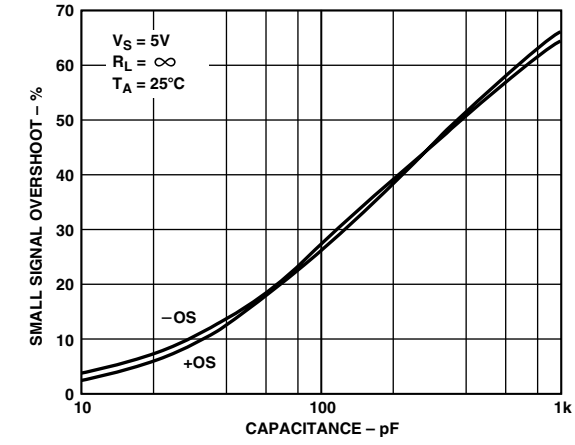
TPC 27. Common-Mode Rejection Ratio vs. Frequency



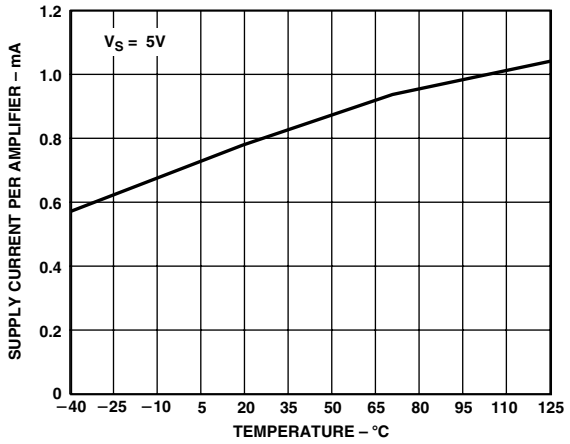
TPC 28. Power Supply Rejection Ratio vs. Frequency



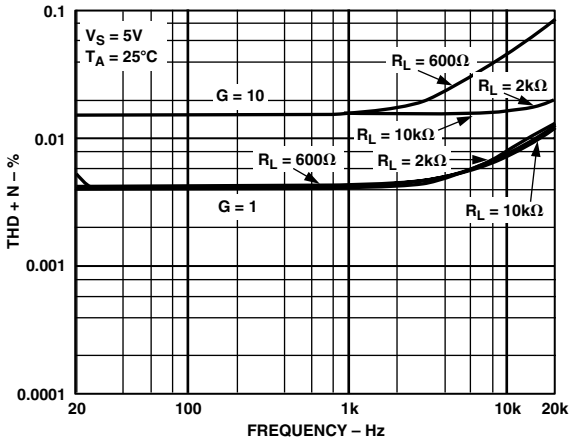
TPC 29. Small Signal Overshoot vs. Load Capacitance



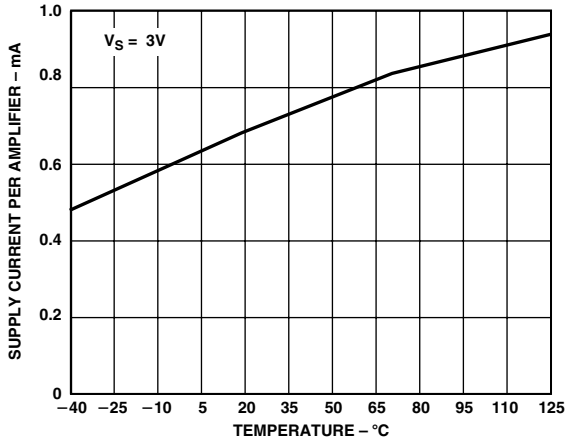
TPC 30. Small Signal Overshoot vs. Load Capacitance



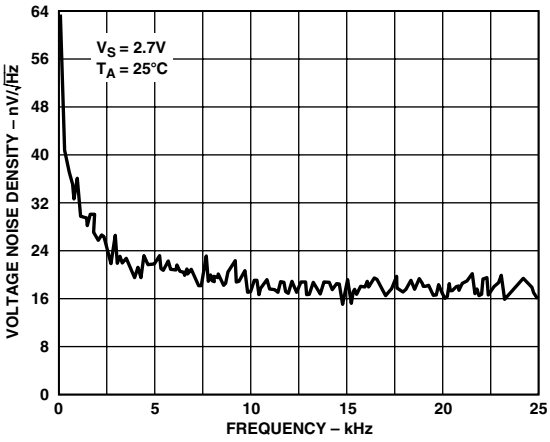
TPC 31. Supply Current per Amplifier vs. Temperature



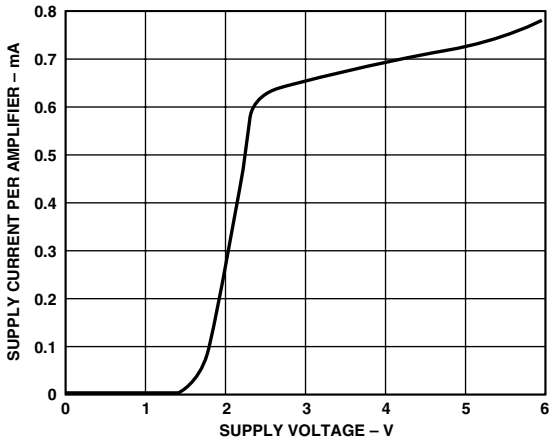
TPC 34. Total Harmonic Distortion + Noise vs. Frequency



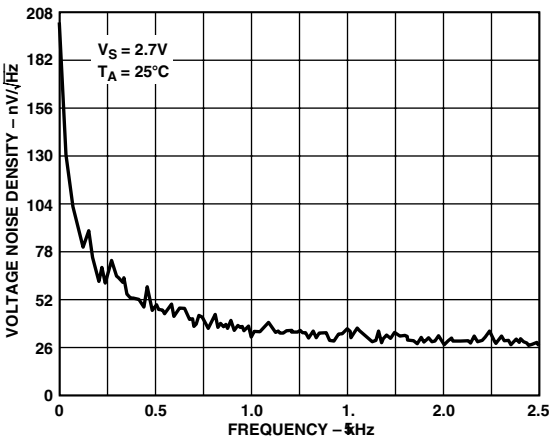
TPC 32. Supply Current per Amplifier vs. Temperature



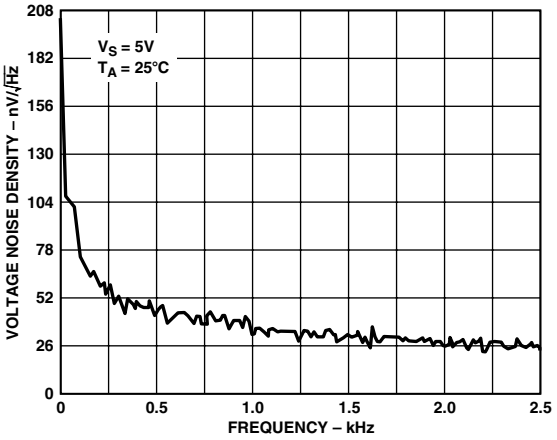
TPC 35. Voltage Noise Density vs. Frequency



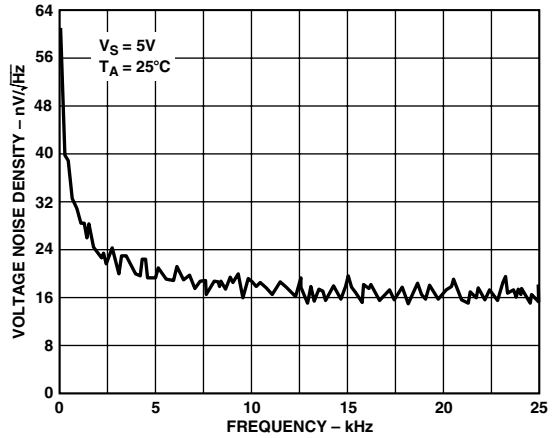
TPC 33. Supply Current per Amplifier vs. Supply Voltage



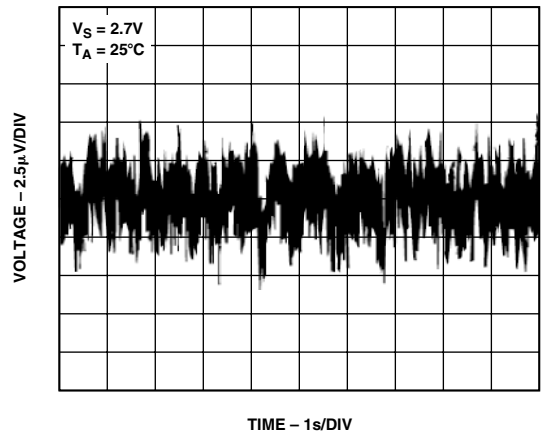
TPC 36. Voltage Noise Density vs. Frequency



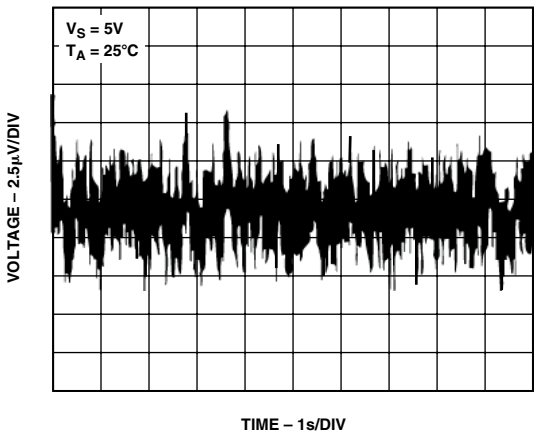
TPC 37. Voltage Noise Density vs. Frequency



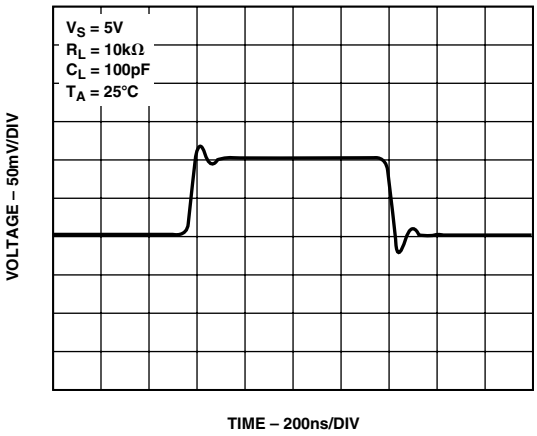
TPC 38. Voltage Noise Density vs. Frequency



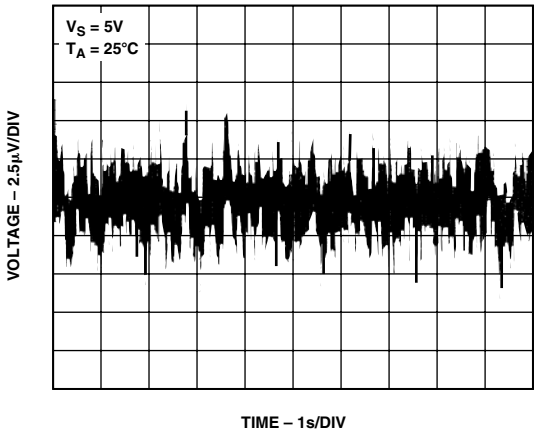
TPC 39. 0.1 Hz to 10 Hz Input Voltage Noise



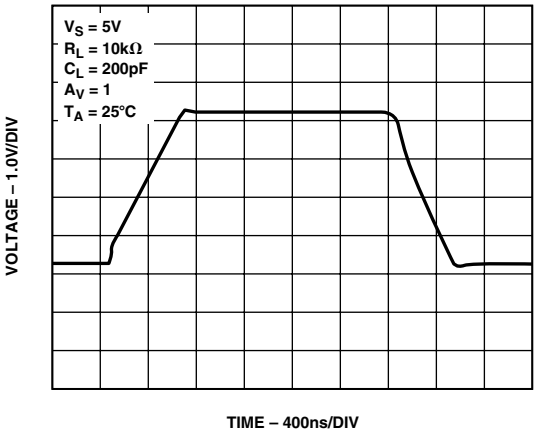
TPC 40. 0.1 Hz to 10 Hz Input Voltage Noise



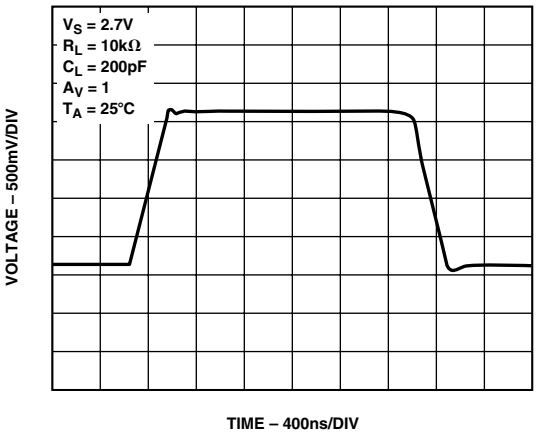
TPC 41. Small Signal Transient Response



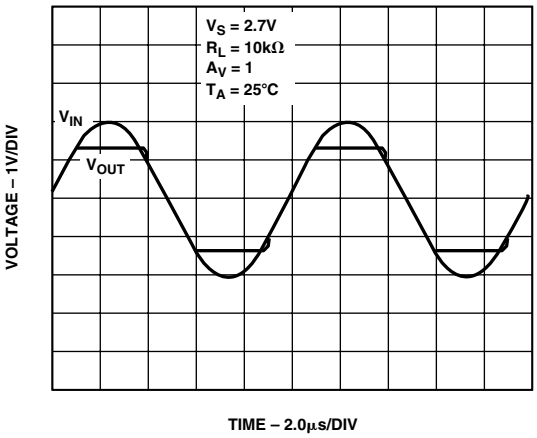
TPC 42. Small Signal Transient Response



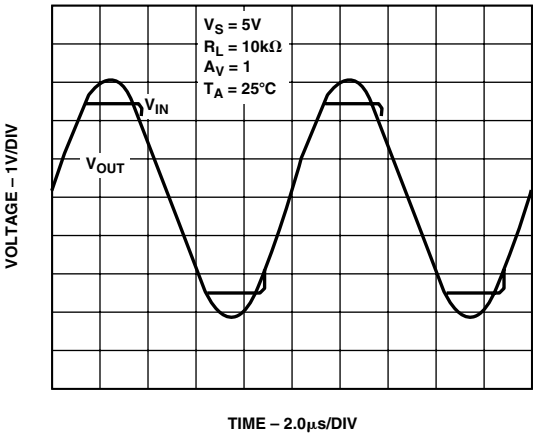
TPC 43. Large Signal Transient Response



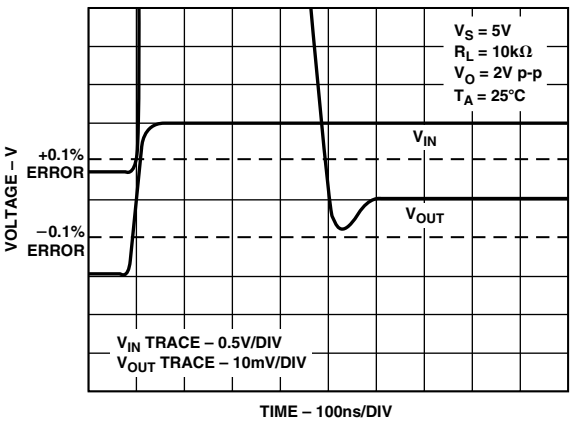
TPC 44. Large Signal Transient Response



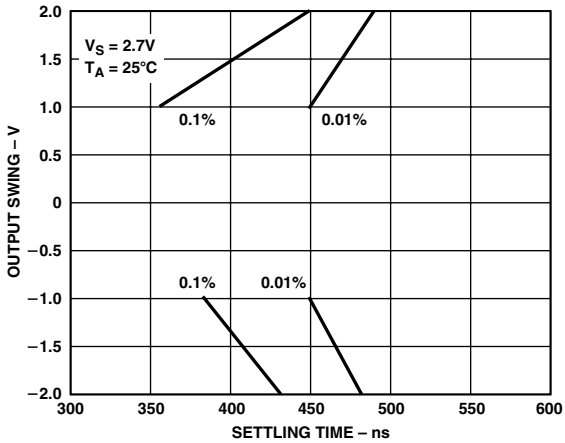
TPC 45. No Phase Reversal



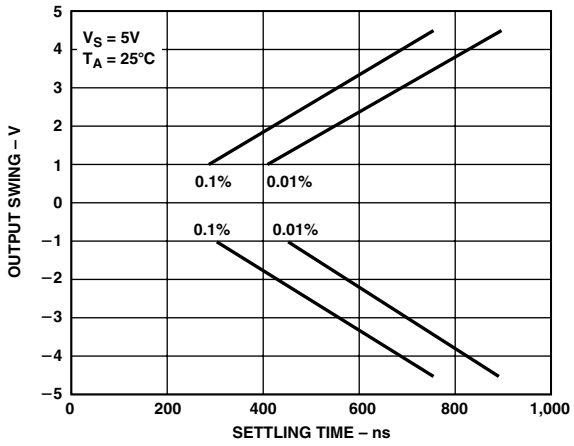
TPC 46. No Phase Reversal



TPC 47. Settling Time



TPC 48. Output Swing vs. Settling Time



TPC 49. Output Swing vs. Settling Time

THEORY OF OPERATION

The AD8601/AD8602 family of amplifiers are rail-to-rail input and output precision CMOS amplifiers specified from 2.7 V to 5.0 V of power supply voltage. These amplifiers use Analog Devices' proprietary technology called DigiTrim™ to achieve a higher degree of precision than available from most CMOS amplifiers. DigiTrim technology is a method of trimming the offset voltage of the amplifier after it has already been assembled. The advantage in post-package trimming lies in the fact that it corrects any offset voltages due to the mechanical stresses of assembly. This technology is scalable and utilized with every package option, including SOT23-5, providing lower offset voltages than previously achieved in these small packages.

The DigiTrim process is done at the factory and does not add additional pins to the amplifier. All AD860x amplifiers are available in standard op amp pinouts, making DigiTrim completely transparent to the user. The AD860x can be used in any precision op amp application.

The input stage of the amplifier is a true rail-to-rail architecture, allowing the input common-mode voltage range of the op amp to extend to both positive and negative supply rails. The voltage swing of the output stage is also rail-to-rail and is achieved by using an NMOS and PMOS transistor pair connected in a common-source configuration. The maximum output voltage swing is proportional to the output current, and larger currents will limit how close the output voltage can get to the supply rail. This is a characteristic of all rail-to-rail output amplifiers. With 1 mA of output current, the output voltage can reach within 20 mV of the positive rail and 15 mV of the negative rail.

The open-loop gain of the AD860x is 100 dB, typical, with a load of 2 kΩ. Because of the rail-to-rail output configuration, the gain of the output stage, and thus the open-loop gain of the amplifier, is dependent on the load resistance. Open-loop gain will decrease with smaller load resistances. Again, this is a characteristic inherent to all rail-to-rail output amplifiers.

Rail-to-Rail Input Stage

The input common-mode voltage range of the AD860x extends to both positive and negative supply voltages. This maximizes the usable voltage range of the amplifier, an important feature for single supply and low voltage applications. This rail-to-rail input range is achieved by using two input differential pairs, one NMOS and one PMOS, placed in parallel. The NMOS pair is active at the upper end of the common-mode voltage range, and the PMOS pair is active at the lower end of the common-mode range.

The NMOS and PMOS input stage are separately trimmed using DigiTrim to minimize the offset voltage in both differential pairs. Both NMOS and PMOS input differential pairs are active in a 500 mV transition region, when the input common-mode voltage is between approximately 1.5 V and 1 V below the positive supply voltage. Input offset voltage will shift slightly in this transition region, as shown in Figures 5 and 6. Common-mode rejection ratio will also be slightly lower when the input common-mode voltage is within this transition band. Compared to the Burr Brown OPA2340 rail-to-rail input amplifier, shown in Figure 1, the AD860x, shown in Figure 2, exhibits lower offset voltage shift across the entire input common-mode range, including the transition region.

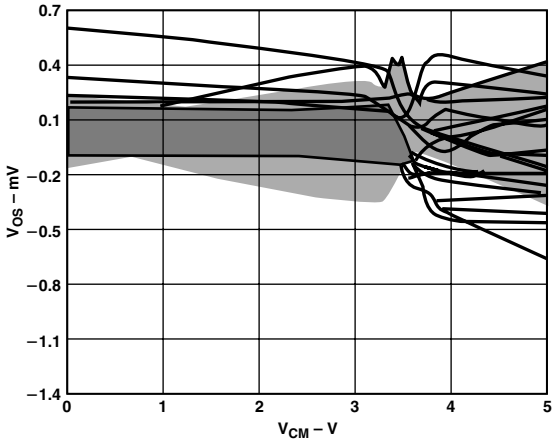


Figure 1. Burr Brown OPA2340UR Input Offset Voltage vs. Common-Mode Voltage, 24 SOIC Units @ 25°C

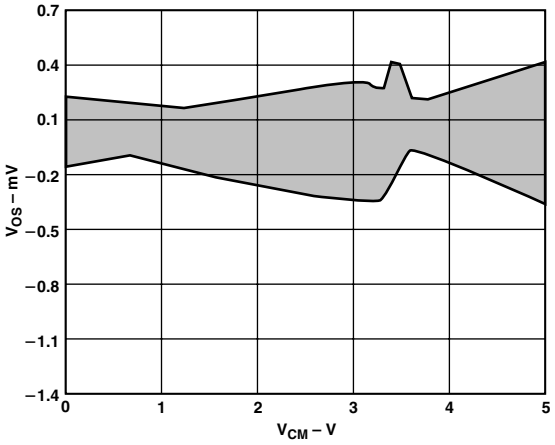


Figure 2. AD8602AR Input Offset Voltage vs. Common-Mode Voltage, 300 SOIC Units @ 25°C

DigiTrim is a trademark of Analog Devices.

Input Overvoltage Protection

As with any semiconductor device, if a condition could exist for the input voltage to exceed the power supply, the device's input overvoltage characteristic must be considered. Excess input voltage will energize internal PN junctions in the AD860x, allowing current to flow from the input to the supplies.

This input current will not damage the amplifier provided it is limited to 5 mA or less. This can be ensured by placing a resistor in series with the input. For example, if the input voltage could exceed the supply by 5 V, the series resistor should be at least (5 V/5 mA) = 1 kΩ. With the input voltage within the supply rails, a minimal amount of current is drawn into the inputs which, in turn, causes a negligible voltage drop across the series resistor. Thus, adding the series resistor will not adversely affect circuit performance.

Overdrive Recovery

Overdrive recovery is defined as the time it takes the output of an amplifier to come off the supply rail when recovering from an overload signal. This is tested by placing the amplifier in a closed-loop gain of 10 with an input square wave of 2 V peak-to-peak while the amplifier is powered from either 5 V or 3 V.

The AD860x has excellent recovery time from overload conditions. The output recovers from the positive supply rail within 200 ns at all supply voltages. Recovery from the negative rail is within 500 ns at 5 V supply, decreasing to within 350 ns when the device is powered from 2.7 V.

Power-On Time

Power-on time is important in portable applications, where the supply voltage to the amplifier may be toggled to shut down the device to improve battery life. Fast power-up behavior ensures the output of the amplifier will quickly settle to its final voltage, thus improving the power-up speed of the entire system. Once the supply voltage reaches a minimum of 2.5 V, the AD860x will settle to a valid output within 1 µs. This turn-on response time is faster than many other precision amplifiers, which can take tens or hundreds of microseconds for their output to settle.

Using the AD8602 in High Source Impedance Applications

The CMOS rail-to-rail input structure of the AD860x allows these amplifiers to have very low input bias currents, typically 0.2 pA. This allows the AD860x to be used in any application that has a high source impedance or must use large value resistances around the amplifier. For example, the photodiode amplifier circuit shown in Figure 3 requires a low input bias current op amp to reduce output voltage error. The AD8601 minimizes offset errors due to its low input bias current and low offset voltage.

The current through the photodiode is proportional to the incident light power on its surface. The 4.7 MΩ resistor converts this current into a voltage, with the output of the AD8601 increasing at 4.7 V/µA. The feedback capacitor reduces excess noise at higher frequencies by limiting the bandwidth of the circuit to:

$$BW = \frac{1}{2\pi(4.7\ M\Omega)C_F} \qquad (1)$$

Using a 10 pF feedback capacitor limits the bandwidth to approximately 3.3 kHz.

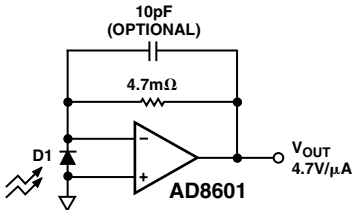


Figure 3. Amplifier Photdiode Circuit

High- and Low-Side Precision Current Monitoring

Because of its low input bias current and low offset voltage, the AD860x can be used for precision current monitoring. The true rail-to-rail input feature of the AD860x allows the amplifier to monitor current on either high-side or low-side. Using both amplifiers in an AD8602 provides a simple method for monitoring both current supply and return paths for load or fault detection. Figure 4 and 54 demonstrate both circuits.

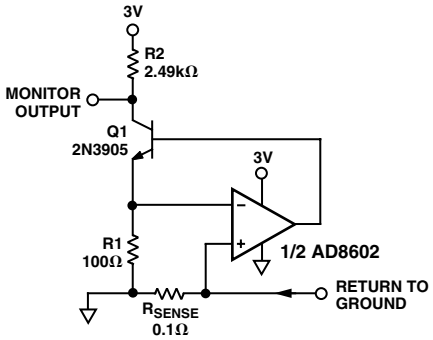


Figure 4. A Low-Side Current Monitor

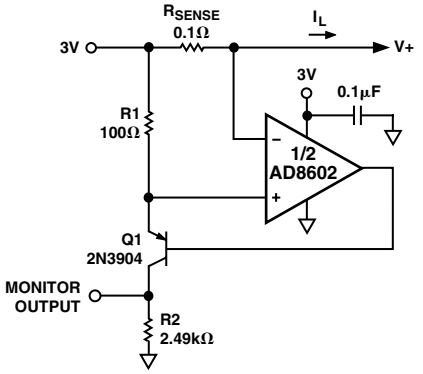


Figure 5. A High-Side Current Monitor

Voltage drop is created across the 0.1 Ω resistor that is proportional to the load current. This voltage appears at the inverting input of the amplifier due to the feedback correction around the op amp. This creates a current through R1 which, in turn, pulls current through R2. For the low side monitor, the monitor output voltage is given by:

$$Monitor\ Output = R2 \times \left(\frac{R_{SENSE}}{R1}\right) \times I_L \qquad (2)$$

For the high-side monitor, the monitor output voltage is:

$$Monitor\ Output = V + (-R2) \times \left(\frac{R_{SENSE}}{R1} \right) \times I_L \qquad (3)$$

Using the components shown, the monitor output transfer function is 2.5 V/A.

Using the AD8601 in Single Supply Mixed-Signal Applications

Single supply mixed-signal applications requiring 10 or more bits of resolution demand both a minimum of distortion and a maximum range of voltage swing to optimize performance. To ensure the A/D or D/A converters achieve their best performance an amplifier often must be used for buffering or signal conditioning. The 750 μV maximum offset voltage of the AD8601 allows the amplifier to be used in 12-bit applications powered from a 3 V single supply, and its rail-to-rail input and output ensure no signal clipping.

Figure 6 shows the AD8601 used as a input buffer amplifier to the AD7476, a 12-bit 1 MHz A/D converter. As with most A/D converters, total harmonic distortion (THD) increases with higher source impedances. By using the AD8601 in a buffer configuration, the low output impedance of the amplifier minimizes THD while the high input impedance and low bias current of the op amp minimizes errors due to source impedance. The 8 MHz gain-bandwidth product of the AD8601 ensures no signal attenuation up to 500 kHz, which is the maximum Nyquist frequency for the AD7476.

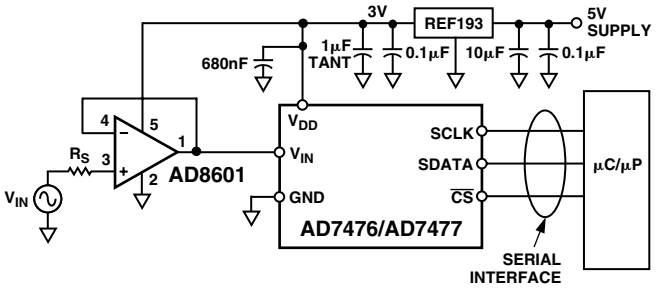


Figure 6. A Complete 3 V 12-Bit 1 MHz A/D Conversion System

Figure 7 demonstrates how the AD8601 can be used as an output buffer for the DAC for driving heavy resistive loads. The AD5320 is a 12-bit D/A converter that can be used with clock frequencies up to 30 MHz and signal frequencies up to 930 kHz. The rail-to-rail output of the AD8601 allows it to swing within 100 mV of the positive supply rail while sourcing 1 mA of current. The total current drawn from the circuit is less than 1 mA, or 3 mW from a 3 V single supply.

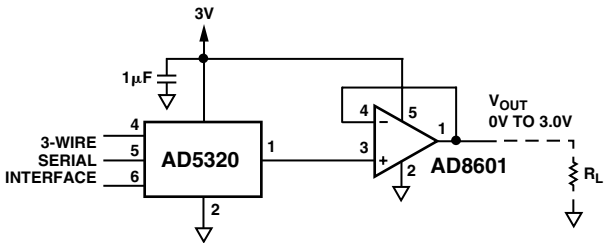


Figure 7. Using the AD8601 as a DAC Output Buffer to Drive Heavy Loads

The AD8601, AD7476, and AD5320 are all available in space-saving SOT-23 packages.

PC100 Compliance for Computer Audio Applications

Because of its low distortion and rail-to-rail input and output, the AD860x is an excellent choice for low cost, single supply audio applications, ranging from microphone amplification to line output buffering. TPC 34 shows the total harmonic distortion plus noise (THD + N) figures for the AD860x. In unity gain, the amplifier has a typical THD + N of 0.004%, or –86 dB, even with a load resistance of 600 Ω. This is compliant with the PC100 specification requirements for audio in both portable and desktop computers.

Figure 8 shows how an AD8602 can be interfaced with an AC'97 codec to drive the line output. Here, the AD8602 is used as a unity-gain buffer from the left and right outputs of the AC'97 CODEC. The 100 μF output coupling capacitors block dc current and the 20 Ω series resistors protect the amplifier from short-circuits at the jack.

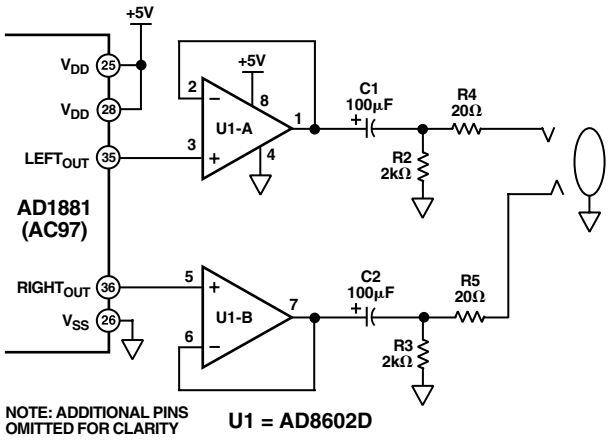


Figure 8. A PC100 Compliant Line Output Amplifier

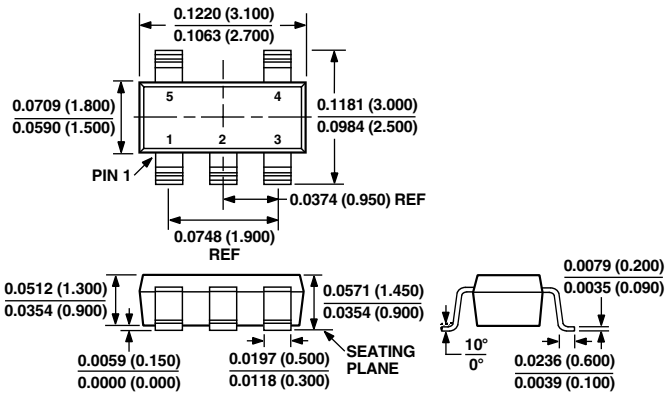
SPICE Model

The SPICE macro-model for the AD860x amplifier is available and can be downloaded from the Analog Devices website at **http://www.analog.com**. The model will accurately simulate a number of both dc and ac parameters, including open-loop gain, bandwidth, phase margin, input voltage range, output voltage swing versus output current, slew rate, input voltage noise, CMRR, PSRR, and supply current versus supply voltage. The model is optimized for performance at 27°C. Although it will function at different temperatures, it may lose accuracy with respect to the actual behavior of the AD860x.

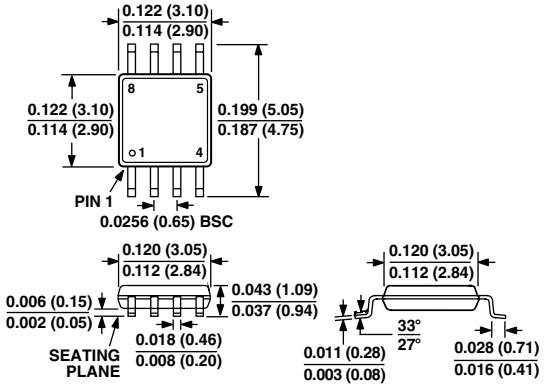
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

5-Lead SOT-23
(RT Suffix)



8-Lead μSOIC
(RM Suffix)



8-Lead SOIC
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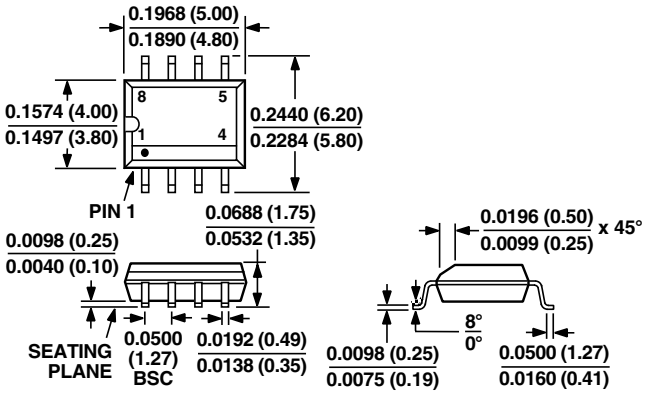

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