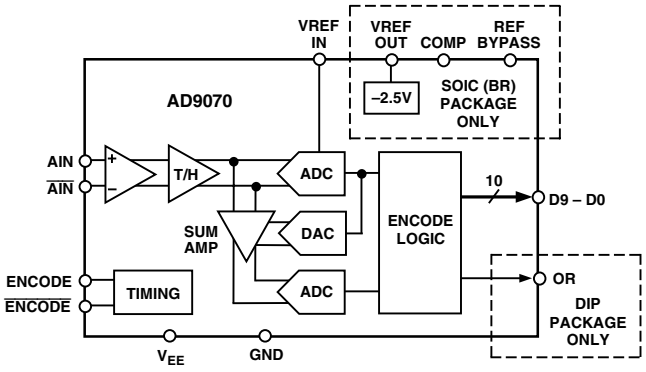
10-Bit, 100 MSPS A/D Converter

AD9070

FEATURES
10-Bit, 100 MSPS ADC
Low Power: 600 mW Typical at 100 MSPS
On-Chip Track/Hold
230 MHz Analog Bandwidth
SINAD = 54 dB @ 41 MHz
On–Chip Reference
1 V p-p Analog Input Range
Single Supply Operation: +5 V or –5 V
Differential Clock Input
Available in Standard Military Drawing Version

APPLICATIONS
Digital Communications
Signal Intelligence
Digital Oscilloscopes
Spectrum Analyzers
Medical Imaging
Radar
HDTV

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD9070 is a monolithic sampling analog-to-digital converter with an on-chip track-and-hold circuit and ECL digital interfaces. The product operates at a 100 MSPS conversion rate with outstanding dynamic performance over its full operating range.

The ADC requires only a single –5 V supply and an encode clock for full performance operation. The digital outputs are ECL compatible, while a differential clock input accommodates a wide range of logic levels. The AD9070 may be operated in a Positive ECL (PECL) environment with a single +5 V supply. An Out-of-Range output (OR) is available in the DIP version to indicate that a conversion result is outside the operating range. In both package styles, the output data are held at saturation levels during an out-of-range condition.

The input amplifier supports single-ended interfaces. An internal –2.5 V reference is included in the SOIC packaged device (an external voltage reference is required for the DIP version).

Fabricated on an advanced bipolar process, the AD9070 is available in a plastic SOIC package specified over the industrial temperature range (–40°C to +85°C), and a full MIL-PRF-38534 QML version (–55°C to +125°C) in a ceramic Dual-in-Line Package (DIP).

REV. B

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AD9070–SPECIFICATIONS

(V_{EE} = –5 V, ENCODE = 100 MSPS, outputs loaded with 100 Ω to –2 V unless otherwise noted)

Parameter	Temp	Test Level	AD9070BR Min	AD9070BR Typ	AD9070BR Max	5962-9756301HXC Min	5962-9756301HXC Typ	5962-9756301HXC Max	Units
RESOLUTION				10			10		Bit
DC ACCURACY									
Differential Nonlinearity	+25°C	I		±0.6	+1.25/–1.0		±0.6	+1.25/–1.0	LSB
	Full	VI		±0.7	+1.5/–1.0		±0.9	+2.00/–1.0	LSB
Integral Nonlinearity	+25°C	I		±0.6	±1.5		±0.6	±1.5	LSB
	Full	VI		±0.9			±1.5	±2.25	LSB
No Missing Codes	Full	VI		Guaranteed			Guaranteed		
Gain Error[1]	+25°C	I		±1	±4		±1	±4	% FS
	Full	VI					±2	±6	% FS
Gain Tempco[1]	Full	V		115			130		ppm/°C
ANALOG INPUT									
Input Voltage Range (with Respect to $\overline{AIN}$)	Full	V		±512			±512		mV p-p
Common-Mode Voltage	Full	V		–2.5 ± 0.2			–2.5 ± 0.2		V
Input Offset Voltage	+25°C	I		±7	±18		±7	±18	mV
	Full	I		±8			±9	±20	mV
Input Resistance	+25°C	I	10	40		10	40		kΩ
	Full	I		40		10	40		kΩ
Input Capacitance	+25°C	V		3			3		pF
Input Bias Current	+25°C	I		75	200		75	200	µA
	Full	I		75			75	200	µA
Analog Bandwidth, Full Power	+25°C	V		230			230		MHz
REFERENCE OUTPUT									
Output Voltage	Full	VI	–2.4	–2.5	–2.6		N/A		V
Temperature Coefficient	Full	V		170			N/A		ppm/°C
SWITCHING PERFORMANCE									
Maximum Conversion Rate	Full	VI	100			100			MSPS
Minimum Conversion Rate	Full	IV			40			40	MSPS
Encode Pulse Width High (t_{EH})	+25°C	IV	4.5		13	4.5		13	ns
Encode Pulse Width Low (t_{EL})	+25°C	IV	4.5		13	4.5		13	ns
Aperture Delay (t_A)	+25°C	V		0.85			0.85		ns
Aperture Uncertainty (Jitter)	+25°C	V		2.5			2.5		ps rms
Output Valid Time (t_V)[2]	Full	VI	1.5	2.6		1.5	2.6		ns
Output Propagation Delay (t_{PD})[2]	Full	VI		3.0	4.0		3.0	4.0	ns
Output Rise Time (t_R)	Full	VI		0.5			0.5	1.2	ns
Output Fall Time (t_F)	Full	VI		0.5			0.5	1.2	ns
DIGITAL INPUTS									
Logic "1" Voltage	Full	IV	–1.1		–0.4	–1.1		–0.4	V
Logic "0" Voltage	Full	IV			–1.5			–1.5	V
Logic "1" Current	Full	VI			±10			±10	µA
Logic "0" Current	Full	VI			±10			±10	µA
Input Capacitance	+25°C	V		3			3		pF
DIGITAL OUTPUTS									
Logic "1" Voltage	Full	VI	–1.1			–1.15			V
Logic "0" Voltage	Full	VI			–1.65			–1.60	V
Output Coding				Twos Complement			Twos Complement		
POWER SUPPLY									
V_{EE} Supply Current (V_{EE} = –5 V)	Full	VI	80	120	150	80	120	150	mA
Power Dissipation[3]	Full	VI	400	600	750	400	600	750	mW
Power Supply Sensitivity[4]	+25°C	I		0.005	0.012		0.005	0.012	V/V

Parameter	Temp	Test Level	AD9070BR Min	AD9070BR Typ	AD9070BR Max	5962-9756301HXC Min	5962-9756301HXC Typ	5962-9756301HXC Max	Units
DYNAMIC PERFORMANCE[5]									
Transient Response	+25°C	V		3			3		ns
Overvoltage Recovery Time	+25°C	V		4			4		ns
Signal-to-Noise Ratio (SNR)									
(Without Harmonics)									
f_{IN} = 10.3 MHz	+25°C	I	55	57		55	57		dB
	Full	V		56			55		dB
f_{IN} = 41 MHz	+25°C	I	54	56		54	56		dB
	Full	V		55			54		dB
Signal-to-Noise Ratio (SINAD)									
(With Harmonics)									
f_{IN} = 10.3 MHz	+25°C	I	54	56		54	56		dB
	Full	V		55			54		dB
f_{IN} = 41 MHz	+25°C	I	51	54		51	54		dB
	Full	V		53			52		dB
Effective Number of Bit									
f_{IN} = 10.3 MHz	+25°C	I	8.8	9.2		8.8	9.2		Bits
f_{IN} = 41 MHz	+25°C	I	8.3	8.9		8.3	8.9		Bits
2nd Harmonic Distortion									
f_{IN} = 10.3 MHz	+25°C	I	63	70		63	70		dBc
f_{IN} = 41 MHz	+25°C	I	58	63		58	63		dBc
3rd Harmonic Distortion									
f_{IN} = 10.3 MHz	+25°C	I	65	71		65	71		dBc
f_{IN} = 41 MHz	+25°C	I	57	61		57	61		dBc
Two-Tone Intermod Distortion (IMD)									
f_{IN} = 10.3 MHz	+25°C	V		70			70		dBc
f_{IN} = 41 MHz	+25°C	V		60			60		dBc

NOTES
[1]Gain error and gain temperature coefficient are based on the ADC only (with a fixed –2.5 V external reference).
[2]t_V and t_{PD} are measured from the threshold crossing of the ENCODE input to the 50% levels of the digital outputs. The output ac load during test is 10 pF.
[3]Power dissipation is measured under the following conditions: f_S 100 MSPS, analog input is –1 dBfs at 10.3 MHz. Power dissipation does not include the current of the external ECL pull-down resistors that set the current in the ECL output followers.
[4]A change in input offset voltage with respect to a change in V_{EE}.
[5]SNR/harmonics based on an analog input voltage of –1.0 dBfs referenced to a 1.024 V full-scale input range.
Typical thermal impedance for the R style (SOIC) 28-lead package: θ_{JC} = 23°C/W, θ_{CA} = 48°C/W, θ_{JA} = 71°C/W.
Typical thermal impedance for the DH style (Ceramic DIP) 28-lead package: θ_{JC} = 8°C/W, θ_{CA} = 43°C/W, θ_{JA} = 51°C/W.

Contact DSCC to obtain the latest revision of the 5962-9756301 drawing.
Specifications subject to change without notice.

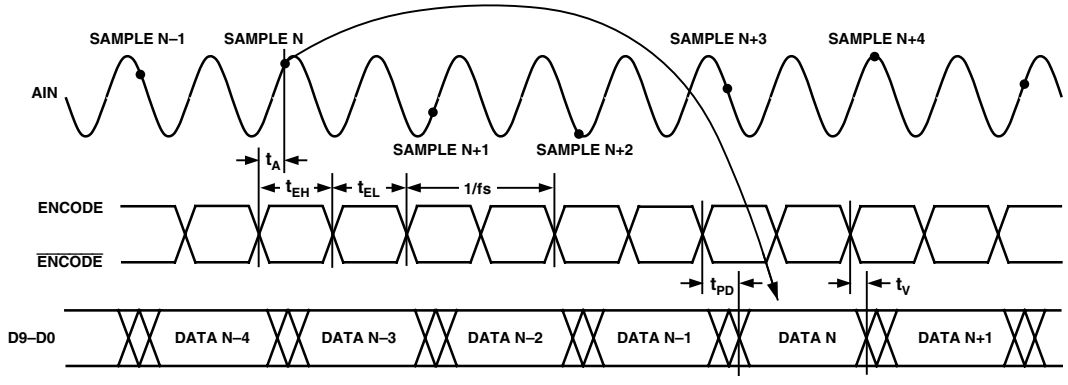


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

V_{EE} . . . . . –6 V
Analog Inputs . . . . . V_{EE} –1 V to +1.0 V
Digital Inputs . . . . . V_{EE} to 0.0 V
VREF IN, VREF OUT . . . . . V_{EE} to 0.0 V
Digital Output Current . . . . . 20 mA
Operating Temperature . . . . . –55°C to +125°C
Storage Temperature . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . +175°C
Maximum Case Temperature . . . . . +150°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions outside of those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

EXPLANATION OF TEST LEVELS

Test Level

I – 100% production tested.

II – 100% production tested at +25°C and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – 100% production tested at +25°C; guaranteed by design and characterization testing for industrial temperature range; 100% production tested at temperature extremes for military devices.

Table I. Output Coding

Step	AIN–$\overline{\text{AIN}}$	Code	Twos Complement	OR
1024	≥ 0.512 V	>511	01 1111 1111	1
1023	0.511 V	511	01 1111 1111	0
1022	0.510 V	510	01 1111 1110	0
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
513	0.001 V	1	00 0000 0001	0
512	0.000 V	0	00 0000 0000	0
511	–0.001 V	–1	11 1111 1111	0
•	•	•	•	•
•	•	•	•	•
•	•	•	•	•
1	–0.511 V	–511	10 0000 0001	0
0	–0.512 V	–512	10 0000 0000	0
–1	≤ –0.513 V	<512	10 0000 0000	1

ORDERING GUIDE

Model	Temperature Range	Package Option*
AD9070BR	–40°C to +85°C	R-28
AD9070/PCB	+25°C	Evaluation Board
5962-9756301HXC	–55°C to +125°C	DH-28

*DH = Ceramic DIP; R = Small Outline IC (SOIC).

CAUTION

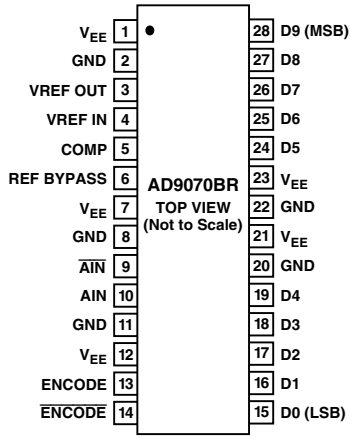
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD9070 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

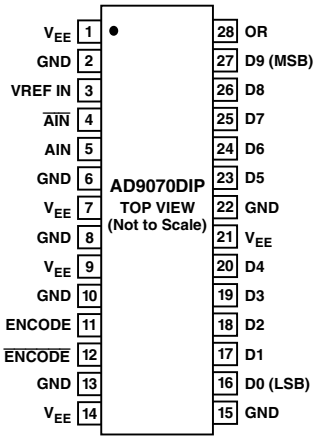
Pin Numbers AD9070BR R Package	Pin Numbers AD9070DIP D Package	Name	Function
1, 7, 12, 21, 23	1, 7, 9, 14, 21	V_{EE}	Negative Power Supply. Nominally –5.0 V.
2, 8, 11, 20, 22	2, 6, 8, 10, 13, 15, 22	GND	Ground.
3	N/A	VREF OUT	Internal Reference Output (–2.5 V typical); Bypass with 0.1 μF to Ground.
4	3	VREF IN	Reference Input for ADC (–2.5 V typical).
5	N/A	COMP	Internal Amplifier Compensation, 0.1 μF to V_{EE}.
6	N/A	REF BYPASS	Reference Bypass Node, 0.1 μF to V_{EE}.
9	4	$\overline{\text{AIN}}$	Analog Input – Complement.
10	5	AIN	Analog Input – True.
13	11	ENCODE	Encode Clock for ADC (ADC Samples on Rising Edge of ENCODE).
14	12	$\overline{\text{ENCODE}}$	Encode Clock Complement (ADC Samples on Falling Edge of $\overline{\text{ENCODE}}$).
28–24, 19–15	27–23, 20–16	D9–D0	Digital Outputs of ADC. D9 is the MSB. Data is twos complement.
N/A	28	OR	Out-of-Range Output. Goes HIGH when the converted sample is more positive than 1FFh or more negative than 200h (Twos Complement Coding).

PIN CONFIGURATIONS

SOIC



Ceramic DIP



AD9070–Typical Circuit Applications

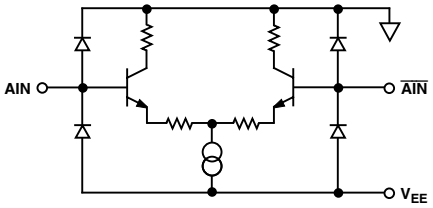


Figure 2. Equivalent Analog Input Circuit

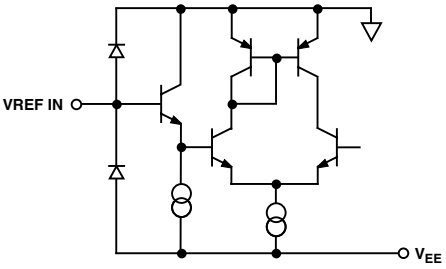


Figure 3. Equivalent Reference Input Circuit

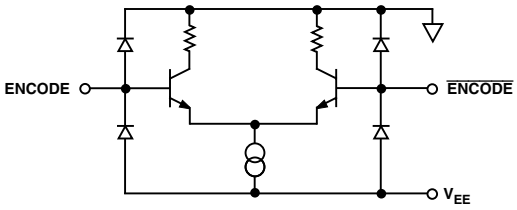


Figure 4. Equivalent Encode Input Circuit

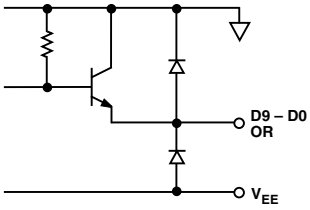


Figure 5. Equivalent Digital Output Circuit

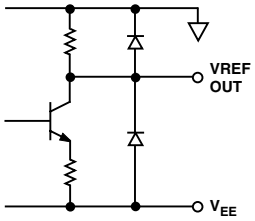


Figure 6. Equivalent Reference Output Circuit

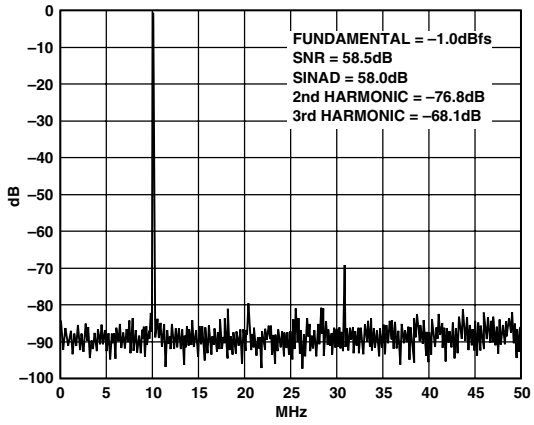


Figure 7. Spectrum: f_S = 100 MSPS, f_{IN} = 10 MHz

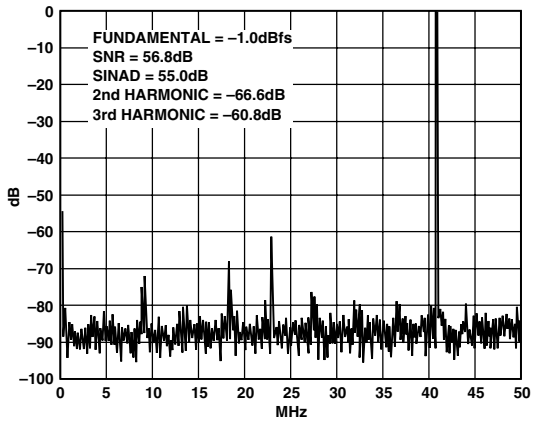


Figure 8. Spectrum: f_S = 100 MSPS, f_{IN} = 40 MHz

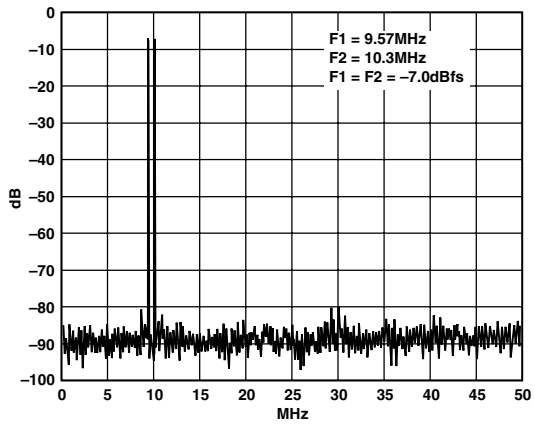


Figure 9. Two Tone Intermodulation Distortion

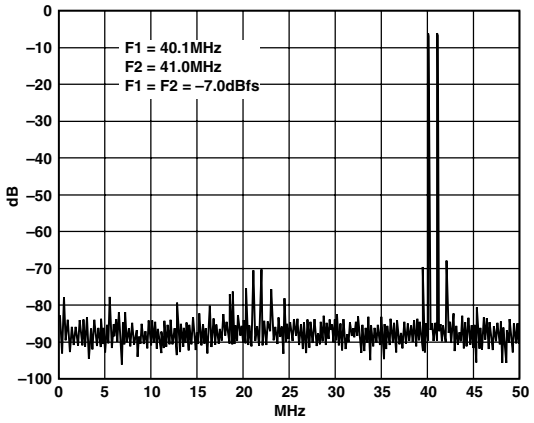


Figure 10. Two Tone Intermodulation Distortion

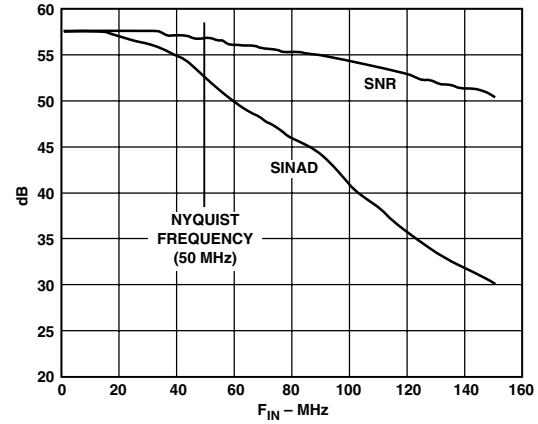


Figure 11. SNR vs. f_{IN}; f_S = 100 MSPS

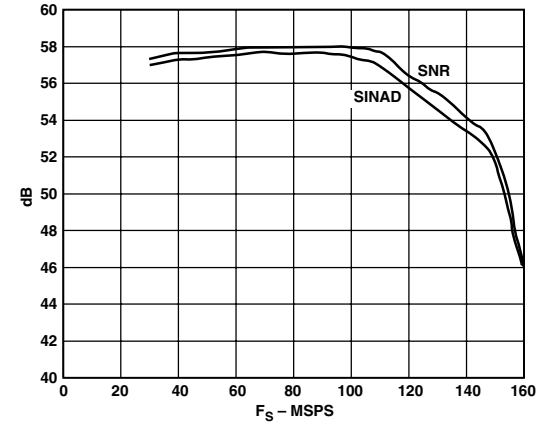


Figure 12. SNR vs. f_S: f_{IN} = 10.3 MHz

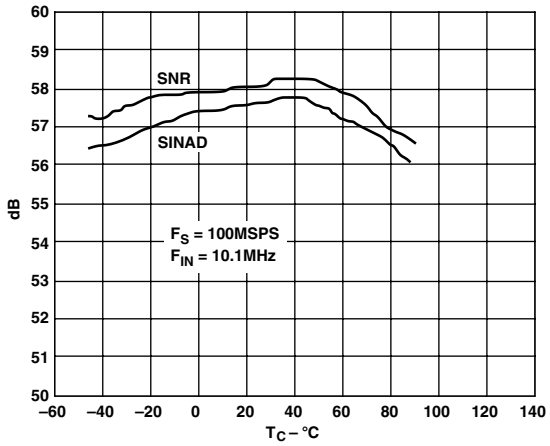


Figure 13. SNR vs. T_C: BR Package (SOIC)

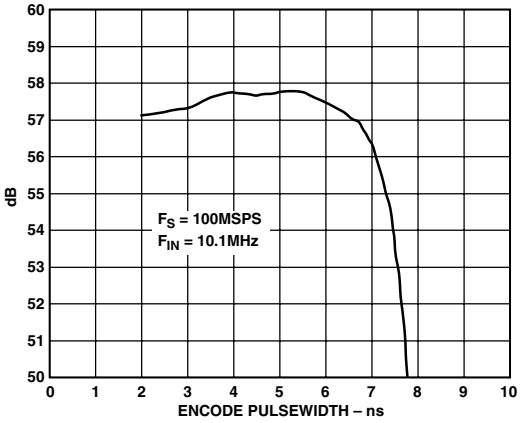


Figure 15. SNR vs. Clock Pulse Width (t_{EH})

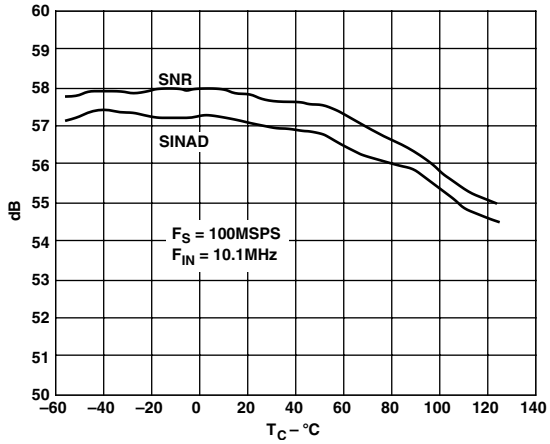


Figure 14. SNR vs. T_C: DIP Package

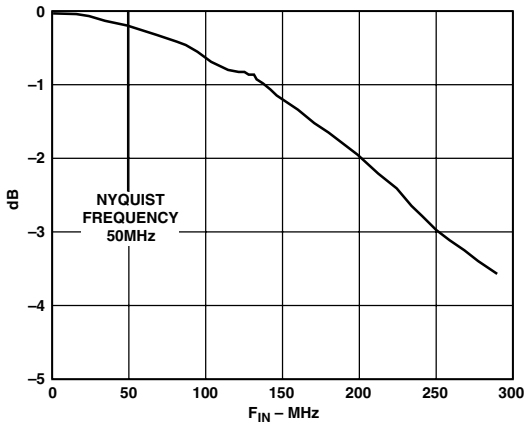


Figure 16. Frequency Response

APPLICATION NOTES

Theory of Operation

The AD9070 employs a two-step subranging architecture with digital error correction.

The sampling and conversion process is initiated by a rising edge at the ENCODE input. The analog input signal is buffered by a high speed differential amplifier and applied to a track-and-hold (T/H) circuit that captures the value of the input at the sampling instant and maintains it for the duration of the conversion.

The coarse quantizer (ADC) produces a five-bit estimate of the input value. Its digital output is reconverted to analog form by the reconstruction DAC and subtracted from the input signal in the SUM AMP. The second stage quantizer generates a six-bit representation of the difference signal. The eleven bits are presented to the ENCODE LOGIC, which corrects for range overlap errors and produces an accurate ten-bit result.

Data are strobed to the output on the rising edge of the ENCODE input, with the data from sample N appearing on the output following ENCODE rising edge N+3.

USING THE AD9070

ENCODE Input

Any high speed A/D converter is extremely sensitive to the quality of the sampling clock provided by the user. A Track/Hold circuit is essentially a mixer, and any noise, distortion or timing jitter on the clock will be combined with the desired signal at the A/D output. For that reason, considerable care has been taken in the design of the ENCODE input of the AD9070 and the user is advised to give commensurate thought to the clock source.

The ENCODE input is fully differential and may be operated in a differential or a single-ended mode. It has a common-mode range of –1 V to –3 V, and is easily driven by a differential ECL driver. Proper termination at the A/D is important.

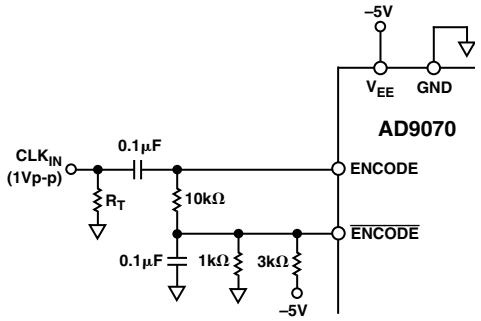


Figure 17. Single-Ended ENCODE: AC Coupled

In single-ended mode, the $\overline{\text{ENCODE}}$ input must be tied to an appropriate reference voltage, generally midway between the high and the low levels of the incoming logic signal. Many ECL circuits provide a V_{BB} reference voltage intended for this purpose. If a reference voltage is produced by dividing the power supply voltage, any noise on the supply used will couple to the clock input and then to the output data. This is not recommended. A better approach is to develop the required voltage from the internal or external converter voltage reference (VREF OUT).

Very small timing errors can reduce the performance of an A/D dramatically. Total jitter of only 3.2 ps will limit the performance of an A/D sampling a full-scale 50 MHz signal to nine effective bits. The AD9070's specified aperture jitter of 2.5 ps leaves only 2.0 ps of jitter budget for the clock source (an RSS calculation).

The cleanest clock source is only a crystal oscillator producing a pure sine wave. In this configuration, or with any roughly symmetrical clock input, the input can be ac coupled and biased to a reference voltage that also provides the $\overline{\text{ENCODE}}$ input (Figure 17). This ensures that the reference voltage is centered on the ENCODE signal.

Digital Outputs

The digital outputs are compatible with 10K ECL logic. The suggested pull-down is 100 Ω to –2 V. However, to reduce power consumption, higher value pull-down resistors can be used when driving very low capacitance loads or at reduced encode rates. The falling edge slew rate of the output bits will be degraded with higher value pull-down resistors.

Analog Input

The analog input to the AD9070 is a differential amplifier, but the design has been optimized for a single-ended input. The $\overline{\text{AIN}}$ input should be connected or bypassed to the ground reference of the input signal. For best dynamic performance, impedances at AIN and $\overline{\text{AIN}}$ should match.

The circuit in Figure 18 illustrates a simple ac-coupled interface. The midscale input voltage and the $\overline{\text{AIN}}$ levels are both provided by the internal reference (VREF OUT).

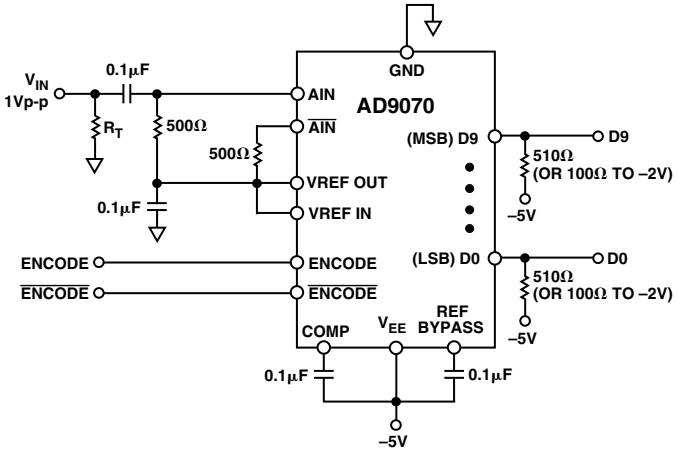


Figure 18. AD9070 in –5 V (ECL) Environment

Figure 19 shows typical connections for the analog inputs when using the AD9070 in a dc-coupled system with single-ended signals. The AD820 is used to offset the ground referenced input signal to the level required by the AD9070. A very high performance amplifier, such as the AD9631, is required to avoid degrading the analog signal presented to the ADC. A buffered ac interface is easily implemented, with even fewer components (Figure 20).

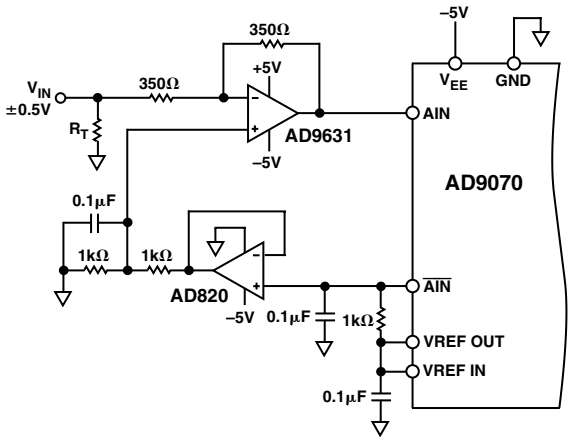


Figure 19. DC-Coupled Input

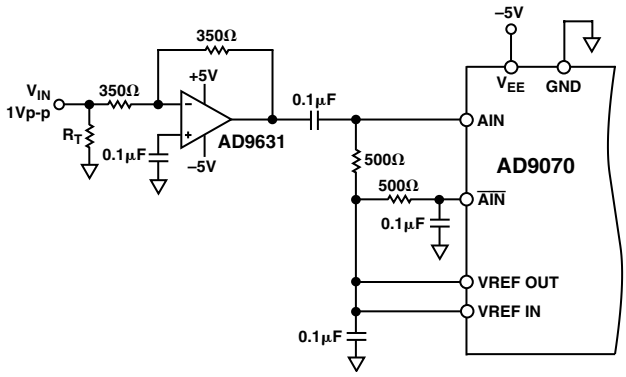


Figure 20. AC-Coupled Input

Special care was taken in the design of the analog input section of the AD9070 to prevent damage and corruption of data when the input is overdriven. The nominal input range is –1.988 V to –3.012 V (1.024 V p–p centered at –2.5 V). Out-of-range comparators detect when the analog input signal is out of this range and set the OR output signal HIGH. The digital outputs are locked at plus or minus full scale (1FFh or 200h) for voltages that are out of range but between –1 V and –5 V. Input voltages outside of this range may result in invalid codes at the ADCs output.

When the analog input signal returns to the nominal range, the out-of-range comparators return the ADC to its active mode and the device recovers in approximately 3 ns.

The input is protected to one volt outside of the power supply rails. For nominal power (–5 V and ground), the analog input will not be damaged with signals ranging from –6.0 V to +1.0 V.

Voltage Reference

A stable and accurate –2.5 V voltage reference is built into the AD9070 (VREF OUT) in the SOIC (BR) package. In normal operation, the internal reference is used by strapping Pins 3 and 4 of the AD9070 together. The internal reference can provide 100 μA of extra drive current that may be used for other circuits.

Some applications may require greater accuracy, improved temperature performance or adjustment of the gain of the AD9070, which cannot be obtained by using the internal reference. For these applications, an external –2.5 V reference can be connected to VREF IN, which requires 5 μA of drive current (Figure 21).

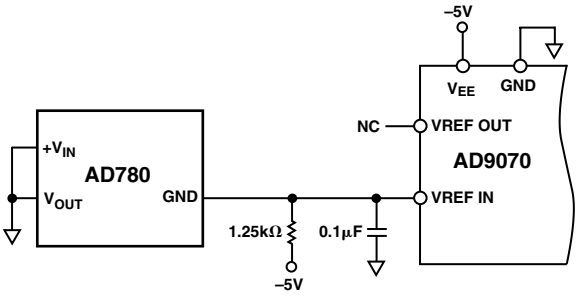


Figure 21. Using the AD780 Voltage Reference

The input range can be adjusted by varying the reference voltage applied to the AD9070. No appreciable degradation in performance occurs when the reference is adjusted ±4%. The full-scale range of the ADC tracks reference voltage changes linearly.

Timing

The performance of the AD9070 is insensitive to the duty cycle of the clock over a wide range of operating conditions: pulse width variations of as much as ±20% will cause no degradation in performance (see Figure 15).

The AD9070 provides latched data outputs, with three pipeline delays. Data outputs are available one propagation delay (t_{PD}) after the rising edge of the encode command (Figure 1). The length of the output data lines and loads placed on them should be minimized to reduce transients within the AD9070; these transients can detract from the converter's dynamic performance.

The minimum guaranteed conversion rate of the AD9070 is 40 MSPS. At clock rates below 40 MSPS, dynamic performance may degrade. The AD9070 will operate in bursts, but the user must flush the internal pipeline each time the clock restarts. Valid data will be produced on the fourth rising edge of the ENCODE signal after the clock is restarted.

+5 V Operation

The AD9070 may be operated above ground, with a single +5 V power supply. All power supply ground pins are connected to +5 V, and V_{EE} pins are connected to ground (Figure 22). Care must be taken in connecting signals and determining bypass rails.

The reference voltage (REF OUT) is still generated with respect to the positive rail, which is now +5 V. It is nominally +2.5 V, but its voltage with respect to ground will vary directly with changes in the power supply voltage (for example, if the power supply goes to +5.1 V, the reference becomes +2.6 V). The reference input is likewise processed with respect to +5 V. This dictates that these pins be bypassed to +5 V as well. However, the COMP and REF BYPASS pins must continue to be bypassed to the most negative supply, which is now ground. The $\overline{AIN}$ input must still be connected or bypassed to the ground reference of the input signal.

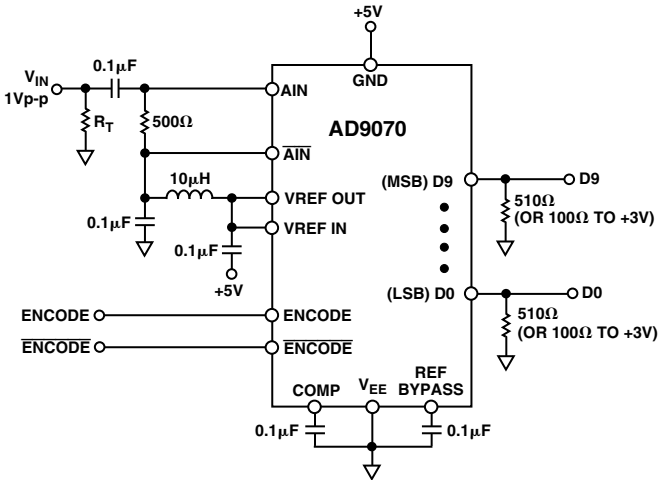


Figure 22. AD9070 in +5 V (PECL) Environment

Package Options

The AD9070 is available in two packages. The BR package is a standard 28-lead Small Outline IC (SOIC). The DIP package is a ceramic Dual-in-Line Hybrid. The SOIC is offered in a commercial grade, and specified over the industrial (–40°C to +85°C) temperature range. The DIP is a full MIL-PRF-38534 QML version that operates from (–55°C to +125°C).

The SOIC version includes the on-chip voltage reference, whereas the DIP does not. The DIP, however, provides the Overrange (OR) output, and includes reference and power supply bypassing, along with an internal compensation capacitor.

Equivalent performance may be obtained with either part though, due to the internal bypassing, the DIP is not as sensitive to board layout and parasitics.

AD9070BR EVALUATION BOARD

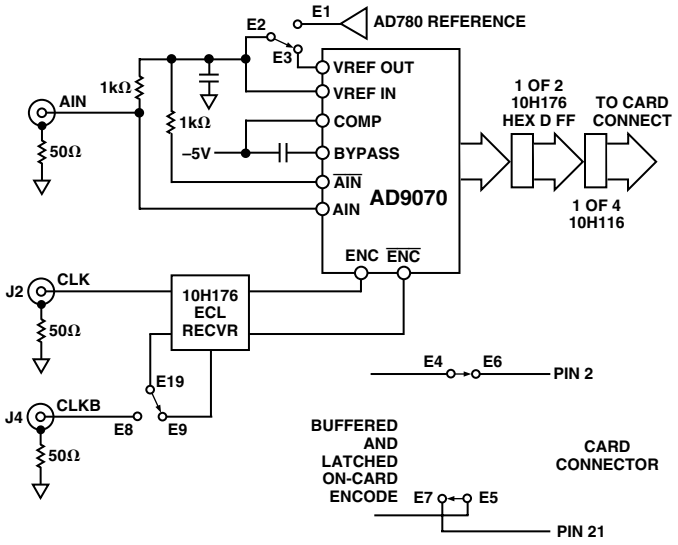


Figure 23.

The AD9070 evaluation board is a convenient and easy way to evaluate the performance of the AD9070 in the SOIC package. The board consists of an AD780 voltage reference (configured for –2.5 V), two 10H176 (hex D flip flop) for capturing data from the A/D converter and five 10H116 triple line receivers for buffering the encode signal and driving the data via the edge connector. Termination resistors (RP11, RP12, and RP14) are provided for the data leaving the board via the connector; (they can be removed if termination resistors are already provided by the user).

Analog Input

The evaluation board requires a 1 V peak-to-peak signal centered at ground (J1). This signal is ac coupled and then dc shifted –2.5 V before it is input to the A/D converter.

Encode

The AD9070 encode inputs can be driven single ended (connect E9 to E19 and drive J2 with an ECL signal) or differentially (connect E8 to E19 and drive J2 and J4 with differential ECL signals). The board is shipped in single ended configuration. The differential encode signal leaving the board via the connector can be inverted by interchanging E4, E5, E6, and E7 (connect E4 to E7 and E5 to E6 or E4 to E6 and E7 to E5). This ensures that the user will be able to capture the data coming from the evaluation board.

Data Out

Data goes single-ended into the 10H116 flip flops but comes out differentially. The data coming out of the AD9070 is in twos complement format, but is changed to straight binary by inverting the MSB at the connector (on the schematic Bit 1 and Bit 1B are swapped).

Voltage Reference

The AD9070 can be operated using its internal bandgap reference (connect E2 to E3) or the on board AD780 external reference (connect E1 to E3). The board is shipped utilizing the internal voltage reference.

Layout

The AD9070 is not layout sensitive if some important guidelines are met. The evaluation board layout provides an example where these guidelines have been followed to optimize performance.

- Provide a good ground plane connecting the analog and digital sections.
- Excellent bypassing is essential. Chip caps with 0.1 μF values and 0603 dimensions are placed flush against the pins. Placing any of the caps on the bottom of the board can degrade performance. These techniques reduce the amount of parasitic inductance which can impact the bypassing ability of the caps.
- Separate power planes and supplies for the analog and digital sections are recommended.

The AD9070 evaluation board is provided as a design example for customers of Analog Devices. ADI makes no warranties express, statutory, or implied regarding merchantability or fitness for a particular purpose.

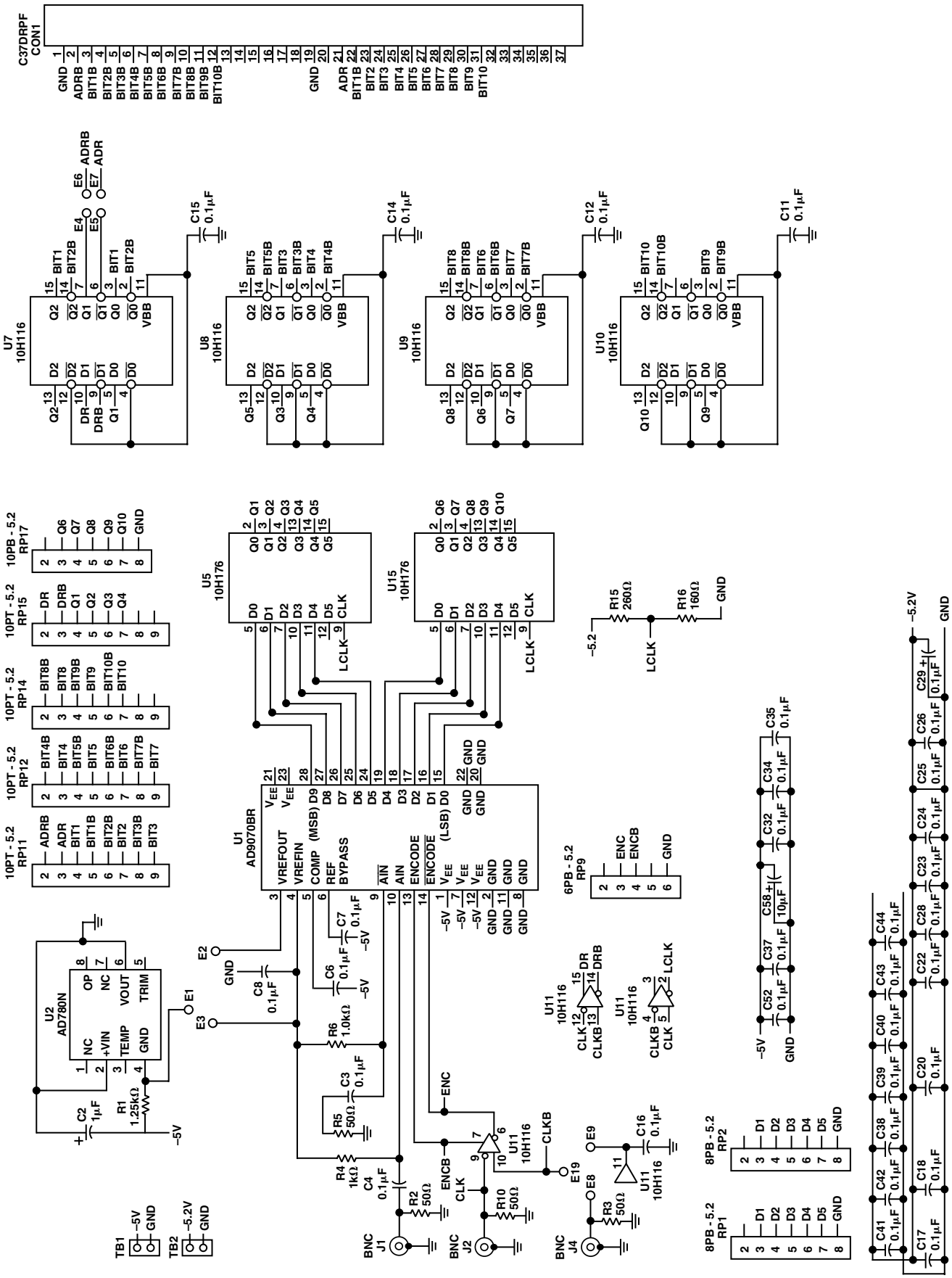


Figure 24. Evaluation Board Schematic

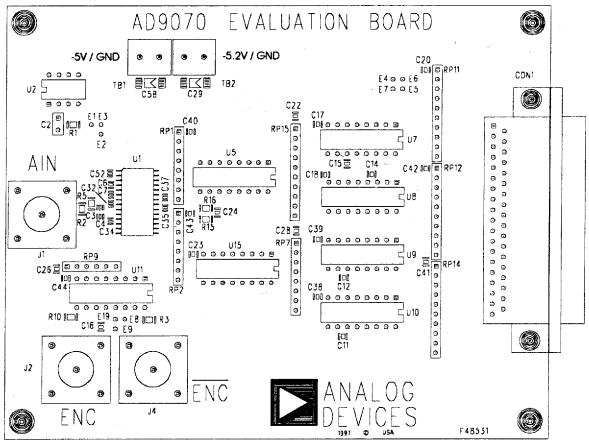


Figure 25. Component Side

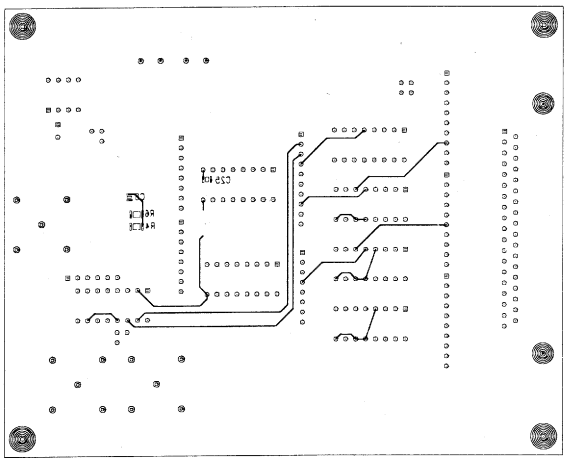


Figure 27. Bottom Side Trace + Components

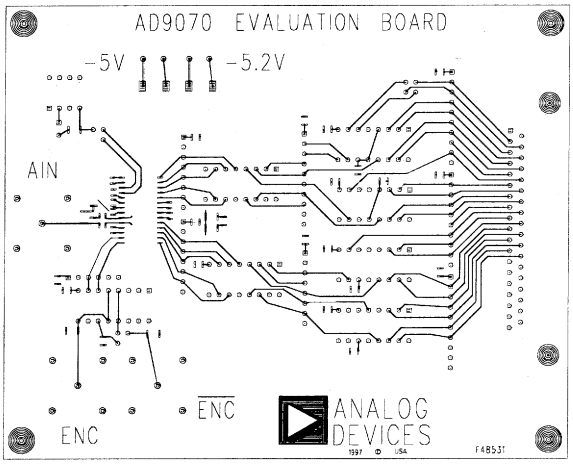


Figure 26. Component Side Signal Traces

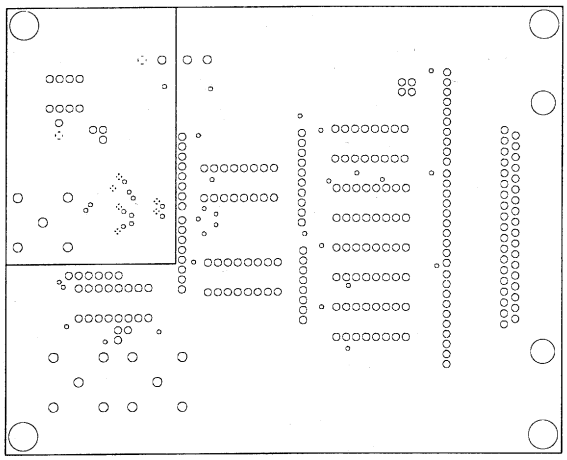


Figure 28. Analog/Digital Split Power Plane

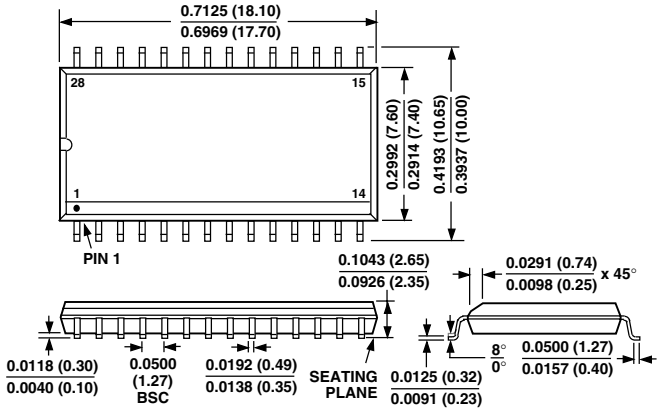
Table II. Evaluation Board Bill of Materials

ITEM	QTY	REFD	DESCRIPTION
1	5	U7–U11	10H116 – TRIPLE DIFFERENTIAL LINE RECEIVER
2	2	U5, U15	10H176 – 10KH HIGH SPEED ECL
3	4	RP11, RP12, RP14, RP15	10PT-5.2 – 10P TER RES NTWK
4	1	RP9	6PB-5.2 – 6P BUSED RES NTWK
5	2	TB1, TB2	8291Z2 – 2-PIN TERMINAL BLOCK
6	3	RP1, RP2, RP7	8PB-5.2 – 8P BUSED RES NTWK
7	1	U2	AD780N – HIGH PREC VOLT REF
8	1	U1	AD9070R – AD9070 SOIC ECL ADC
9	10	C3, C4, C6, C7, C8, C32, C34, C35, C37, C52	BCAP0603 – CER CHIP CAP 0603, .1 μF
10	24	C11, C12, C14–C18, C20, C22–C26, C28, C38–C44	BCAP0805 – CER CHIP CAP 0805, .1 μF
11	2	C29, C58	BCAPTAJD – CHIP TANT CAP, 10 μF
12	3	J1, J2, J4	BNC – BNC COAX CONN PCMT
13	1	R1	BRES1206 – SURF MT RES 1206, 1.25K
14	1	R16	BRES1206 – SURF MT RES 1206, 160
15	2	R4, R6	BRES1206 – SURF MT RES 1206, 1K
16	1	R15	BRES1206 – SURF MT RES 1206, 260
17	4	R2, R3, R5, R10	BRES1206 – SURF MT RES 1206, 50
18	1	CON1	C37DRPF – 37P D CONN RT ANG PLASTIC PCMT FEMALE
19	1	C2	T330A – TANT CAP, 1 μF
20	10	E1–E9, E19	W-HOLE – WIRE HOLE

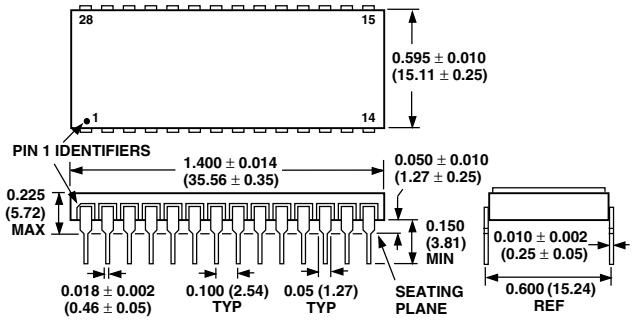
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28–Lead SOIC
(R–28)



28-Lead Hermetic Ceramic DIP
(DH-28)



C2996a–0–3/00 (rev. B)

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