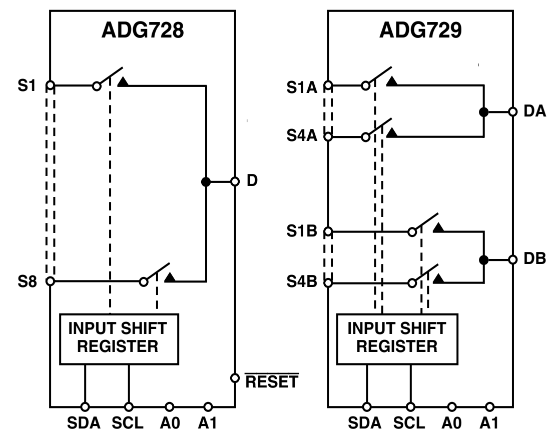
# CMOS, Low-Voltage, 2-Wire Serially-Controlled, Matrix Switches

# ADG728/ADG729

**FEATURES**
**2-Wire Serial Interface**
**2.7 V to 5.5 V Single Supply**
**2.5 Ω On Resistance**
**0.75 Ω On-Resistance Flatness**
**100 pA Leakage Currents**
**Single 8-to-1 Matrix Switch ADG728**
**Dual 4-to-1 Matrix Switch ADG729**
**Power-On Reset**
**Small 16-Lead TSSOP Package**

**APPLICATIONS**
**Data Acquisition Systems**
**Communication Systems**
**Relay Replacement**
**Audio and Video Switching**
**Automatic Test Equipment**

**FUNCTIONAL BLOCK DIAGRAMS**




## GENERAL DESCRIPTION

The ADG728 and ADG729 are CMOS analog matrix switches with a serially controlled 2-wire interface. The ADG728 is an 8-channel matrix switch, while the ADG729 is a dual 4-channel matrix switch. On resistance is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either multiplexers, demultiplexers or switch arrays and the input signal range extends to the supplies.

The ADG728 and ADG729 utilize a 2-wire serial interface that is compatible with the $I^2C$™ interface standard. Both have two external address pins (A0 and A1). This allows the 2 LSBs of the 7-bit slave address to be set by the user. Four of each of the devices can be connected to the one bus. The ADG728 also has a $\overline{\text{RESET}}$ pin that should be tied high if not in use.

Each channel is controlled by one bit of an 8-bit word. This means that these devices may be used in a number of different configurations; all, any, or none of the channels may be on at any one time.

On power-up of the device, all switches will be in the OFF condition and the internal shift register will contain all zeros.

All channels exhibit break-before-make switching action preventing momentary shorting when switching channels.

The ADG728 and ADG729 are available in 16-lead TSSOP packages.

## PRODUCT HIGHLIGHTS

1. 2-Wire Serial Interface.
2. Single Supply Operation. The ADG728 and ADG729 are fully specified and guaranteed with 3 V and 5 V supply rails.
3. Low On Resistance 2.5 Ω typical.
4. Any configuration of switches may be on at any one time.
5. Guaranteed Break-Before-Make Switching Action.
6. Small 16-Lead TSSOP Package.

$I^2C$ is a trademark of Philips Corporation.

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# ADG728/ADG729–SPECIFICATIONS[1] ($V_{DD}$ = 5 V ± 10%, GND = 0 V, unless otherwise noted.)

| Parameter | B Version 25°C | B Version –40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 2.5 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA; |
| | 4.5 | 5 | Ω max | Test Circuit 1 |
| On-Resistance Match Between | | 0.4 | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA |
| Channels ($\Delta R_{ON}$) | | 0.8 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | 0.75 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA |
| | | 1.2 | Ω max | |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = 5.5 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.01 | | nA typ | $V_D$ = 4.5 V/1 V, $V_S$ = 1 V/4.5 V, Test Circuit 2 |
| | ±0.1 | ±0.3 | nA max | |
| Drain OFF Leakage $I_D$ (OFF) | ±0.01 | | nA typ | $V_D$ = 4.5 V/1 V, $V_D$ = 1 V/4.5 V, Test Circuit 3 |
| | ±0.1 | ±1 | nA max | |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.01 | | nA typ | $V_D$ = $V_S$ = 4.5 V/1 V, Test Circuit 4 |
| | ±0.1 | ±1 | nA max | |
| LOGIC INPUTS (A0, A1)[2] | | | | |
| Input High Voltage, $V_{INH}$ | | 2.4 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.8 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | µA typ | |
| | | ±0.1 | µA max | |
| $C_{IN}$, Input Capacitance | 6 | | pF typ | |
| LOGIC INPUTS (SCL, SDA)[2] | | | | |
| Input High Voltage, $V_{INH}$ | | 0.7 $V_{DD}$ | V min | |
| | | $V_{DD}$ + 0.3 | V max | |
| Input Low Voltage, $V_{INL}$ | | –0.3 | V min | |
| | | 0.3 $V_{DD}$ | V max | |
| $I_{IN}$, Input Leakage Current | 0.005 | | µA typ | $V_{IN}$ = 0 V to $V_{DD}$ |
| | | ±1.0 | µA max | |
| $V_{HYST}$, Input Hysteresis | 0.05 $V_{DD}$ | | V min | |
| $C_{IN}$, Input Capacitance | 6 | | pF typ | |
| LOGIC OUTPUT (SDA)[2] | | | | |
| $V_{OL}$, Output Low Voltage | | 0.4 | V max | $I_{SINK}$ = 3 mA |
| | | 0.6 | V max | $I_{SINK}$ = 6 mA |
| DYNAMIC CHARACTERISTICS[2] | | | | |
| $t_{ON}$ | 95 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, Test Circuit 5; |
| | | 140 | ns max | $V_{S1}$ = 3 V |
| $t_{OFF}$ | 85 | | ns typ | $V_{S1}$ = 3 V, $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 130 | ns max | Test Circuit 5 |
| Break-Before-Make Time Delay, $t_D$ | 8 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 1 | ns min | $V_{S1}$ = $V_{S2}$ = 3 V, Test Circuit 5 |
| Charge Injection | ±3 | | pC typ | $V_S$ = 2.5 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; |
| | | | | Test Circuit 6 |
| Off Isolation | –55 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz; |
| | –75 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; |
| | | | | Test Circuit 8 |
| Channel-to-Channel Crosstalk | –55 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz; |
| | –75 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; |
| | | | | Test Circuit 7 |
| –3 dB Bandwidth | | | | |
| ADG728 | 65 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, Test Circuit 8 |
| ADG729 | 100 | | MHz typ | |
| $C_S$ (OFF) | 13 | | pF typ | |
| $C_D$ (OFF) | | | | |
| ADG728 | 85 | | pF typ | |
| ADG729 | 42 | | pF typ | |
| $C_D$, $C_S$ (ON) | | | | |
| ADG728 | 96 | | pF typ | |
| ADG729 | 48 | | pF typ | |
| POWER REQUIREMENTS | | | | $V_{DD}$ = 5.5 V |
| $I_{DD}$ | 10 | | µA typ | Digital Inputs = 0 V or 5.5 V |
| | | 20 | µA max | |

NOTES
[1]Temperature range is as follows: B Version: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

# SPECIFICATIONS[1] ($V_{DD}$ = 3 V ± 10%, GND = 0 V, unless otherwise noted.)

| Parameter | B Version 25°C | B Version –40°C to +85°C | Unit | Test Conditions/Comments |
|---|---|---|---|---|
| ANALOG SWITCH | | | | |
| Analog Signal Range | | 0 V to $V_{DD}$ | V | |
| On Resistance ($R_{ON}$) | 6 | | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA; |
| | 11 | 12 | Ω max | Test Circuit 1 |
| On-Resistance Match Between | | 0.4 | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA |
| Channels ($\Delta R_{ON}$) | | 1.2 | Ω max | |
| On-Resistance Flatness ($R_{FLAT(ON)}$) | | 3.5 | Ω typ | $V_S$ = 0 V to $V_{DD}$, $I_S$ = 10 mA |
| LEAKAGE CURRENTS | | | | $V_{DD}$ = 3.3 V |
| Source OFF Leakage $I_S$ (OFF) | ±0.01 | | nA typ | $V_S$ = 3 V/1 V, $V_D$ = 1 V/3 V, Test Circuit 2 |
| | ±0.1 | ±0.3 | nA max | |
| Drain OFF Leakage $I_D$ (OFF) | ±0.01 | | nA typ | $V_D$ = 3 V/1 V, $V_D$ = 1 V/3 V, Test Circuit 3 |
| | ±0.1 | ±1 | nA max | |
| Channel ON Leakage $I_D$, $I_S$ (ON) | ±0.01 | | nA typ | $V_D$ = $V_S$ = 3 V/1 V, Test Circuit 4 |
| | ±0.1 | ±1 | nA max | |
| LOGIC INPUTS (A0, A1)[2] | | | | |
| Input High Voltage, $V_{INH}$ | | 2.0 | V min | |
| Input Low Voltage, $V_{INL}$ | | 0.4 | V max | |
| Input Current | | | | |
| $I_{INL}$ or $I_{INH}$ | 0.005 | | µA typ | |
| | | ±0.1 | µA max | |
| $C_{IN}$, Input Capacitance | 3 | | pF typ | |
| LOGIC INPUTS (SCL, SDA)[2] | | | | |
| Input High Voltage, $V_{INH}$ | | 0.7 $V_{DD}$ | V min | |
| | | $V_{DD}$ + 0.3 | V max | |
| Input Low Voltage, $V_{INL}$ | | –0.3 | V min | |
| | | 0.3 $V_{DD}$ | V max | |
| $I_{IN}$, Input Leakage Current | 0.005 | | µA typ | $V_{IN}$ = 0 V to $V_{DD}$ |
| | | ±1.0 | µA max | |
| $V_{HYST}$, Input Hysteresis | 0.05 $V_{DD}$ | | V min | |
| $C_{IN}$, Input Capacitance | 3 | | pF typ | |
| LOGIC OUTPUT (SDA)[2] | | | | |
| $V_{OL}$, Output Low Voltage | | 0.4 | V max | $I_{SINK}$ = 3 mA |
| | | 0.6 | V max | $I_{SINK}$ = 6 mA |
| DYNAMIC CHARACTERISTICS[2] | | | | |
| $t_{ON}$ | 130 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF, Test Circuit 5; |
| | | 200 | ns max | $V_{S1}$ = 2 V |
| $t_{OFF}$ | 115 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 180 | ns max | $V_S$ = 2 V, Test Circuit 5 |
| Break-Before-Make Time Delay, $t_D$ | 8 | | ns typ | $R_L$ = 300 Ω, $C_L$ = 35 pF; |
| | | 1 | ns min | $V_{S1}$ = $V_{S8}$ = 2 V, Test Circuit 5 |
| Charge Injection | ±3 | | pC typ | $V_S$ = 1.5 V, $R_S$ = 0 Ω, $C_L$ = 1 nF; |
| | | | | Test Circuit 6 |
| Off Isolation | –55 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz; |
| | –75 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; |
| | | | | Test Circuit 8 |
| Crosstalk | –55 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 10 MHz; |
| | –75 | | dB typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, f = 1 MHz; |
| | | | | Test Circuit 7 |
| –3 dB Bandwidth | | | | |
| ADG728 | 65 | | MHz typ | $R_L$ = 50 Ω, $C_L$ = 5 pF, Test Circuit 8 |
| ADG729 | 100 | | MHz typ | |
| $C_S$ (OFF) | 13 | | pF typ | |
| $C_D$ (OFF) | | | | |
| ADG728 | 85 | | pF typ | |
| ADG729 | 42 | | pF typ | |
| $C_D$, $C_S$ (ON) | | | | |
| ADG728 | 96 | | pF typ | |
| ADG729 | 48 | | pF typ | |
| POWER REQUIREMENTS | | | | $V_{DD}$ = 3.3 V |
| $I_{DD}$ | 10 | | µA typ | Digital Inputs = 0 V or 3.3 V |
| | | 20 | µA max | |

NOTES
[1]Temperature ranges are as follows: B Versions: –40°C to +85°C.
[2]Guaranteed by design, not subject to production test.
Specifications subject to change without notice.

# TIMING CHARACTERISTICS[1] ($V_{DD}$ = 2.7 V to 5.5 V. All specifications –40°C to +85°C, unless otherwise noted.)

| Parameter | Limit at $T_{MIN}$, $T_{MAX}$ | Unit | Conditions/Comments |
|---|---|---|---|
| $f_{SCL}$ | 400 | kHz max | SCL Clock Frequency |
| $t_1$ | 2.5 | ms min | SCL Cycle Time |
| $t_2$ | 0.6 | ms min | $t_{HIGH}$, SCL High Time |
| $t_3$ | 1.3 | ms min | $t_{LOW}$, SCL Low Time |
| $t_4$ | 0.6 | ms min | $t_{HD, STA}$, Start/Repeated Start Condition Hold Time |
| $t_5$ | 100 | ns min | $t_{SU, DAT}$, Data Setup Time |
| $t_6$[2] | 0.9 | ms max | $t_{HD, DAT}$, Data Hold Time |
| | 0 | ms min | |
| $t_7$ | 0.6 | ms min | $t_{SU, STA}$, Setup Time for Repeated Start |
| $t_8$ | 0.6 | ms min | $t_{SU, STO}$, Stop Condition Setup Time |
| $t_9$ | 1.3 | ms min | $t_{BUF}$, Bus Free Time Between a STOP Condition and a Start Condition |
| $t_{10}$ | 300 | ns max | $t_R$, Rise Time of Both SCL and SDA when Receiving |
| | $20 + 0.1C_b$[3] | ns min | |
| $t_{11}$ | 250 | ns max | $t_F$, Fall Time of SDA when Receiving |
| | 300 | ns max | $t_F$, Fall Time of SDA when Transmitting |
| | $20 + 0.1C_b$[3] | ns min | |
| $C_b$ | 400 | pF max | Capacitive Load for Each Bus Line |
| $t_{SP}$[4] | 50 | ns max | Pulsewidth of Spike Suppressed |

NOTES

[1]See Figure 1.

[2]A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the $V_{IH}$ min of the SCL signal) in order to bridge the undefined region of the falling edge of SCL.

[3]$C_b$ is the total capacitance of one bus line in pF. $t_R$ and $t_F$ measured between 0.3 $V_{DD}$ and 0.7 $V_{DD}$.

[4]Input filtering on both the SCL and SDA inputs suppress noise spikes which are less than 50 ns.

Specifications subject to change without notice.

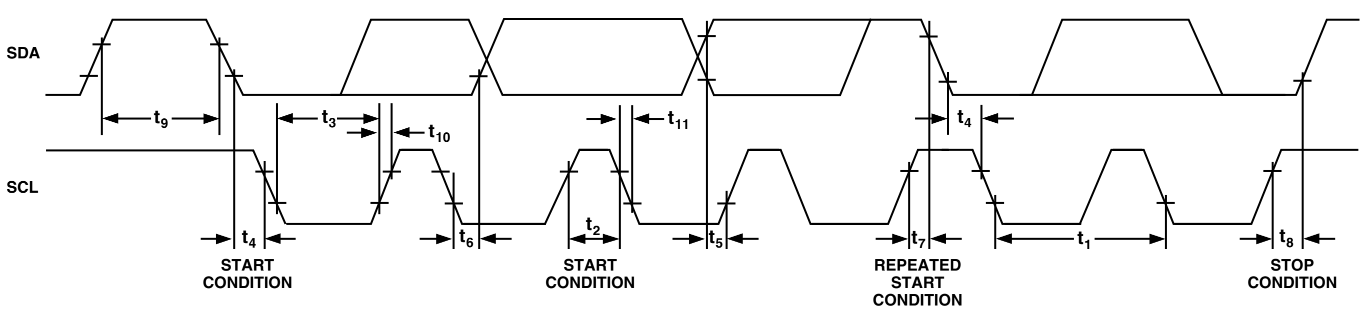


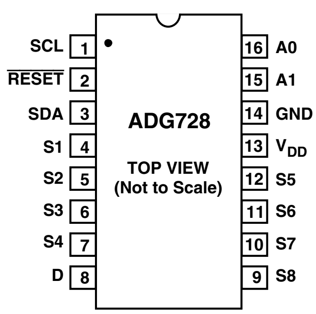

*Figure 1. 2-Wire Serial Interface Timing Diagram*

## PIN FUNCTION DESCRIPTIONS

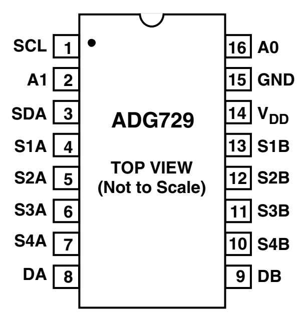
| ADG728 | ADG729 | Mnemonic | Function |
|---|---|---|---|
| 1 | 1 | SCL | Serial Clock Line. This is used in conjunction with the SDA line to clock data into the 8-bit input shift register. Clock rates of up to 400 kbit/s can be accommodated with this 2-wire serial interface. |
| 2 | | $\overline{\text{RESET}}$ | Active low control input that clears the input register and turns all switches to the OFF condition. |
| 3 | 3 | SDA | Serial Data Line. This is used in conjunction with the SCL line to clock data into the 8-bit input shift register during the write cycle and used to read back 1 byte of data during the read cycle. It is a bidirectional open-drain data line which should be pulled to the supply with an external pull-up resistor. |
| 4, 5, 6, 7 | 4, 5, 6, 7 | Sxx | Source. May be an input or output. |
| 8 | 8, 9 | Dx | Drain. May be an input or output. |
| 9, 10, 11, 12 | 10, 11, 12, 13 | Sxx | Source. May be an input or output. |
| 13 | 14 | $V_{DD}$ | Power Supply Input. These parts can be operated from a supply of 2.7 V to 5.5 V. |
| 14 | 15 | GND | Ground Reference. |
| 15 | 2 | A1 | Address Input. Sets the second least significant bit of the 7-bit slave address. |
| 16 | 16 | A0 | Address Input. Sets the least significant bit of the 7-bit slave address. |

## PIN CONFIGURATIONS

**ADG728**




**ADG729**




## ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADG728BRU | –40°C to +85°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADG729BRU | –40°C to +85°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |

## ABSOLUTE MAXIMUM RATINGS[1]

($T_A$ = 25°C unless otherwise noted.)

$V_{DD}$ to GND . . . . . . . . . . . . . . . . . . . . . . . . . –0.3 V to +7 V
Analog, Digital Inputs[2] . . . . . . . . . . –0.3 V to $V_{DD}$ + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D . . . . . . . . . . . . . . . . . . . . . . . . . 100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, Each S . . . . . . . . . . . . . . . . . . . . . 30 mA
Continuous Current D, ADG729 . . . . . . . . . . . . . . . . . 80 mA
Continuous Current D, ADG728 . . . . . . . . . . . . . . . . 120 mA
Operating Temperature Range
Industrial (B Version) . . . . . . . . . . . . . . . . –40°C to +85°C
Storage Temperature Range . . . . . . . . . . . . –65°C to +150°C
Junction Temperature . . . . . . . . . . . . . . . . . . . . . . . . . 150°C
TSSOP Package
$\theta_{JA}$ Thermal Impedance . . . . . . . . . . . . . . . . . . . 150.4°C/W
$\theta_{JC}$ Thermal Impedance . . . . . . . . . . . . . . . . . . . . 27.6°C/W
Lead Temperature, Soldering (10 seconds) . . . . . . . . . . 300°C
IR Reflow, Peak Temperature . . . . . . . . . . . . . . . . . . . . 220°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

[2]Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG728/ADG729 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.


## TERMINOLOGY

| | |
|---|---|
| $V_{DD}$ | Most Positive Power Supply Potential. |
| $I_{DD}$ | Positive Supply Current. |
| GND | Ground (0 V) Reference. |
| S | Source Terminal. May be an input or output. |
| D | Drain Terminal. May be an input or output. |
| $V_D$ ($V_S$) | Analog Voltage on Terminals D, S. |
| $R_{ON}$ | Ohmic Resistance between D and S. |
| $\Delta R_{ON}$ | On Resistance Match Between any Two Channels, i.e., $R_{ON}$max – $R_{ON}$min. |
| $R_{FLAT(ON)}$ | Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range. |
| $I_S$ (OFF) | Source Leakage Current with the Switch "OFF." |
| $I_D$ (OFF) | Drain Leakage Current with the Switch "OFF." |
| $I_D$, $I_S$ (ON) | Channel Leakage Current with the Switch "ON." |
| $V_{INL}$ | Maximum Input Voltage for Logic "0." |
| $V_{INH}$ | Minimum Input Voltage for Logic "1." |
| $I_{INL}$ ($I_{INH}$) | Input Current of the Digital Input. |
| $C_S$ (OFF) | "OFF" Switch Source Capacitance. Measured with reference to ground. |
| $C_D$ (OFF) | "OFF" Switch Drain Capacitance. Measured with reference to ground. |
| $C_D$, $C_S$ (ON) | "ON" Switch Capacitance. Measured with reference to ground. |
| $C_{IN}$ | Digital Input Capacitance. |
| $t_{ON}$ | Delay time between the 50% and 90% points of the STOP condition and the switch "ON" condition. |
| $t_{OFF}$ | Delay time between the 50% and 90% points of the STOP condition and the switch "OFF" condition. |
| $t_D$ | "OFF" time measured between the 80% points of both switches when switching from one switch to another. |
| Charge Injection | A measure of the glitch impulse transferred from the digital input to the analog output during switching. |
| Off Isolation | A measure of unwanted signal coupling through an "OFF" switch. |
| Crosstalk | A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance. |
| Bandwidth | The frequency at which the output is attenuated by 3 dBs. |
| On Response | The frequency response of the "ON" switch. |
| Insertion Loss | The loss due to the ON resistance of the switch. |

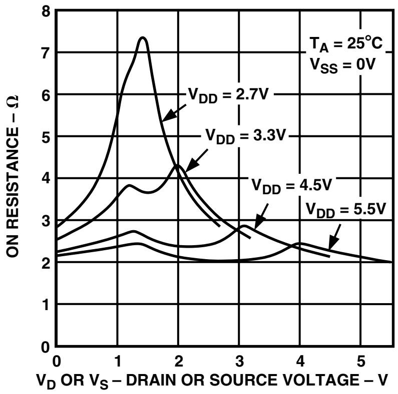



*Figure 2. On Resistance as a Function of $V_D$ ($V_S$) for Single Supply*

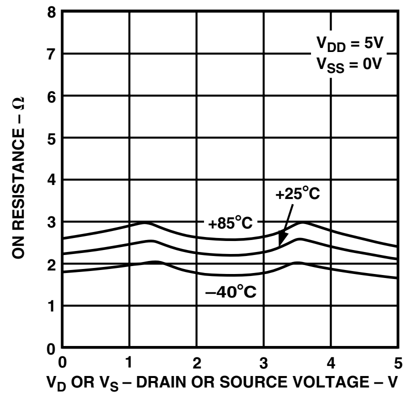



*Figure 3. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures, Single Supply*

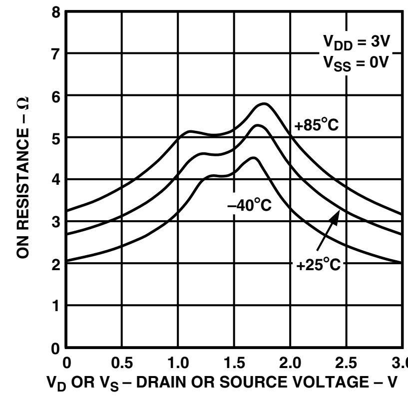



*Figure 4. On Resistance as a Function of $V_D$ ($V_S$) for Different Temperatures, Single Supply*

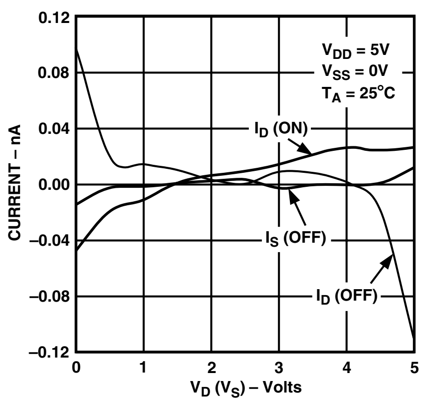



*Figure 5. Leakage Currents as a Function of $V_D$ ($V_S$)*

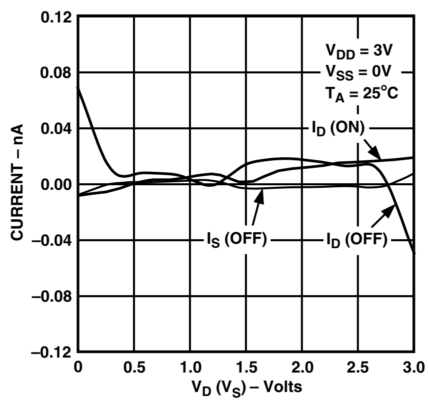



*Figure 6. Leakage Currents as a Function of $V_D$ ($V_S$)*

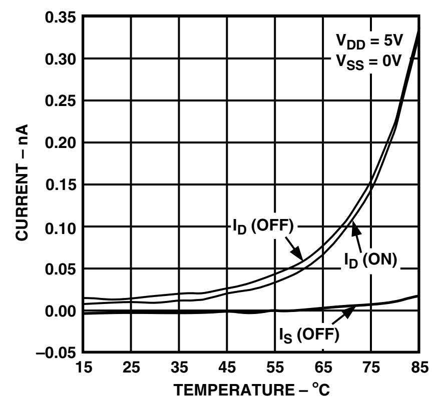



*Figure 7. Leakage Currents as a Function of Temperature*

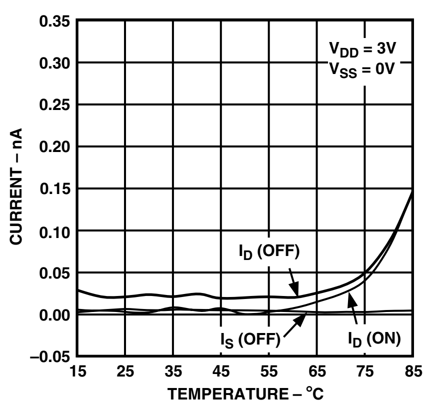



*Figure 8. Leakage Currents as a Function of Temperature*

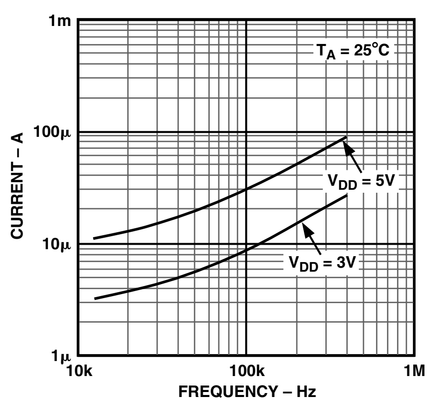



*Figure 9. Input Current vs. Switching Frequency*

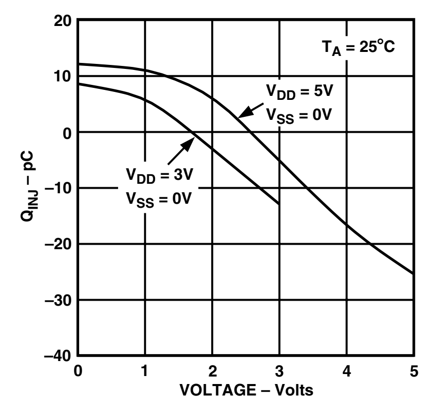



*Figure 10. Charge Injection vs. Source Voltage*

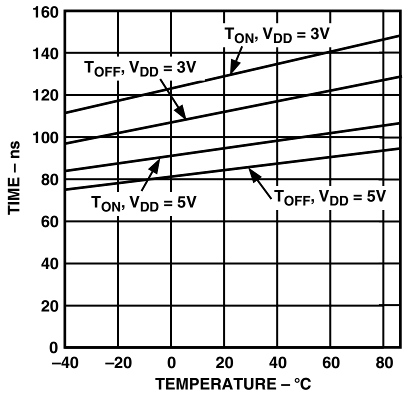



*Figure 11. $T_{ON}/T_{OFF}$ Times vs. Temperature*

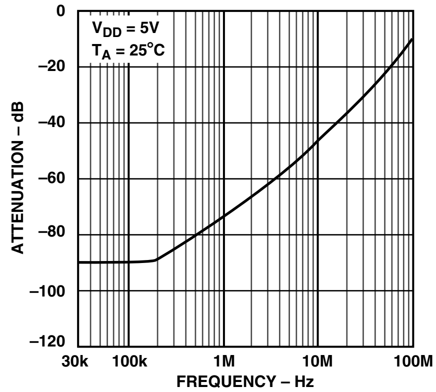



*Figure 12. Off Isolation vs. Frequency*

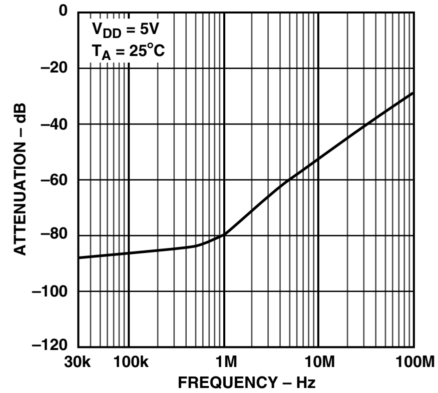



*Figure 13. Crosstalk vs. Frequency*

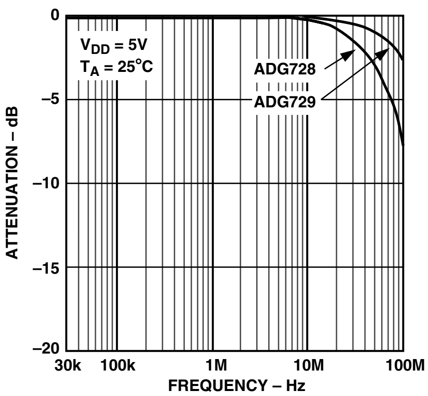



*Figure 14. On Response vs. Frequency*

## GENERAL DESCRIPTION

The ADG728 and ADG729 are serially controlled, 8-channel and dual 4-channel matrix switches respectively. While providing the normal multiplexing and demultiplexing functions, these devices also provide the user with more flexibility as to where their signal may be routed. Each bit of the serial word corresponds to one switch of the device. A Logic 1 in the particular bit position turns on the switch, while a Logic 0 turns the switch off. Because each switch is independently controlled by an individual bit, this provides the option of having any, all, or none of the switches ON. This feature may be particularly useful in the demultiplexing application where the user may wish to direct one signal from the drain to a number of outputs (sources). Care must be taken, however, in the multiplexing situation where a number of inputs may be shorted together (separated only by the small on resistance of the switch).

When changing the switch conditions, a new 8-bit word is written to the input shift register. Some of the bits may be the same as the previous write cycle, as the user may not wish to change the state of some switches. In order to minimize glitches on the output of these switches, the part cleverly compares the state of switches from the previous write cycle. If the switch is already in the ON condition, and is required to stay ON, there will be minimal glitches on the output of the switch.

## POWER-ON RESET

On power-up of the device, all switches will be in the OFF condition and the internal shift register is filled with zeros and will remain so until a valid write takes place.

## SERIAL INTERFACE

### 2-Wire Serial Bus

The ADG728/ADG729 are controlled via an $I^2C$ compatible serial bus. These parts are connected to this bus as a slave device (no clock is generated by the multiplexer).

The ADG728/ADG729 have different 7-bit slave addresses. The five MSBs of the ADG728 are 10011, while the MSBs of the ADG729 are 10001 and the two LSBs are determined by the state of the A0 and A1 pins.

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a START condition which is when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address followed by a $R/\overline{W}$ bit (this bit determines whether data will be read from or written to the slave device).

   The slave whose address corresponds to the transmitted address responds by pulling the SDA line low during the ninth clock pulse (this is termed the Acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its serial register. If the R/W bit is high, the master will read from the slave device. However, if the $R/\overline{W}$ bit is low, the master will write to the slave device.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a STOP condition is established by the master. A STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. In Write mode, the master will pull the SDA line high during the 10th clock pulse to establish a STOP condition. In Read mode, the master will issue a No Acknowledge for the ninth clock pulse (i.e., the SDA line remains high). The master will then bring the SDA line low before the tenth clock pulse and then high during the tenth clock pulse to establish a STOP condition.

See Figures 18 to 21 below for a graphical explanation of the serial interface.

A repeated write function gives the user flexibility to update the matrix switch a number of times after addressing the part only once. During the write cycle, each data byte will update the configuration of the switches. For example, after the matrix switch has acknowledged its address byte, and receives one data byte, the switches will update after the data byte, if another data byte is written to the matrix switch while it is still the addressed slave device, this data byte will also cause an switch configuration update. Repeat read of the matrix switch is also allowed.

## INPUT SHIFT REGISTER

The input shift register is eight bits wide. Figure 15 illustrates the contents of the input shift register. Data is loaded into the device as an 8-bit word under the control of a serial clock input, SCL. The timing diagram for this operation is shown in Figure 1. The 8-bit word consists of eight data bits each controlling one switch. MSB (Bit 7) is loaded first.

| DB7 (MSB) | | | | | | | DB0 (LSB) |
|---|---|---|---|---|---|---|---|
| S8 | S7 | S6 | S5 | S4 | S3 | S2 | S1 |
| ← DATA BITS → | | | | | | | |

*Figure 15. ADG728/ADG729 Input Shift Register Contents*

### WRITE OPERATION

When writing to the ADG728/ADG729, the user must begin with an address byte and R/$\overline{W}$ bit, after which the switch will acknowledge that it is prepared to receive data by pulling SDA low. This address byte is followed by the 8-bit word. The write operations for each matrix switch are shown in the figures below.

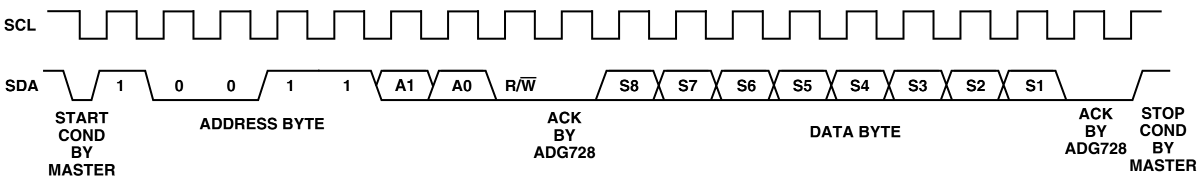



*Figure 16. ADG728 Write Sequence*

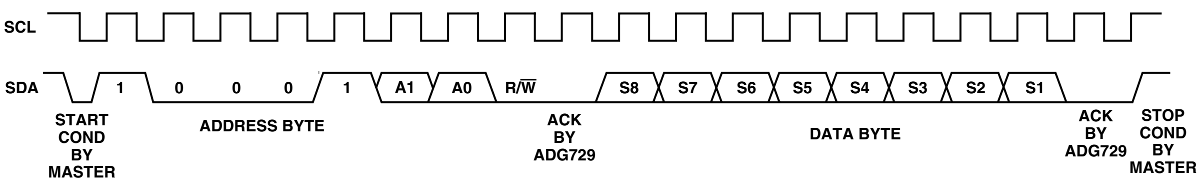



*Figure 17. ADG729 Write Sequence*

### READ OPERATION

When reading data back from the ADG728/ADG729, the user must begin with an address byte and R/$\overline{W}$ bit, after which the matrix switch will acknowledge that it is prepared to transmit data by pulling SDA low. The readback operation is a single byte that consists of the eight data bits in the input register. The read operations for each part are shown in Figures 18 and 19.

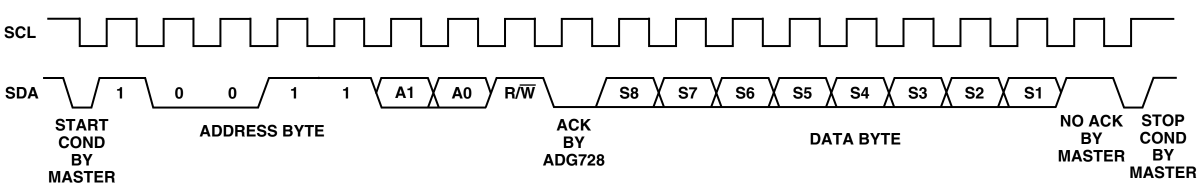



*Figure 18. ADG728 Readback Sequence*

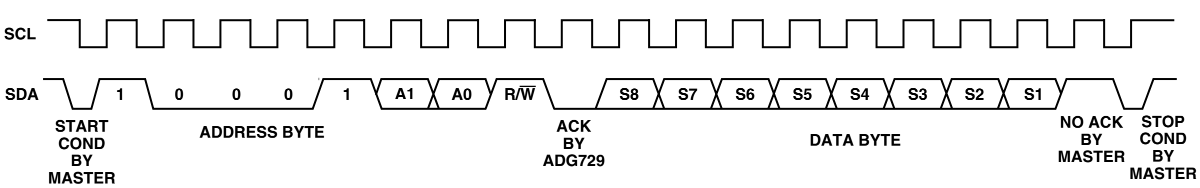



*Figure 19. ADG729 Readback Sequence*

**MULTIPLE DEVICES ON ONE BUS**

Figure 20 shows four ADG728s devices on the same serial bus. Each has a different slave address since the state of their A0 and A1 pins is different. This allows each Matrix Switch to be written to or read from independently. Because the ADG729 has a different address to the ADG728, it would be possible for four of each of these devices to be connected to the same bus.

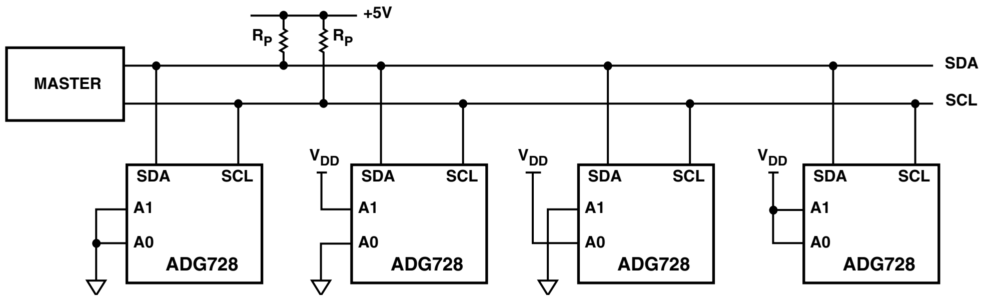
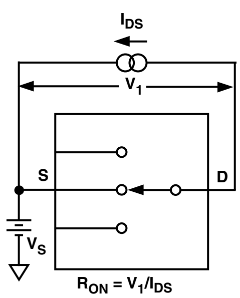
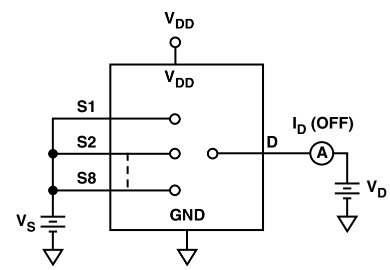



*Figure 20. Multiple ADG728s on the Same Bus*

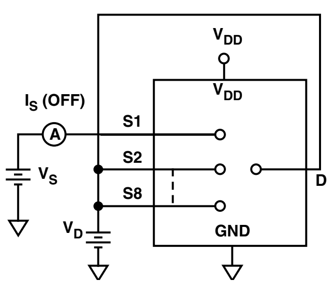
**TEST CIRCUITS**



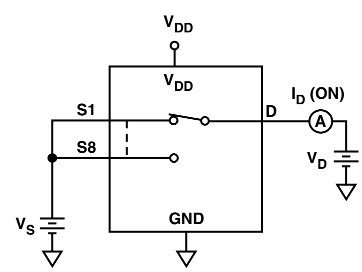

*Test Circuit 1. On Resistance*



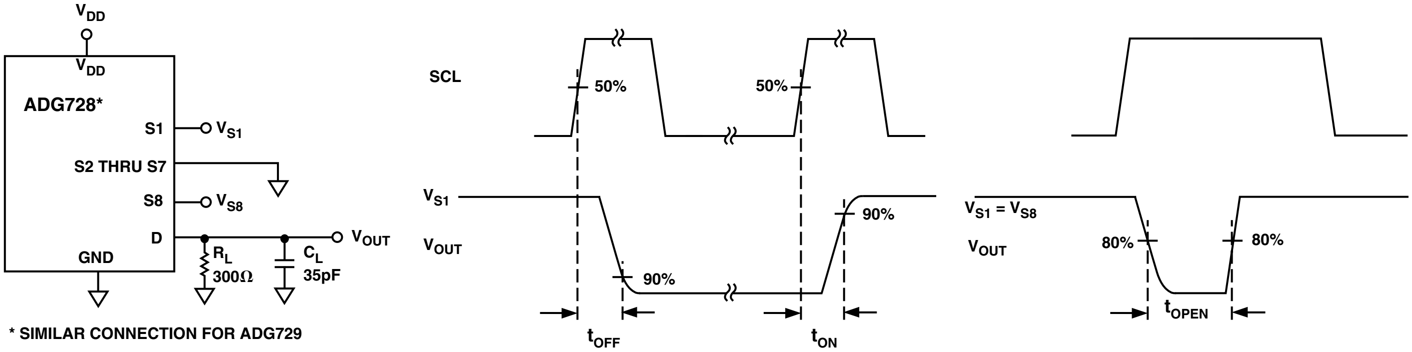

*Test Circuit 3. $I_S$ (OFF)*



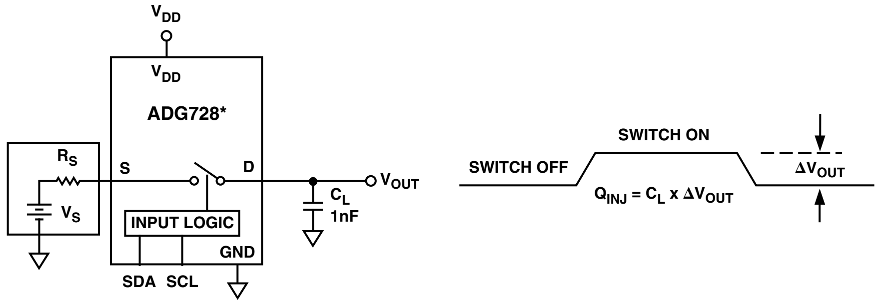

*Test Circuit 2. $I_D$ (OFF)*




*Test Circuit 4. $I_D$ (ON)*

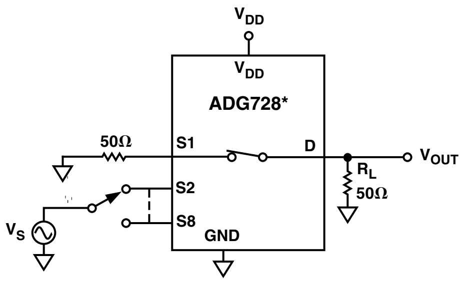



*Test Circuit 5. Switching Times and Break-Before-Make Times*




* SIMILAR CONNECTION FOR ADG729

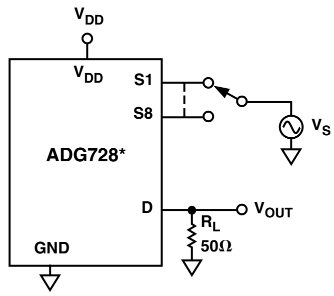
*Test Circuit 6. Charge Injection*




* SIMILAR CONNECTION FOR ADG729

CHANNEL-TO-CHANNEL CROSSTALK = $20LOG_{10}(V_{OUT}/V_S)$

*Test Circuit 7. Channel-to-Channel Crosstalk*




*SIMILAR CONNECTION FOR ADG729

S1 IS SWITCHED OFF FOR OFF ISOLATION MEASUREMENTS AND ON FOR BANDWIDTH MEASUREMENTS

OFF ISOLATION = $20LOG_{10}(V_{OUT}/V_S)$

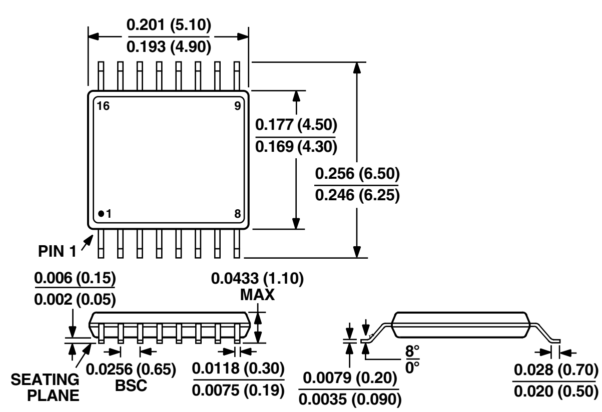
INSERTION LOSS = $20LOG_{10}\left(\frac{V_{OUT} \text{ WITH SWITCH}}{V_{OUT} \text{ WITHOUT SWITCH}}\right)$

*Test Circuit 8. Off Isolation and Bandwidth*

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 16-Lead TSSOP (RU-16)




C3833–2.5–4/00 (rev. 0) 01002

PRINTED IN U.S.A.