# CMOS
# 220 MHz Pseudo-Color Graphics Triple 10-Bit Video RAM-DAC

# ADV7151

## FEATURES

**220 MHz, 10-Bit (30-Bit Gamma Corrected) Pseudo Color (Indexed-Color)**
**Triple 10-Bit "Gamma Correcting" D/A Converters**
**Triple 256 × 10 (256 × 30) Color Palette RAM (256 Colors out of 1 Billion)**
**On-Chip Clock Control Circuit**
**Palette Priority Select Registers**
**RS-343A/RS-170 Compatible Analog Outputs**
**TTL Compatible Digital Inputs**
**Standard MPU I/O Interface**
**10-Bit Parallel Structure**
**8+2 Byte Structure**
**Multiplexed Pixel Input Ports; 1:1, 2:1, 4:1**
**+5 V CMOS Monolithic Construction**
**100-Lead Plastic Quad Flatpack (QFP)**
**Thermally Enhanced to Achieve $\theta_{JC} < 1.0°C/W$**

## MODES OF OPERATION

**8-Bit Pseudo Color**
**@ 220 MHz**
**@ 170 MHz**
**@ 135 MHz**
**@ 110 MHz**
**@ 85 MHz**

## APPLICATIONS

**High Resolution Graphics**

## GENERAL DESCRIPTION

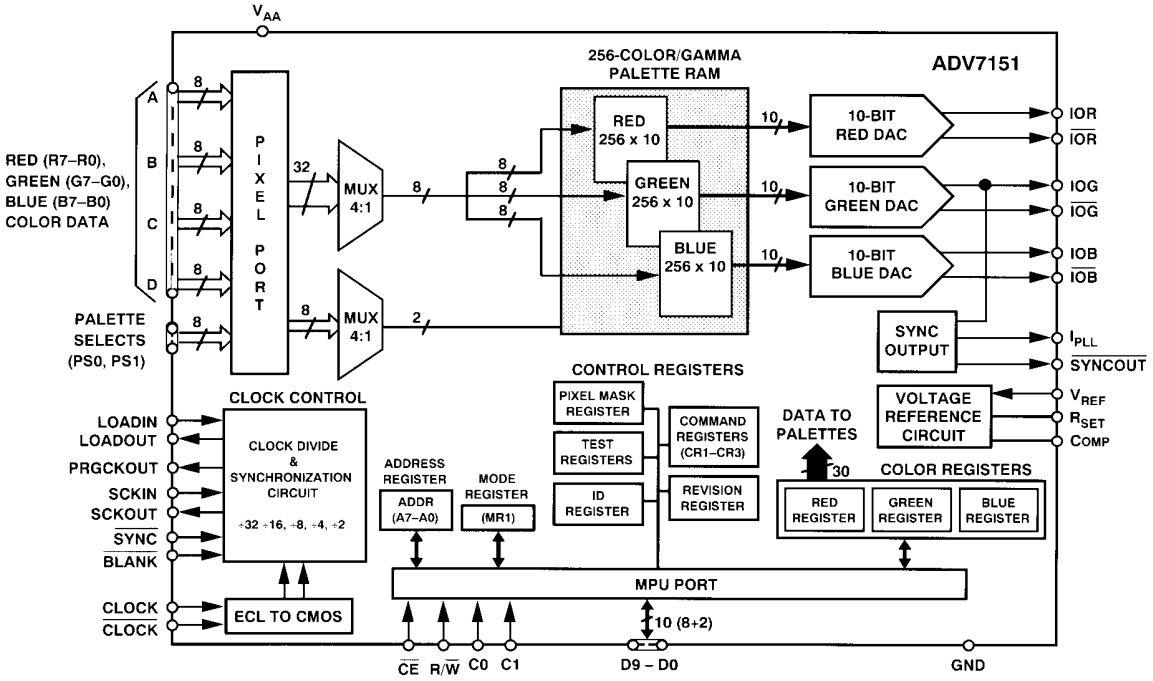
The ADV7151 (ADV*) is a complete analog output, Video RAM-DAC on a single CMOS monolithic chip. The part is specifically designed for use in high performance, color graphics workstations. The ADV7151 integrates a number of graphic functions onto one device allowing 8-bit Pseudo-Color (Indexed-Color) operation at the maximum screen update rate of 220 MHz.

The device consists of three, high speed, 10-bit, video D/A converters (RGB), three 256 × 10 (one 256 × 30) color look-up tables, palette priority selects, a pixel input data multiplexer/serializer and a clock generator/divider circuit. The ADV7151 is capable of 1:1, 2:1 and 4:1 multiplexing. The on-board palette priority select inputs enable multiple palette devices to be connected together for use in multipalette and window applications. The part is controlled and programmed through the microprocessor (MPU) port. The part also contains a number of on-board test registers, associated with self diagnostic testing of the device.

*ADV is a registered trademark of Analog Devices, Inc.

*(Continued on page 12)*

## FUNCTIONAL BLOCK DIAGRAM




REV. A



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# ADV7151—SPECIFICATIONS ($V_{AA}$[1] = +5 V; $V_{REF}$ = +1.235 V; $R_{SET}$ = 280 Ω. IOR, IOG, IOB ($R_L$ = 37.5 Ω, $C_L$ = 10 pF); $\overline{IOR}$, $\overline{IOG}$, $\overline{IOB}$ = GND. All specifications $T_{MIN}$ to $T_{MAX}$[2] unless otherwise noted.)

| Parameter | All Versions | Unit | Test Conditions/Comments |
|---|---|---|---|
| STATIC PERFORMANCE | | | |
| Resolution (Each DAC) | 10 | Bits | |
| Accuracy (Each DAC) | | | |
| Integral Nonlinearity | ±1 | LSB max | |
| Differential Nonlinearity | ±1 | LSB max | Guaranteed Monotonic |
| Gray Scale Error | ±5 | % Gray Scale max | |
| Coding | | Binary | |
| DIGITAL INPUTS (Excluding CLOCK, $\overline{CLOCK}$) | | | |
| Input High Voltage, $V_{INH}$ | 2 | V min | |
| Input Low Voltage, $V_{INL}$ | 0.8 | V max | |
| Input Current, $I_{IN}$ | ±10 | μA max | $V_{IN}$ = 0.4 V or 2.4 V |
| Input Capacitance, $C_{IN}$ | 10 | pF typ | |
| CLOCK INPUTS (CLOCK, $\overline{CLOCK}$) | | | |
| Input High Voltage, $V_{INH}$ | $V_{AA}$ – 1.0 | V min | |
| Input Low Voltage, $V_{INL}$ | $V_{AA}$ – 1.6 | V max | |
| Input Current, $I_{IN}$ | ±10 | μA max | $V_{IN}$ = 0.4 V or 2.4 V |
| Input Capacitance, $C_{IN}$ | 10 | pF typ | |
| DIGITAL OUTPUTS | | | |
| Output High Voltage, $V_{OH}$ | 2.4 | V min | $I_{SOURCE}$ = 400 μA |
| Output Low Voltage, $V_{OL}$ | 0.4 | V max | $I_{SINK}$ = 3.2 mA |
| Floating-State Leakage Current | 20 | μA max | |
| Floating-State Output Capacitance | 20 | pF typ | |
| ANALOG OUTPUTS | | | |
| Gray Scale Current Range | 15 | mA min | |
| | 22 | mA max | |
| Output Current | | | |
| White Level Relative to Blank | 17.69 | mA min | Typically 19.05 mA |
| | 20.40 | mA max | |
| White Level Relative to Black | 16.74 | mA min | Typically 17.62 mA |
| | 18.50 | mA max | |
| Black Level Relative to Blank | 0.95 | mA min | Typically 1.44 mA |
| | 1.90 | mA max | |
| Blank Level on IOR, IOB | 0 | μA min | Typically 5 μA |
| | 50 | μA max | |
| Blank Level on IOG | 6.29 | mA min | Typically 7.62 mA |
| | 8.96 | mA max | |
| Sync Level on IOG | 0 | μA min | Typically 5 μA |
| | 50 | μA max | |
| LSB Size | 17.22 | μA typ | |
| DAC-to-DAC Matching | 2 | % max | Typically 1% |
| Output Compliance, $V_{OC}$ | 0 | V min | |
| | +1.4 | V max | |
| Output Impedance, $R_{OUT}$ | 100 | kΩ typ | |
| Output Capacitance, $C_{OUT}$ | 30 | pF max | $I_{OUT}$ = 0 mA |
| VOLTAGE REFERENCE | | | |
| Voltage Reference Range, $V_{REF}$ | 1.14/1.26 | V min/V max | $V_{REF}$ = 1.235 V for Specified Performance |
| Input Current, $I_{VREF}$ | +5 | μA typ | |
| POWER REQUIREMENTS | | | |
| $V_{AA}$ | 5 | V nom | |
| $I_{AA}$[3] | 400 | mA max | 220 MHz Parts |
| $I_{AA}$ | 370 | mA max | 170 MHz Parts |
| $I_{AA}$ | 350 | mA max | 135 MHz Parts |
| $I_{AA}$ | 330 | mA max | 110 MHz Parts |
| $I_{AA}$ | 315 | mA max | 85 MHz Parts |
| Power Supply Rejection Ratio | 0.5 | %/% max | Typically 0.12%/%: COMP = 0.1 μF |
| DYNAMIC PERFORMANCE | | | |
| Clock and Data Feedthrough[4, 5] | –30 | dB typ | |
| Glitch Impulse | 50 | pV secs typ | |
| DAC-to-DAC Crosstalk[6] | –23 | dB typ | |

NOTES
[1]±5% for all versions.
[2]Temperature range ($T_{MIN}$ to $T_{MAX}$): 0°C to +70°C; $T_J$ (Silicon Junction Temperature) ≤ 100°C.
[3]Pixel Port is continuously clocked with data corresponding to a linear ramp. $T_J$ = 100°C.
[4]Clock and data feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough.
[5]TTL input values are 0 to 3 volts, with input rise/fall times ≤3 ns, measured the 10% and 90% points. Timing reference points at 50% for inputs and outputs.
[6]DAC-to-DAC crosstalk is measured by holding one DAC high while the other two are making low-to-high and high-to-low transitions.
Specifications subject to change without notice.

# TIMING CHARACTERISTICS[1] ($V_{AA}$[2] = +5 V; $V_{REF}$ = +1.235 V; $R_{SET}$ = 280 Ω. IOR, IOG, IOB ($R_L$ = 37.5 Ω, $C_L$ = 10 pF); $\overline{IOR}$, $\overline{IOG}$, $\overline{IOB}$ = GND. All specifications $T_{MIN}$ to $T_{MAX}$[3] unless otherwise noted.)

## CLOCK CONTROL AND PIXEL PORT[4]

| Parameter | 220 MHz Version | 170 MHz Version | 135 MHz Version | 110 MHz Version | 85 MHz Version | Units | Conditions/Comments |
|---|---|---|---|---|---|---|---|
| $f_{CLOCK}$ | 220 | 170 | 135 | 110 | 85 | MHz max | Pixel CLOCK Rate |
| $t_1$ | 4.55 | 5.88 | 7.4 | 9.1 | 11.77 | ns min | Pixel CLOCK Cycle Time |
| $t_2$ | 2 | 2.5 | 3.2 | 4 | 4 | ns min | Pixel CLOCK High Time |
| $t_3$ | 2 | 2.5 | 3 | 4 | 4 | ns min | Pixel CLOCK Low Time |
| $t_4$ | 10 | 10 | 10 | 10 | 10 | ns max | Pixel CLOCK to LOADOUT Delay |
| $f_{LOADIN}$ | | | | | | | LOADIN Clocking Rate |
| 1:1 Multiplexing | 110 | 110 | 110 | 110 | 85 | MHz max | |
| 2:1 Multiplexing | 110 | 85 | 67.5 | 55 | 42.5 | MHz max | |
| 4:1 Multiplexing | 55 | 42.5 | 42.5 | 33.75 | 27.5 | 21.25 | MHz max |
| $t_5$ | | | | | | | LOADIN Cycle Time |
| 1:1 Multiplexing | 9.1 | 9.1 | 9.1 | 9.1 | 11.76 | ns min | |
| 2:1 Multiplexing | 9.1 | 11.76 | 14.8 | 18.18 | 23.53 | ns min | |
| 4:1 Multiplexing | 18.18 | 23.53 | 29.63 | 36.36 | 47.1 | ns min | |
| $t_6$ | | | | | | | LOADIN High Time |
| 1:1 Multiplexing | 4 | 4 | 4 | 4 | 4 | ns min | |
| 2:1 Multiplexing | 4 | 5 | 6 | 8 | 9 | ns min | |
| 4:1 Multiplexing | 8 | 9 | 12 | 15 | 18 | ns min | |
| $t_7$ | | | | | | | LOADIN Low Time |
| 1:1 Multiplexing | 4 | 4 | 4 | 4 | 4 | ns min | |
| 2:1 Multiplexing | 4 | 5 | 6 | 8 | 9 | ns min | |
| 4:1 Multiplexing | 8 | 9 | 12 | 15 | 18 | ns min | |
| $t_8$ | 0 | 0 | 0 | 0 | 0 | ns min | Pixel Data Setup Time |
| $t_9$ | 5 | 5 | 5 | 5 | 5 | ns min | Pixel Data Hold Time |
| $t_{10}$ | 0 | 0 | 0 | 0 | 0 | ns min | LOADOUT to LOADIN Delay |
| $\tau$-$t_{11}$[5] | $\tau$-5 | $\tau$-5 | $\tau$-5 | $\tau$-5 | $\tau$-4 | ns max | LOADOUT to LOADIN Delay |
| $t_{PD}$[6] | | | | | | | Pipeline Delay |
| 1:1 Multiplexing | 5 | 5 | 5 | 5 | 5 | CLOCKs | (1 × CLOCK = $t_1$) |
| 2:1 Multiplexing | 6 | 6 | 6 | 6 | 6 | CLOCKs | |
| 4:1 Multiplexing | 8 | 8 | 8 | 8 | 8 | CLOCKs | |
| $t_{12}$ | 10 | 10 | 10 | 10 | 10 | ns max | Pixel CLOCK to PRGCKOUT Delay |
| $t_{13}$ | 5 | 5 | 5 | 5 | 5 | ns max | $\overline{SCKIN}$ to SCKOUT Delay |
| $t_{14}$ | 5 | 5 | 5 | 5 | 5 | ns min | $\overline{BLANK}$ to SCKIN Setup Time |
| $t_{15}$ | 1 | 1 | 1 | 1 | 1 | ns min | $\overline{BLANK}$ to SCKIN Hold Time |

## ANALOG OUTPUTS[7]

| Parameter | 220 MHz Version | 170 MHz Version | 135 MHz Version | 110 MHz Version | 85 MHz Version | Units | Conditions/Comments |
|---|---|---|---|---|---|---|---|
| $t_{16}$ | 15 | 15 | 15 | 15 | 15 | ns typ | Analog Output Delay |
| $t_{17}$ | 1 | 1 | 1 | 1 | 1 | ns typ | Analog Output Rise/Fall Time |
| $t_{18}$ | 15 | 15 | 15 | 15 | 15 | ns typ | Analog Output Transition Time |
| $t_{SK}$ | 2 | 2 | 2 | 2 | 2 | ns max | Analog Output Skew (IOR, IOG, IOB) |
| | 0 | 0 | 0 | 0 | 0 | ns typ | |

## MPU PORT[8, 9]

| Parameter | 220 MHz Version | 170 MHz Version | 135 MHz Version | 110 MHz Version | 85 MHz Version | Units | Conditions/Comments |
|---|---|---|---|---|---|---|---|
| $t_{19}$ | 3 | 3 | 3 | 3 | 3 | ns min | R/$\overline{W}$, C0, C1 to $\overline{CE}$ Setup Time |
| $t_{20}$ | 10 | 10 | 10 | 10 | 10 | ns min | R/$\overline{W}$, C0, C1 to $\overline{CE}$ Hold Time |
| $t_{21}$ | 45 | 45 | 45 | 45 | 45 | ns min | $\overline{CE}$ Low Time |
| $t_{22}$ | 25 | 25 | 25 | 25 | 25 | ns min | $\overline{CE}$ High Time |
| $t_{23}$[8] | 5 | 5 | 5 | 5 | 5 | ns min | $\overline{CE}$ Asserted to Databus Driven |
| $t_{24}$[9] | 45 | 45 | 45 | 45 | 45 | ns max | $\overline{CE}$ Asserted to Data Valid |
| $t_{25}$[9] | 20 | 20 | 20 | 20 | 20 | ns max | $\overline{CE}$ Disabled to Databus Three-Stated |
| | 5 | 5 | 5 | 5 | 5 | ns min | |
| $t_{26}$ | 20 | 20 | 20 | 20 | 20 | ns min | Write Data (D0–D9) Setup Time |
| $t_{27}$ | 5 | 5 | 5 | 5 | 5 | ns min | Write Data (D0–D9) Hold Time |

NOTES

[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤ 3 ns, measured between the 10% and 90% points. ECL inputs (CLOCK, $\overline{\text{CLOCK}}$) are $V_{AA}$–0.8 V to $V_{AA}$–1.8 V, with input rise/fall times ≤ 2 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤ 10 pF. Databus (D0–D9) loaded as shown in Figure 1. Digital output load for LOADOUT, PRGCKOUT and SCKOUT ≤ 30 pF.

[2]±5% for all versions.

[3]Temperature range ($T_{MIN}$ to $T_{MAX}$); 0°C to +70°C; $T_J$ (Silicon Junction Temperature) ≤ 100°C.

[4]Pixel Port consists of the following inputs: Pixel Inputs: P0–P7 [A, B, C, D]; Palette Selects: PS0 [A, B, C, D] PS1 [A, B, C, D]; Pixel Controls: $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$; Clock Inputs: CLOCK, $\overline{\text{CLOCK}}$, LOADIN, SCKIN; Clock Outputs: LOADOUT, PRGCKOUT, SCKOUT.

[5]$\tau$ is the LOADOUT Cycle Time and is a function of the Pixel CLOCK Rate and the Multiplexing Mode: 1:1 multiplexing; $\tau$ = CLOCK = $t_1$ ns: 2:1 multiplexing; $\tau$ = CLOCK × 2 = 2 × $t_1$ ns: 4:1 multiplexing; $\tau$ = CLOCK × 4 = 4 × $t_1$ ns.

[6]These fixed values for Pipeline Delay are valid under conditions where $t_{10}$ and $\tau$-$t_{11}$ are met. If either $t_{10}$ or $\tau$-$t_{11}$ are not met, the part will operate but the Pipeline Delay is increased by an additional 2 Clock Cycles for 2:1 Mode and is increased by an additional 4 Clock Cycles for 4:1 Mode, after calibration is performed.

[7]Output delay measured from the 50% point of the rising edge of CLOCK to the 50% point of full-scale transition. Output rise/fall time measured between the 10% and 90% points of full-scale transition. Transition time measured from the 50% point of full-scale transition to the output remaining within ±1 LSB. (Transition time does not include clock and data feedthrough.)

[8]$t_{23}$ and $t_{24}$ are measured with the load circuit of Figure 1 and defined as the time required for an output to cross 0.4 V or 2.4 V.

[9]$t_{25}$ is derived from the measured time taken by the data outputs to change by 0.5 V when loaded with the circuit of Figure 1. The measured number is then extrapolated back to remove the effects of charging the 100 pF capacitor. This means that the time, $t_{25}$, quoted in the Timing Characteristics is the true value for the device and as such is independent of external databus loading capacitances.

Specifications subject to change without notice.

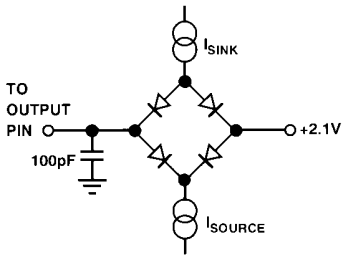



*Figure 1. Load Circuit for Databus Access and Relinquish Times*

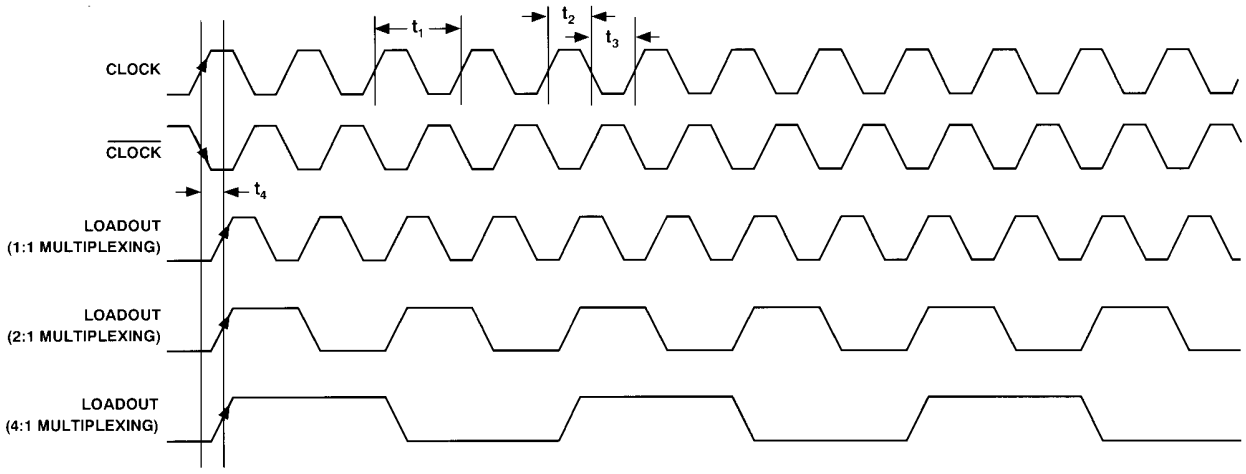
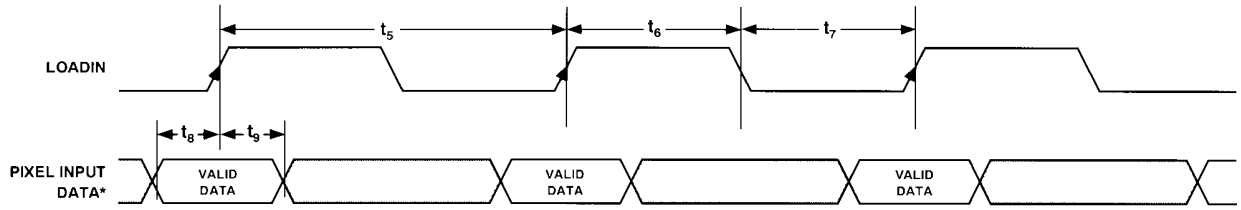
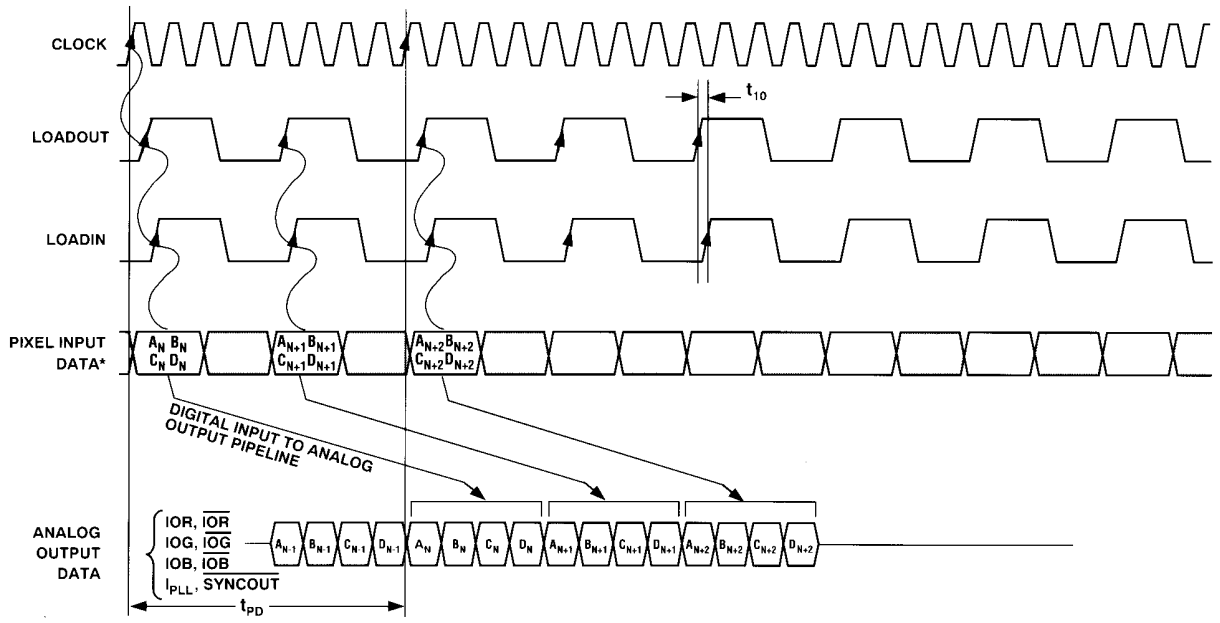



*Figure 2. LOADOUT vs. Pixel Clock Input (CLOCK, $\overline{\text{CLOCK}}$)*



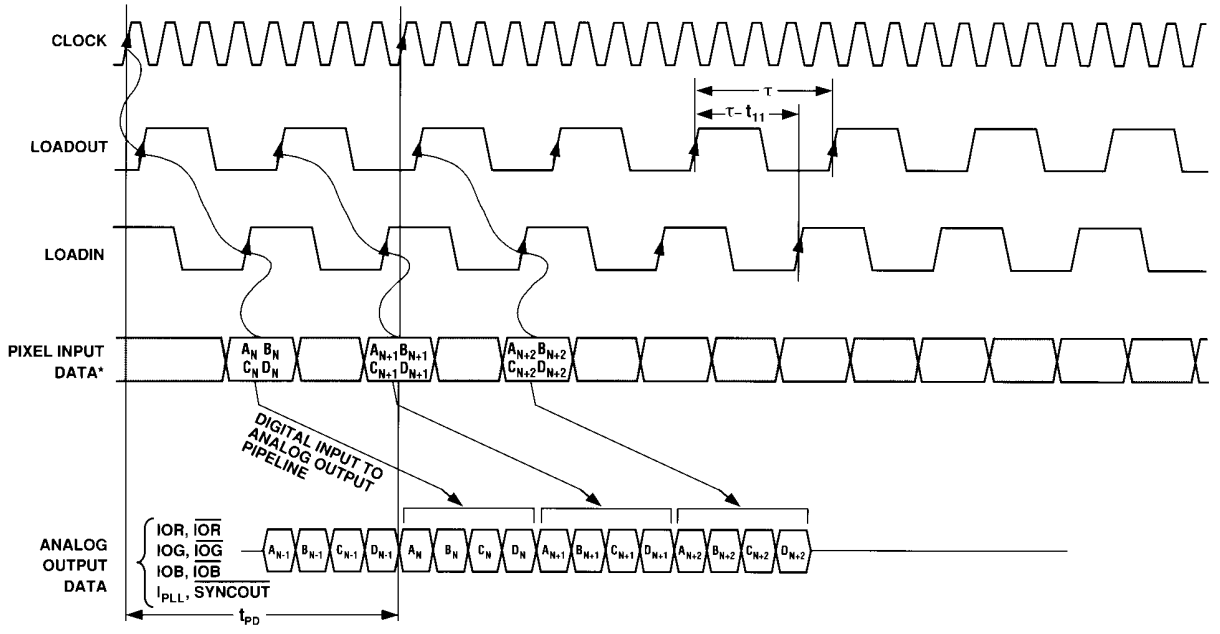

*INCLUDES PIXEL DATA (P0–P7); PALETTE SELECT INPUTS (PS0-PS1); $\overline{\text{SYNC}}$; $\overline{\text{BLANK}}$

*Figure 3. LOADIN vs. Pixel Input Data*




*INCLUDES PIXEL DATA (P0–P7); PALETTE SELECT INPUTS (PS0-PS1); $\overline{\text{SYNC}}$; $\overline{\text{BLANK}}$

*Figure 4. Pixel Input to Analog Output Pipeline with Minimum LOADOUT to LOADIN Delay (4:1 Multiplex Mode)*




*INCLUDES PIXEL DATA (P0–P7); PALETTE SELECT INPUTS (PS0-PS1); $\overline{\text{SYNC}}$; $\overline{\text{BLANK}}$

*Figure 5. Pixel Input to Analog Output Pipeline with Maximum LOADOUT to LOADIN Delay (4:1 Multiplex Mode)*

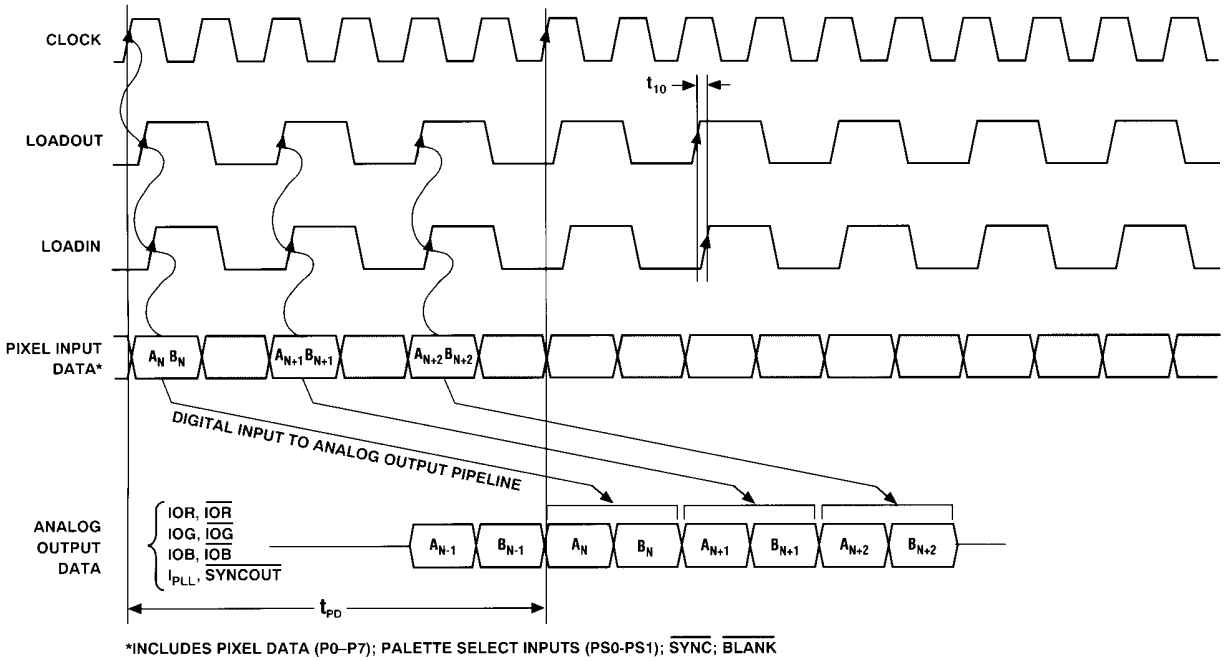



*Figure 6. Pixel Input to Analog Output Pipeline with Minimum LOADOUT to LOADIN Delay (2:1 Multiplex Mode)*

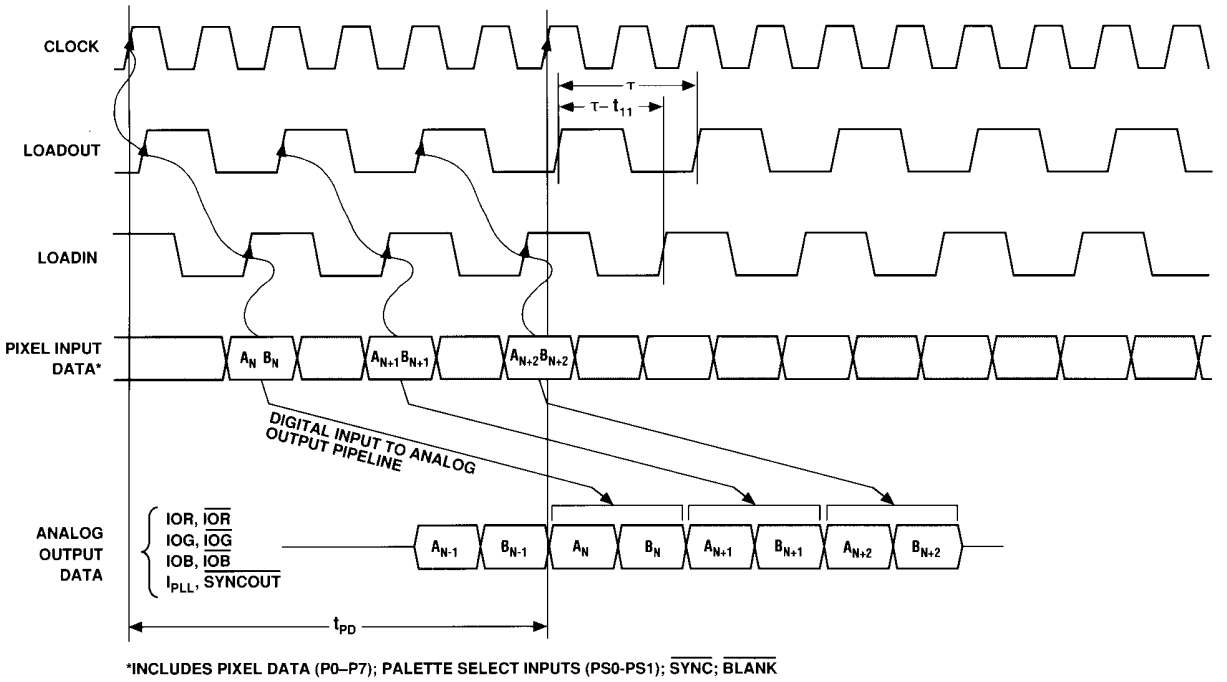



*Figure 7. Pixel Input to Analog Output Pipeline with Maximum LOADOUT to LOADIN Delay (2:1 Multiplex Mode)*

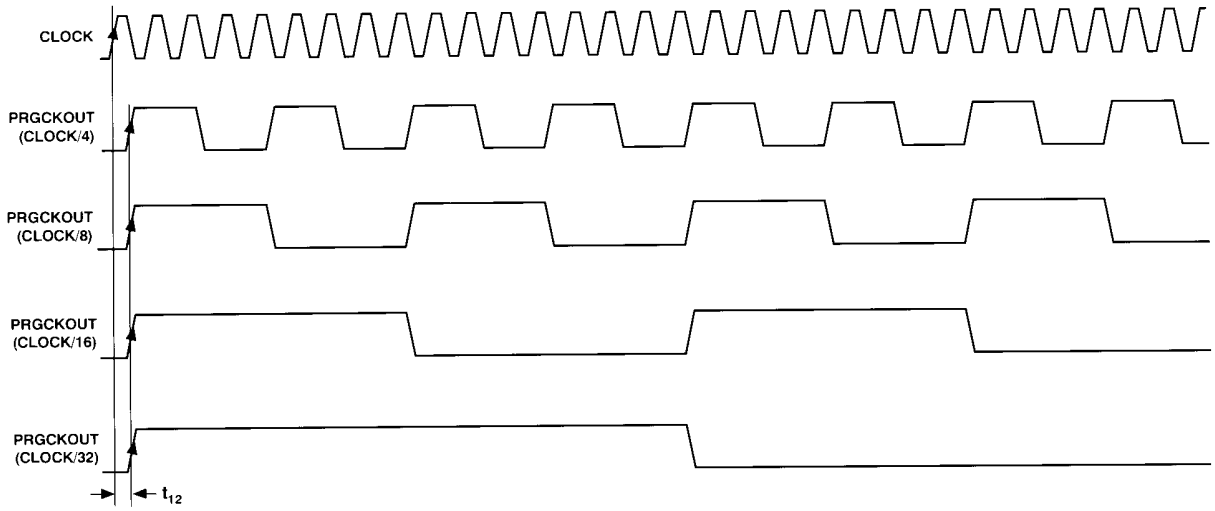



*Figure 8. Pixel Clock Input vs. Programmable Clock Output (PRGCKOUT)*

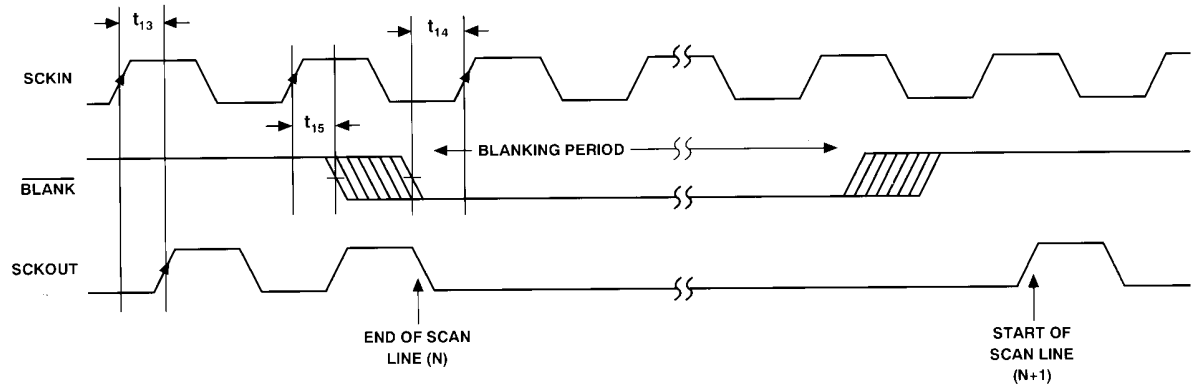



*Figure 9. Video Data Shift Clock Input (SCKIN) and BLANK vs. Video Data Shift Clock Output (SCKOUT)*

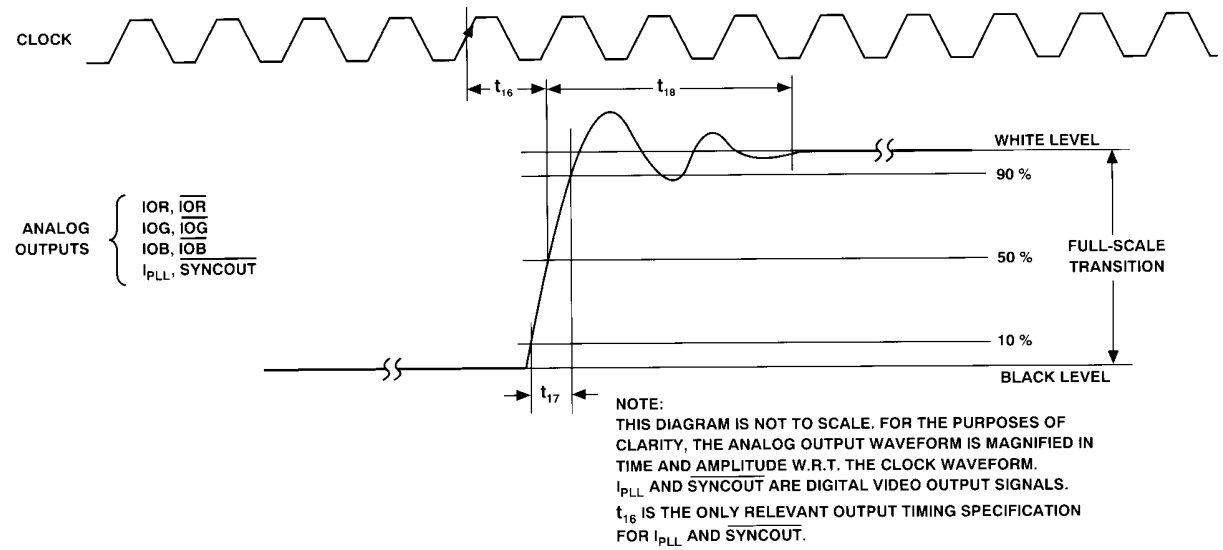



*Figure 10. Analog Output Response vs. CLOCK*

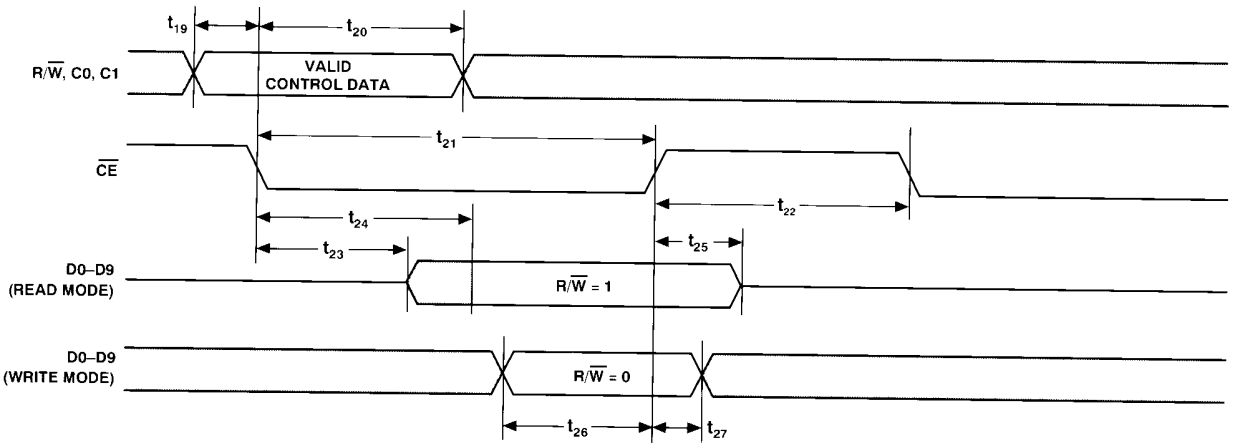



*Figure 11. Microprocessor Port (MPU) Interface Timing*

# RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Power Supply | $V_{AA}$ | 4.75 | 5.00 | 5.25 | Volts |
| Ambient Operating Temperature | $T_A$ | 0 | | +70 | °C |
| Reference Voltage | $V_{REF}$ | 1.14 | 1.235 | 1.26 | Volts |
| Output Load | $R_L$ | | 37.5 | | Ω |

**CAUTION**

ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.


**ABSOLUTE MAXIMUM RATINGS***

$V_{AA}$ to GND . . . . . 7 V
Voltage on Any Digital Pin . . . GND − 0.5 V to $V_{AA}$ + 0.5 V
Ambient Operating Temperature ($T_A$) . . . . . −55°C to +125°C
Storage Temperature ($T_S$) . . . . . −65°C to +150°C
Junction Temperature ($T_J$) . . . . . +150°C
Lead Temperature (Soldering, 10 secs) . . . . . +260°C
Vapor Phase Soldering (1 minute) . . . . . +220°C
Analog Outputs to GND[1] . . . . . GND − 0.5 to $V_{AA}$

NOTES

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

**ORDERING GUIDE[1, 2, 3]**

| Speed | | | | |
|---|---|---|---|---|
| 220 MHz | 170 MHz | 135 MHz | 110 MHz | 85 MHz |
| ADV7151LS220 | ADV7151LS170 | ADV7151LS135 | ADV7151LS110 | ADV7151LS85 |

NOTES

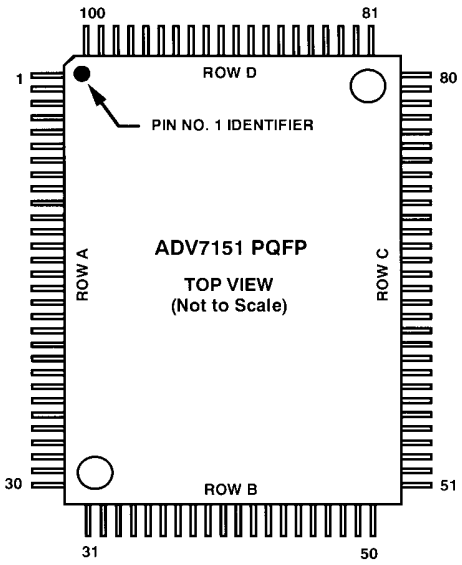
[1]ADV7151 is packaged in a 100-pin plastic quad flatpack, QFP.
[2]All devices are specified for 0°C to +70°C operation.
[3]Contact sales office for latest information on package design.

## ADV7151 PIN ASSIGNMENTS

| Pin No. | Mnemonic | Pin No. | Mnemonic | Pin No. | Mnemonic |
|---|---|---|---|---|---|
| 1 | $V_{AA}$ | 41 | $\overline{SYNCOUT}$ | 81 | $V_{AA}$ |
| 2 | $\overline{SYNC}$ | 42 | GND | 82 | D6 |
| 3 | $\overline{BLANK}$ | 43 | NC | 83 | D7 |
| 4 | NC | 44 | GND | 84 | D8 |
| 5 | NC | 45 | GND | 85 | D9 |
| 6 | NC | 46 | NC | 86 | GND |
| 7 | $P0_A$ | 47 | NC | 87 | GND |
| 8 | $P0_B$ | 48 | $PS0_A$ | 88 | $\overline{IOB}$ |
| 9 | $P0_C$ | 49 | $PS0_B$ | 89 | $\overline{IOR}$ |
| 10 | $P0_D$ | 50 | $PS0_C$ | 90 | $\overline{IOG}$ |
| 11 | $P1_A$ | 51 | $PS0_D$ | 91 | IOB |
| 12 | $P1_B$ | 52 | $PS1_A$ | 92 | IOG |
| 13 | $P1_C$ | 53 | $PS1_B$ | 93 | $V_{AA}$ |
| 14 | $P1_D$ | 54 | $PS1_C$ | 94 | $V_{AA}$ |
| 15 | NC | 55 | $PS1_D$ | 95 | IOR |
| 16 | $P2_A$ | 56 | $P5_A$ | 96 | COMP |
| 17 | $P2_B$ | 57 | $P5_B$ | 97 | $V_{REF}$ |
| 18 | $P2_C$ | 58 | $P5_C$ | 98 | $R_{SET}$ |
| 19 | $P2_D$ | 59 | $P5_D$ | 99 | $I_{PLL}$ |
| 20 | NC | 60 | $P6_A$ | 100 | GND |
| 21 | NC | 61 | $P6_B$ | | |
| 22 | $P3_A$ | 62 | $P6_C$ | | |
| 23 | $P3_B$ | 63 | $P6_D$ | | |
| 24 | $P3_C$ | 64 | NC | | |
| 25 | $P3_D$ | 65 | $P7_A$ | | |
| 26 | NC | 66 | $P7_B$ | | |
| 27 | NC | 67 | $P7_C$ | | |
| 28 | $P4_A$ | 68 | $P7_D$ | | |
| 29 | $P4_B$ | 69 | NC | | |
| 30 | $P4_C$ | 70 | $\overline{CE}$ | | |
| 31 | $P4_D$ | 71 | $R/\overline{W}$ | | |
| 32 | $\overline{CLOCK}$ | 72 | C0 | | |
| 33 | CLOCK | 73 | C1 | | |
| 34 | LOADIN | 74 | D0 | | |
| 35 | LOADOUT | 75 | D1 | | |
| 36 | $V_{AA}$ | 76 | D2 | | |
| 37 | $V_{AA}$ | 77 | GND | | |
| 38 | PRGCKOUT | 78 | D3 | | |
| 39 | SCKIN | 79 | D4 | | |
| 40 | SCKOUT | 80 | D5 | | |

NC = NO CONNECT.

### 100-Lead QFP Configuration



## PIN FUNCTION DESCRIPTION

| Mnemonic | Function |
|---|---|
| $P0_A$ . . . $P0_D$–$P7_A$ . . . $P7_D$ | Pixel Port (TTL Compatible Inputs). There are 32 pixel select inputs on the ADV7151. Each bit is multiplexed [A–D] 4:1, 2:1 or 1:1. Pixel Data is latched into the device on a rising LOADIN signal rising edge. |
| $PS0_A$ . . . $PS0_D$, $PS1_A$ . . . $PS1_D$ | Palette Priority Selects (TTL Compatible Inputs). These pixel port select inputs determine whether or not the device's pixel data port is selected on a pixel by pixel basis. The palette selects allow switching between multiple palette devices. The device can be preprogrammed to completely shut off the DAC analog outputs. If the values of PS0 and PS1 match the values programmed into bits MR16 and MR17 of the Mode Register, then the device is selected. Each bit is multiplexed [A–D] 4:1, 2:1 or 1:1. PS0 and PS1 are latched into the device on a rising LOADIN signal rising edge. |
| LOADIN | Pixel Data Load Input (TTL Compatible Input). This input latches the serialized pixel data, including PS0–PS1, $\overline{\text{BLANK}}$ and $\overline{\text{SYNC}}$ into the device. |
| LOADOUT | Pixel Data Load Output (TTL Compatible Output). This output control signal runs at a divided down frequency of the pixel CLOCK input. Its frequency is a function of the multiplex rate. It can be used to directly or indirectly drive LOADIN<br>$f_{LOADOUT} = f_{CLOCK}/M$<br>where ($M$ = 1 for 1:1 Multiplex Mode)<br>($M$ = 2 for 2:1 Multiplex Mode)<br>($M$ = 4 for 4:1 Multiplex Mode). |
| PRGCKOUT | Programmable Clock Output (TTL Compatible Output). This output control signal runs at a divided down frequency of the pixel CLOCK input. Its frequency is user programmable and is determined by bits CR30 and CR31 of Command Register 3<br>$f_{PRGCKOUT} = f_{CLOCK}/N$<br>where $N$ = 4, 8, 16 and 32. |
| SCKIN | Video Shift Clock Input (TTL Compatible Input). The signal on this input is internally gated synchronously with the $\overline{\text{BLANK}}$ signal. The resultant output, SCKOUT, is a video clocking signal that is stopped during video blanking periods. |
| SCKOUT | Video Shift Clock Output (TTL Compatible Output). This output is a synchronously gated version of SCKIN and $\overline{\text{BLANK}}$. SCKOUT, is a video clocking signal that is stopped during video blanking periods. |
| CLOCK, $\overline{\text{CLOCK}}$ | Clock Inputs (ECL Compatible Inputs). These differential clock inputs are designed to be driven by ECL logic levels configured for single supply (+5 V) operation. The clock rate is normally the pixel clock rate of the system. |
| $\overline{\text{BLANK}}$ | Composite Blank (TTL Compatible Input). This video control signal drives the analog outputs to the blanking level. |
| $\overline{\text{SYNC}}$ | Composite-Sync Input (TTL Compatible Input). This video control signal drives the IOG analog output to the $\overline{\text{SYNC}}$ level. It is only asserted during the blanking period. CR22 in Command Register 2 must be set if $\overline{\text{SYNC}}$ is to be decoded onto the analog output, otherwise the $\overline{\text{SYNC}}$ input is ignored. |
| $\overline{\text{SYNCOUT}}$ | Composite SYNC O/P (TTL Compatible Output). This video output is a delayed version of $\overline{\text{SYNC}}$. The delay corresponds to the number of pipeline stages of the device. |
| D0–D9 | Databus (TTL Compatible Input/Output Bus). Data, including color palette values and device control information is written to and read from the device over this 10-bit, bidirectional databus. 10-bit data or 8-bit data can be used. The databus can be configured for either 10-bit parallel data or byte data (8+2) as well as standard 8-bit data. Any unused bits of the databus should be terminated through a resistor to either the digital power plane ($V_{CC}$) or GND. |
| $\overline{\text{CE}}$ | Chip Enable (TTL Compatible Input). This input must be at Logic "0" when writing to or reading from the device over the databus (D0–D9). Internally, data is latched on the rising edge of $\overline{\text{CE}}$. |
| R/$\overline{\text{W}}$ | Read/Write Control (TTL Compatible Input). This input determines whether data is written to or read from the device's registers and color palette RAM. R/$\overline{\text{W}}$ and $\overline{\text{CE}}$ must be at Logic "0" to write data to the part. R/$\overline{\text{W}}$ must be at Logic "1" and $\overline{\text{CE}}$ at Logic "0" to read from the device. |

| Mnemonic | Function |
|---|---|
| C0, C1 | Command Controls (TTL Compatible Inputs). These inputs determine the type of read or write operation being performed on the device over the databus (see Interface Truth Table). Data on these inputs is latched on the falling edge of $\overline{CE}$. |
| IOR; $\overline{IOR}$, IOG; $\overline{IOG}$, IOB; $\overline{IOB}$ | Red, Green and Blue Current Outputs (High Impedance Current Sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into doubly terminated 75 Ω loads.<br>$\overline{IOR}$, $\overline{IOG}$ and $\overline{IOB}$ are the complementary outputs of IOR, IOG and IOB. These outputs can be tied to GND if it is not required to use differential outputs. |
| $V_{REF}$ | Voltage Reference Input (Analog Input). An external 1.235 V voltage reference is required to drive this input. An AD589 (2-terminal voltage reference) or equivalent is recommended. (Note: It is not recommended to use a resistor network to generate the voltage reference.) |
| $R_{SET}$ | Output Full-Scale Adjust Control (Analog Input). A resistor connected between this pin and analog ground controls the absolute amplitude of the output video signal. The value of $R_{SET}$ is derived from the full-scale output current on IOG according to the following equations:<br>$R_{SET}\ (\Omega) = C1 \times R_{REF}/IOG\ (mA)$; $\overline{SYNC}$ *on GREEN*<br>$R_{SET}\ (\Omega) = C2 \times R_{REF}/IOG\ (mA)$; *No* $\overline{SYNC}$ *on GREEN.*<br>Full-Scale output currents on IOR and IOB for a particular value of $R_{SET}$ are given by:<br>$IOR\ (mA) = C2 \times R_{REF}\ (V)/R_{SET}\ (\Omega)$<br>and<br>$IOB\ (mA) = C2 \times R_{REF}\ (V)/R_{SET}\ (\Omega)$<br>where *C1* = 6,050: PEDESTAL = 7.5 IRE<br>= 5,723: PEDESTAL = 0 IRE<br>and<br>*C2* = 4,323: PEDESTAL = 7.5 IRE<br>= 3,996: PEDESTAL = 0 IRE. |
| COMP | Compensation Pin. A 0.1 μF capacitor should be connected between this pin and $V_{AA}$. |
| $I_{PLL}$ | Phase Lock Loop Output Current (High Impedance Current Source). This output is used to enable multiple ADV7151s along with ADV7150/ADV7152s to be synchronized together with subpixel resolution when using an external PLL. This output is triggered either from the falling edge of $\overline{SYNC}$ or $\overline{BLANK}$ as determined by bit CR21 of Command Register 2. When activated, it supplies a current corresponding to<br>$I_{PLL}\ (mA) = 1{,}728 \times R_{REF}(V)/R_{SET}\ (\Omega)$.<br>When not using the $I_{PLL}$ function, this output pin should be tied to GND. |
| $V_{AA}$ | Power Supply (+5 V ± 5%). The part contains multiple power supply pins, all should be connected together to one common +5 V filtered analog power supply. |
| GND | Analog Ground. The part contains multiple ground pins, all should be connected together to the system's ground plane. |

*(Continued from page 1)*

Indexed-Color image rendition, at speeds of up to 220 MHz, is achieved through the use of the on-board data multiplexer/ serializer. The pixel input port's flexibility allows for direct interface to most standard frame buffer memory configurations.

The 30 bits of resolution, associated with the color look-up table and triple 10-bit DAC, realizes 8-bit Indexed-Color resolution, while also allowing for the on-board implementation of linearization algorithms, such as Gamma-Correction. This allows effective 10-bit Indexed-Color operation.

The on-chip video clock controller circuit generates all the internal clocking and some additional external clocking signals. An external ECL oscillator source with differential outputs is all that is required to drive the CLOCK and $\overline{\text{CLOCK}}$ inputs of the ADV7151. The part can also be driven by an external clock generator chip circuit, such as the AD730.

The ADV7151 is capable of generating RGB video output signals which are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

Test diagnostic circuitry has been included to complement the users system level debugging.

The ADV7151 is fabricated in a +5 V CMOS process. Its monolithic CMOS construction ensures greater functionality with low power dissipation.

The ADV7151 is packaged in a plastic 100-pin quad flatpack (QFP). Superior thermal dissipation is achieved by inclusion of a copper heatslug, within the standard package outline to which the die is attached.

# CIRCUIT DETAILS AND OPERATION

## OVERVIEW

Digital video or pixel data is latched into the ADV7151 over the devices Pixel Port. This data acts as a pointer to the on-board Color Palette RAM. The data at the RAM address pointed to is latched into the digital-to-analog converters (DACs) and output as an RGB analog video signal.

For the purposes of clarity of description, the ADV7151 is broken down into three separate functional blocks. These are:

1. Pixel port and clock control circuit
2. MPU port, registers and color palette
3. Digital-to-analog converters and video outputs

**Table I. Architectural and Packaging Differences of the ADV715x Series**

| Description | ADV7150* | ADV7151 | ADV7152* |
|---|---|---|---|
| 24-Bit "Gamma" True Color | • | | • |
| 24-Bit "Standard" True Color | • | | • |
| 8-Bit "Gamma" Pseudo Color | • | • | • |
| 8-Bit "Standard" Pseudo Color | • | • | • |
| 15-Bit True Color | • | | • |
| 220 MHz—True Color | • | | • |
| 220 MHz—Pseudo Color | • | • | • |
| Triple 10-Bit DACs | • | • | • |
| 4:1 Multiplexing | • | • | |
| 2:1 Multiplexing | • | • | • |
| 1:1 Multiplexing | • | • | • |
| 160-Lead QFP | • | | |
| 100-Lead QFP | | • | • |

*See the relevant data sheet for more information on these parts.

Table I shows the architectural and packaging differences between the ADV7151 and the associated ADV7150/ADV7152. (For more details on the ADV7150 or the ADV7152, please consult the relevant data sheet).

### Pixel Port and Clock Control Circuit

The Pixel Port of the ADV7151 is directly interfaced to the video/graphics pipeline of a computer graphics subsystem. It is connected directly or through a gate array to the video RAM of the systems Frame-Buffer (video memory). The pixel port on the device consists of:

| | |
|---|---|
| Color Data | P0A–P7A . . . P0D–P7D |
| Pixel Controls | $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ |
| Palette Selects | PS0–PS1 |

The associated clocking signals for the pixel port include:

| | |
|---|---|
| Clock Inputs | CLOCK, $\overline{\text{CLOCK}}$, LOADIN, SCKIN |
| Clock Outputs | LOADOUT, PRGCKOUT, SCKOUT |

These on-board clock control signals are included to simplify interfacing between the part and the frame buffer. Only two control input signals are necessary to get the part operational, CLOCK and $\overline{\text{CLOCK}}$ (ECL Levels). No additional signals or external glue logic are required to get the *Pixel Port and Clock Control Circuit* of the part operational.

### Pixel Port (Color Data)

The ADV7151 has 32 pixel data inputs. These are organized as four (for 4:1 multiplexing) 8-bit wide indexed color data inputs. The part supports 8-bit Pseudo Color in 4:1, 2:1 and 1:1 multiplex modes.

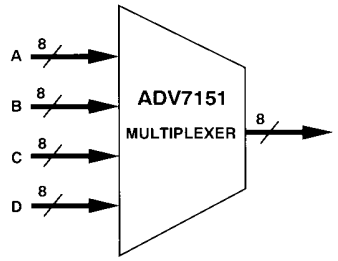



*Figure 12. Multiplexed Color Inputs for the ADV7151*

Color data is latched into the parts pixel port on every rising edge of LOADIN (see Timing Waveform Figure 3). The required frequency of LOADIN is determined by the multiplex rate, where

$f_{LOADIN} = f_{CLOCK}/4$ 4:1 Multiplex Mode
$f_{LOADIN} = f_{CLOCK}/2$ 2:1 Multiplex Mode
$f_{LOADIN} = f_{CLOCK}$ 1:1 Multiplex Mode

Other pixel data signals latched into the device by LOADIN include $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and PS0–PS1.

Internally, data is pipelined through the part by the differential pixel clock inputs, CLOCK and $\overline{\text{CLOCK}}$. The LOADIN control signal does not need to have a relationship to the pixel CLOCK (see "Pipeline Delay" section). A completely asynchronous LOADIN signal can be used with the ADV7151.

Alternatively, the LOADOUT signal of the ADV7151 can be used. LOADOUT can be connected either directly or indirectly to LOADIN. Its frequency is automatically set to the correct LOADIN requirement.

### SYNC, BLANK

The BLANK and composite SYNC video control signals drive the analog outputs to the blanking and sync levels respectively. These signals are latched into the part on the rising edge of LOADIN. The SYNC information is encoded onto the IOG analog signal when Bit CR22 of Command Register 2 is set to a Logic "1." The SYNC input is ignored if CR22 is set to "0."

### SYNCOUT

In some applications where it is not permissible to encode SYNC on green (IOG), SYNCOUT can be used as a separate TTL digital SYNC output. This has the advantage over an independent (of the ADV7151) SYNC in that it does not necessitate knowing the absolute pipeline delay of the part. This allows complete independence between LOADIN/Pixel Data and CLOCK. The SYNC input is connected to the device as normal with Bit CR22 of Command Register 2 set to "0" thereby preventing SYNC from being encoded onto IOG. Bit CR12 of Command Register 1 is set to "1", enabling SYNCOUT. The output signal generates a TTL SYNCOUT with correct pipeline delay which is capable of directly driving the composite SYNC signal of a computer monitor.

### PS0–PS1 (Palette Priority Select Inputs)

These pixel port select inputs determine whether or not the device is selected. This is determined on a pixel by pixel basis as the PS0–PS1 inputs are multiplexed in exactly the same format as the pixel port data. These controls allow for switching between multiple devices (see Appendix 4). If values of PS0 and PS1 don't match the values programmed into bits MR16 and MR17 of the mode register, then the outputs of the device are forced to 0 mA regardless of the state of the pixel and control data inputs. Otherwise the device is selected and acts as normal.

### Multiplexing

The on-board multiplexers of the ADV7151 eliminate the need for external data serializer circuits. Multiple video memory devices can be connected, in parallel, directly to the device. Figure 13 shows four memory banks of 33 MHz memory connected to the ADV7151, running in 4:1 multiplex mode, giving a resultant pixel or dot clock rate of 132 MHz. As mentioned in the previous section, the ADV7151 supports a number of color data formats in 4:1, 2:1 and 1:1 multiplex modes.

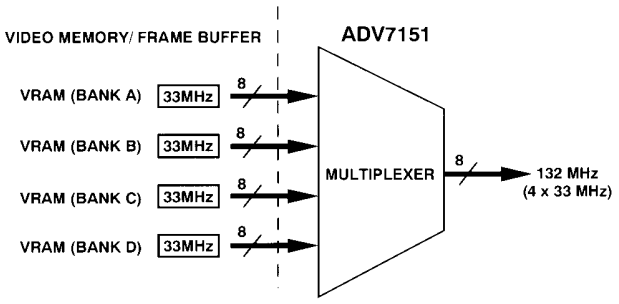



*Figure 13. Direct Interfacing of Video Memory to ADV7151*

In 1:1 multiplex mode, the ADV7151 is clocked using the LOADIN signal. This means that there is no requirement for differential ECL inputs on CLOCK and CLOCK. The pixel clock is connected directly to LOADIN. (Note the ECL CLOCK can still be used to generate LOADOUT, PRGCKOUT, etc.)

### CLOCK CONTROL CIRCUIT

The ADV7151 has an integrated Clock Control Circuit (Figure 14). This circuit is capable of both generating the ADV7151's internal clocking signals as well as external graphics subsystem clocking signals. Total system synchronization can be attained by using the parts output clocking signals to drive the controlling graphics processor's master clock as well as the video frame buffers shift clock signals.

### CLOCK, CLOCK Inputs

The Clock Control Circuit is driven by the pixel clock inputs, CLOCK and CLOCK. These inputs can be driven by a differential ECL oscillator running from a +5 V supply.

Alternatively, the ADV7151 CLOCK inputs can be driven by a Programmable Clock Generator (Figure 15), such as the ICS1562. The ICS1562 is a monolithic, phase-locked-loop, clock generator chip capable of synthesizing differential ECL output frequencies of up to 220 MHz from a single low frequency reference crystal.

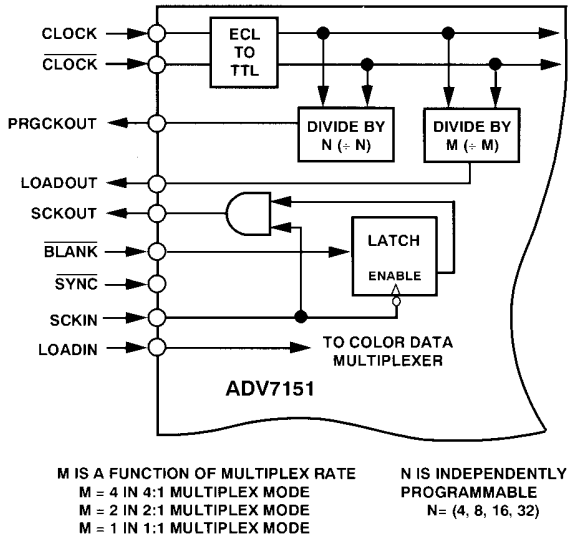



*Figure 14. Clock Control Circuit of the ADV7151*

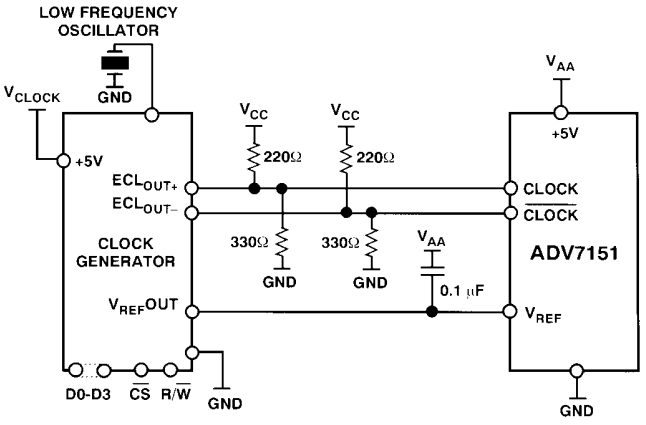



*Figure 15. PLL Clock Generator Driving the ECL Clock Inputs of the ADV7151*

## CLOCK CONTROL SIGNALS

### LOADOUT

The ADV7151 generates a LOADOUT control signal which runs at a divided down frequency of the pixel CLOCK. The frequency is automatically set to the programmed multiplex rate, controlled by CR37 and CR36 of Command Register 3.

$f_{LOADOUT} = f_{CLOCK}/4$ 4:1 Multiplex Mode
$f_{LOADOUT} = f_{CLOCK}/2$ 2:1 Multiplex Mode
$f_{LOADOUT} = f_{CLOCK}$ 1:1 Multiplex Mode

The LOADOUT signal is used to directly drive the LOADIN pixel latch signal of the ADV7151. This is most simply achieved by tying the LOADOUT and LOADIN pins together. Alternatively, the LOADOUT signal can be used to drive the frame buffer's shift clock signals, returning to the LOADIN input delayed with respect to LOADOUT.

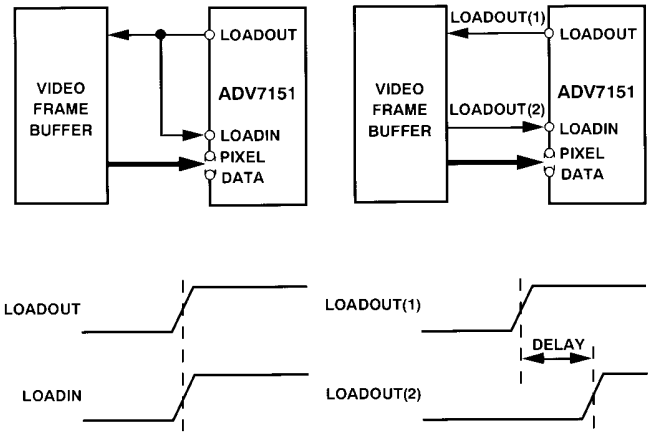



*Figure 16. LOADOUT vs. Pixel Clock Input (CLOCK, $\overline{CLOCK}$)*

If it is not necessary to have a known fixed number of pipeline delays, then there is no limitation on the delay between LOADOUT and LOADIN (LOADOUT(1) and LOADOUT(2)). LOADIN and Pixel Data must conform to the setup and hold times $t_8$ and $t_9$).

If however, it is required that the ADV7151 has a fixed number of pipeline delays ($t_{PD}$), LOADOUT and LOADIN must conform to timing specifications $t_{10}$ and $\tau$–$t_{11}$ as illustrated in Figures 4 to 7.

### PRGCKOUT

The PRGCKOUT control signal outputs a user programmable clock frequency. It is a divided down frequency of the pixel CLOCK (see Figure 8). The rising edge of PRGCKOUT is synchronous with the rising edge of LOADOUT.

$f_{PRGCKOUT} = f_{CLOCK}/N$ where N = 4, 8, 16 or 32

One application of the PRGCKOUT is to use it as the master clock frequency of the graphics subsystems processor or controller.

### SCKIN, SCKOUT

These video memory signals are used to minimize external support chips. Figure 17 illustrates the function that is provided. An input signal applied to SCKIN is AND-ed with the video blanking signal ($\overline{BLANK}$). The resulting signal is output on SCKOUT. Figure 9 of the Timing Waveform section shows the relationship between SCKOUT, SCKIN and $\overline{BLANK}$.

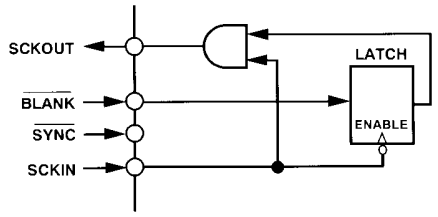



*Figure 17. SCKOUT Generation Circuit*

The SCKOUT signal is essentially the video memory shift control signal. It is stopped during the screen retrace. Figure 18 shows a suggested frame buffer to ADV7151 interface. This is a minimum chip solution and allows the ADV7151 control the overall graphics system clocking and synchronization.

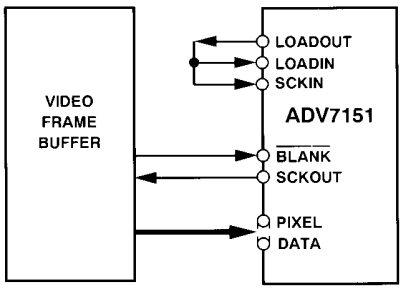



*Figure 18. ADV7151 Interface Using SCKIN and SCKOUT*

### Pipeline Delay and On-Board Calibration

The ADV7151 has a fixed number of pipeline delays ($t_{PD}$), so long as timings $t_{10}$ and $\tau$–$t_{11}$ are met. However, if a fixed pipeline delay is not a requirement, timings $t_{10}$ and $\tau$–$t_{11}$ can be ignored, a calibration cycle must be run and there is no restriction on LOADIN to LOADOUT timing. If timings $t_{10}$ and $\tau$–$t_{11}$ are met the part will function correctly though with an increased number of pipeline delays: $t_{PD}$ + N CLOCKS (for 4:1 Mode N = 4, for 2:1 Mode N = 2, for 1:1 Mode N = 0). The ADV7151 has on-board calibration circuitry which synchronizes pixel data and LOADIN with the internal ADV7151 clocking signals. Calibration is performed in two ways. During the devices initialization sequence by toggling two bits of the Mode Register, MR10 followed by MR15 or by writing a "1" to Bit CR10 of Command Register 1 which executes a calibration on every vertical sync.

## COLOR VIDEO MODES

The ADV7151 supports two color video modes all at the maximum video rate.

Command bits CR24–CR27 of Command Register 2 along with bit MR11 of Mode Register 1 determine the color mode.

### 8-Bit "Gamma" Pseudo Color (CR24, CR25, CR26, CR27 = X, X, 0, 0 and MR11 = 1)

This mode sets the part into 8-bit Pseudo-Color operation. The pixel port accepts 8-bits of pixel data which indexes a 30-bit word in the Look-Up Table RAM. The Look-Up Table is configured as a 256 location by 30 bits deep RAM (10 bits each for Red, Green and Blue). The output of the RAM drives the DACs with 30-bit data (10 bits each for Red, Green and Blue).

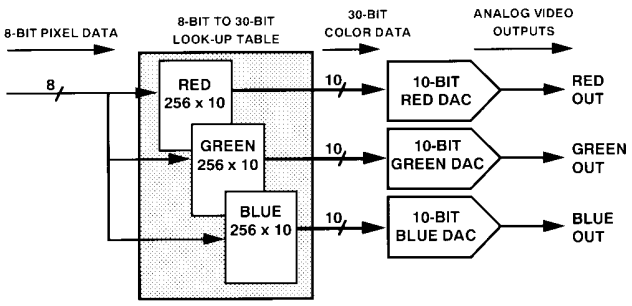



*Figure 19. 8-Bit to 30-Bit Pseudo-Color Configuration*

This mode allows for the display of 256 simultaneous colors out of a total palette of millions of addressable colors

**8-Bit "Standard" Pseudo Color**
**(CR24, CR25, CR26, CR27 = X,X,0,0 and MR11 = 0)**
This mode sets the part into 8-bit Pseudo-Color operation. The pixel port accepts 8-bits of pixel data which indexes a 24-bit word in the Look-Up Table RAM. The Look-Up Table is configured as a 256 location by 24 bits deep RAM (10 bits each for Red, Green and Blue). The output of the RAM drives the DACs with 24-bit data (8 bits each for Red, Green and Blue).

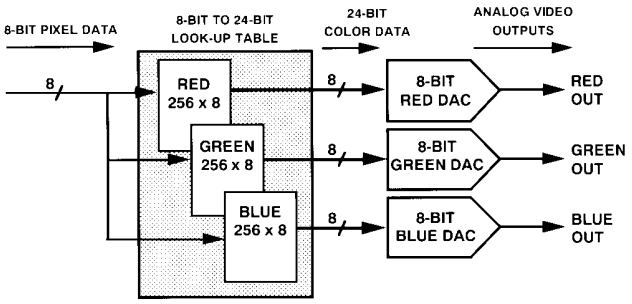



*Figure 20. 8-Bit to 24-Bit Pseudo-Color Configuration*

This mode allows for the display of 256 simultaneous colors out of a total palette of millions of addressable colors.

# MICROPROCESSOR (MPU) PORT

The ADV7151 supports a standard MPU Interface. All the functions of the part are controlled via this MPU port. Direct access is gained to the Address Register, Mode Register and all the Control Registers as well as the Color Palette. The following sections describe the setup for reading and writing to all of the devices registers.

**MPU Interface**
The MPU interface (Figure 21) consists of a bidirectional, 10-bit wide databus and interface control signals $\overline{CE}$, C0, C1 and R/$\overline{W}$. The 10-bit wide databus is user configurable as illustrated.

**Table II. Databus Width**

| Databus Width | RAM/DAC Resolution | Read/Write Mode |
|---|---|---|
| 10-Bit | 10-Bit | 10-Bit Parallel |
| 10-Bit | 8-Bit | 8-Bit Parallel |
| 8-Bit | 10-Bit | 8+2 Byte |
| 8-Bit | 8-Bit | 8-Bit Parallel |

**Register Mapping**
The ADV7151 contains a number of on-board registers including the Mode Register (MR17–MR10), Address Register (A7–A0) and nine Control Registers as well as Red (R9–R0), Green (G9–G0) and Blue (B9–B0) Color Registers. These registers control the entire operation of the part. Figure 22 shows the internal register configuration.

Control lines C1 and C0 determine which register the MPU is accessing. C1 and C0 also determine whether the Address Register is pointing to the color registers and look-up table RAM or the control registers. If C1, C0 = 1, 0, the MPU has access to whatever control register is pointed to by the Address Register (A7–A0). If C1, C0 = 0, 1, the MPU has access to the Look-Up Table RAM (Color Palette) through the associated color registers. The $\overline{CE}$ input latches data to or from the part.

The R/$\overline{W}$ control input determines between read or write accesses. The Truth Tables III and IV show all modes of access to the various registers and color palette for both the 8-bit wide databus configuration and 10-bit wide databus configuration. It should be noted that after power-up, the devices MPU port is automatically set to 10-bit wide operation (see Power-On Reset section).

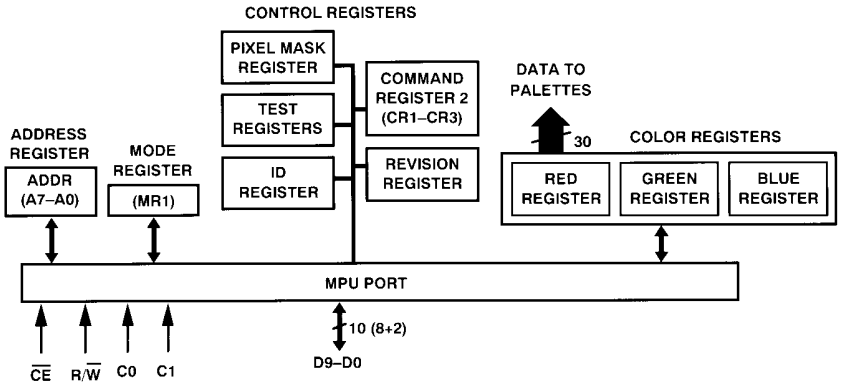



*Figure 21. MPU Port and Register Configuration*

### Color Palette Accesses

Data is written to the color palette by first writing to the address register, the address of the color palette location to be modified. The MPU performs three successive write cycles for each of the red, green and blue registers (10-bit or 8-bit). An internal pointer moves from red to green to blue after each write is completed. This pointer is reset to red after a blue write or whenever the address register is written. During the blue write cycle, the three bytes of red green and blue are concatenated into a single 30-bit/24-bit word and written to the RAM location as specified in the address register (A7–A0). The address register then automatically increments to point to the next RAM location and a similar red, green and blue palette write sequence is performed. The address register resets to 00H following a blue write cycle to color palette RAM location FFH.

Data is read from the color palette by first writing to the address register the address of the color palette location to be read. The MPU performs three successive read cycles from each of the red, green and blue locations (10-bit or 8-bit) of the RAM. An internal pointer moves from red to green to blue after each read is completed. This pointer is reset to red after a blue read or whenever the address register is written. The address register then automatically increments to point to the next RAM location and a similar red, green and blue palette read sequence is performed. The address register resets to 00H following a blue read cycle of color palette RAM location FFH.

### Register Accesses

The MPU can write to or read from all of the ADV7151s registers. C0 and C1 determine whether the Mode Register or Address Register is being accessed. Access to these registers is direct. The Control Registers are accessed indirectly. The Address Register must point to the desired Control Register.

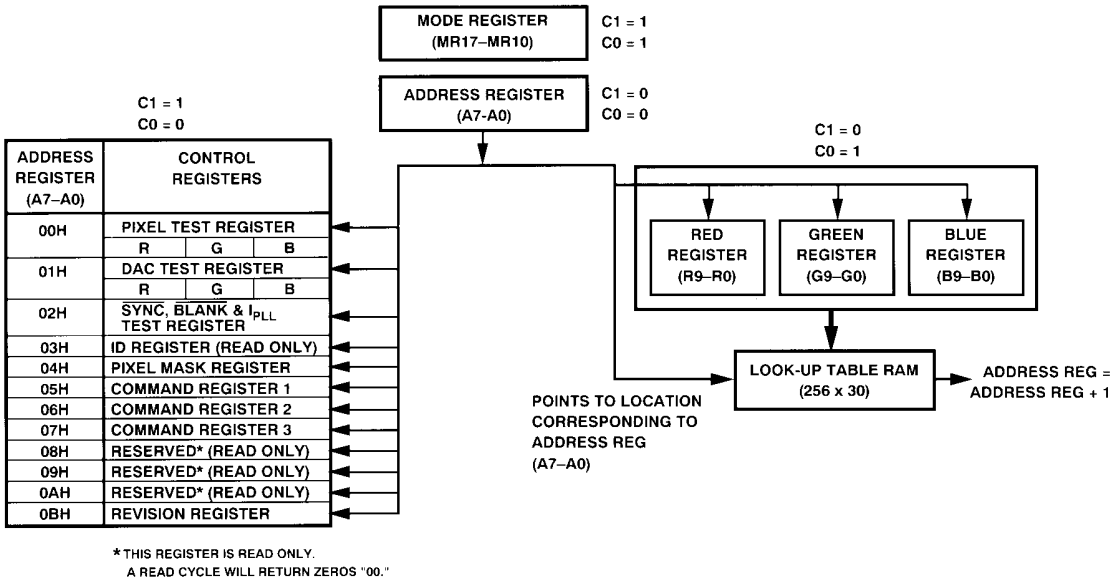



*Figure 22. Internal Register Configuration and Address Decoding*

**Table III. Truth Table (10-Bit Databus Mode)**

| R/$\overline{W}$ | C1 | C0 | Databus (D9–D0) | Operation | Result |
|---|---|---|---|---|---|
| 0 | 1 | 1 | DB7–DB0 | Write to Mode Register | DB7–DB0 → MR17–MR10 |
| 0 | 0 | 0 | DB7–DB0 | Write to Address Register | DB7–DB0 → A7–A0 |
| 0 | 1 | 0 | DB7–DB0 | Write to Control Registers | DB7–DB0 → Control Registers |
| | | | | *(Particular Control Register Determined by Address Register)* | |
| 0 | 0 | 1 | DB9–DB0 | Write to RED Register | DB9–DB0 → R9–R0 |
| 0 | 0 | 1 | DB9–DB0 | Write to GREEN Register | DB9–DB0 → G9–G0 |
| 0 | 0 | 1 | DB9–DB0 | Write to BLUE Register | DB9–DB0 → B9–B0 |
| | | | | Write RGB Data to RAM Location Pointed to by Address Register (A7–A0) | |
| | | | | Address Register = Address Register + 1 | |
| 1 | 1 | 1 | DB7–DB0 | Read Mode Register | MR17–MR10 → DB7–DB0 |
| 1 | 0 | 0 | DB7–DB0 | Read Address Register | A7–A0 → DB7–DB0 |
| 1 | 1 | 0 | DB7–DB0 | Read Control Registers | Register Data → DB7–DB0 |
| | | | | *(Particular Control Register Determined by Address Register)* | |
| 1 | 0 | 1 | DB9–DB0 | Read RED RAM Location | R9–R0 → DB9–DB0 |
| 1 | 0 | 1 | DB9–DB0 | Read GREEN RAM Location | G9–G0 → DB9–DB0 |
| 1 | 0 | 1 | DB9–DB0 | Read BLUE RAM Location | B9–B0 → DB9–DB0 |
| | | | | *(RAM Location Pointed to by Address Register (A7–A0)* | |
| | | | | Address Register = Address Register + 1 | |

DB = Data Bit.

Table IV. Truth Table (8-Bit Databus Mode)*

| R/$\overline{W}$ | C1 | C0 | Databus (D7–D0) | Operation | Result |
|---|---|---|---|---|---|
| 0 | 1 | 1 | DB7–DB0 | Write to Mode Register | DB7–DB0 → MR17–MR10 |
| 0 | 0 | 0 | DB7–DB0 | Write to Address Register | DB7–DB0 → A7–A0 |
| 0 | 1 | 0 | DB7–DB0 | Write to Control Registers | DB7–DB0 → Control Registers |
| | | | | *(Particular Control Register Determined by Address Register (A7–A0))* | |
| 0 | 0 | 1 | DB9–DB2 | Write to RED Register | DB9–DB2 → R9–R2 |
| 0 | 0 | 1 | DB1–DB0 | Write to RED Register | DB1–DB0 → R1–R0 |
| 0 | 0 | 1 | DB9–DB2 | Write to GREEN Register | DB9–DB2 → G9–G2 |
| 0 | 0 | 1 | DB1–DB0 | Write to GREEN Register | DB1–DB0 → G1–G0 |
| 0 | 0 | 1 | DB9–DB2 | Write to BLUE Register | DB9–DB2 → B9–B2 |
| 0 | 0 | 1 | DB1–DB0 | Write to BLUE Register | DB1–DB0 → B1–B0 |
| | | | | Write RGB Data to RAM Location Pointed to by Address Register (A7–A0) | |
| | | | | Address Register = Address Register + 1 | |
| 1 | 1 | 1 | DB7–DB0 | Read Mode Register | MR17–MR10 → DB7–DB0 |
| 1 | 0 | 0 | DB7–DB0 | Read Address Register | A7–A0 → DB7–DB0 |
| 1 | 1 | 0 | DB7–DB0 | Read Control Registers | Register Data → DB7–DB0 |
| | | | | *(Particular Control Register Determined by Address Register)* | |
| 1 | 0 | 1 | DB9–DB2 | Read RED RAM Location | R9–R2 → DB9–DB2 |
| 1 | 0 | 1 | DB1–DB0 | Read RED RAM Location | R1–R0 → DB1–DB0 |
| 1 | 0 | 1 | DB9–DB2 | Read GREEN RAM Location | G9–G2 → DB9–DB2 |
| 1 | 0 | 1 | DB1–DB0 | Read GREEN RAM Location | G1–G0 → DB1–DB0 |
| 1 | 0 | 1 | DB9–DB2 | Read BLUE RAM Location | B9–B2 → DB9–DB2 |
| 1 | 0 | 1 | DB1–DB0 | Read BLUE RAM Location | B1–B0 → DB1–DB0 |
| | | | | *(RAM Location Pointed to by Address Register (A7–A0))* | |
| | | | | Address Register = Address Register + 1 | |

DB = Data Bit.
*Writing or reading 10-bit data (DB9–DB0) over an 8-bit databus (D7–D0) requires two write or two read cycles. DB9–DB2 is mapped to D7–D0 on the first cycle. DB1–DB0 is mapped to D1–D0 on the second cycle with D7–D2 ignored.

**Power-On Reset**

On power-up, the ADV7151 executes a power-on reset sequence. This initializes the pixel port such that the pixel sequence ABCD starts at A. The Mode Register (MR17–MR10), Command Register 2 (CR27–CR20) and Command Register 3 (CR37–CR30) have all bits set to a Logic "1."

The output clocking signals are also set during this reset period.

PRGCKOUT = CLOCK/32
LOADOUT = CLOCK/4

The power-on reset is activated when $V_{AA}$ goes from 0 V to 5 V. This reset is active for 1 μs. The ADV7151 should not be accessed during this reset period. The pixel clock should be applied at power-up.

## REGISTER PROGRAMMING

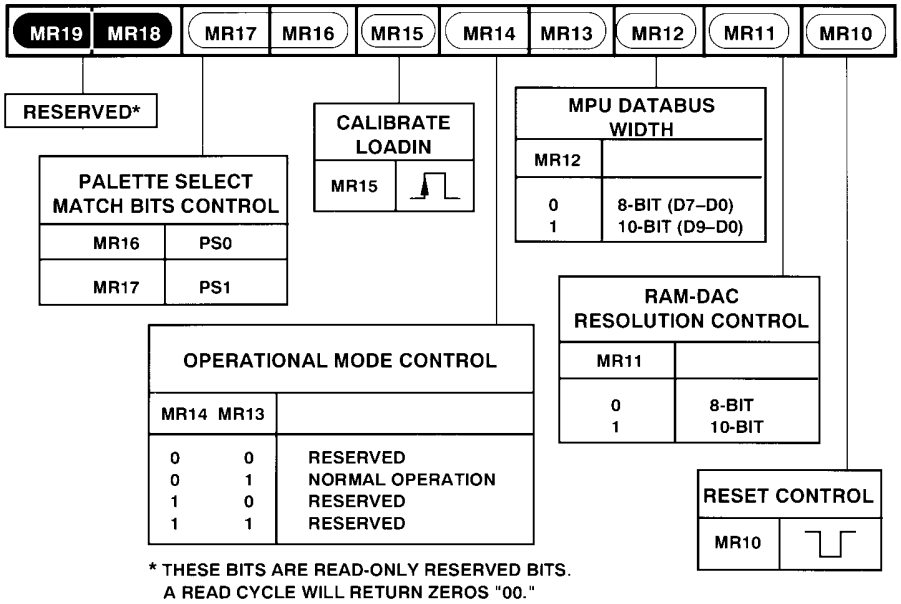
The following section describes each register, including Address Register, Mode Register and each of the nine Control Registers in terms of its configuration.

**Address Register (A7–A0)**

As illustrated in the previous tables, the C0 and C1 control inputs, in conjunction with this address register specify which control register, or color palette location is accessed by the MPU port. The address register is 8 bits wide and can be read from as well as written to. When writing to or reading from the color palette on a sequential basis, only the start address needs to be written. After a red, green and blue write sequence, the address register is automatically incremented.

**MODE REGISTER MR1 (MR19–MR10)**

The mode register is a 10-bit wide register. However, for programming purposes, it may be considered as an 8-bit wide register (MR18 and MR19 are both reserved). It is denoted as MR17–MR10 for simplification purposes.




*Mode Register 1 (MR1) (MR19–MR10)*

The diagram shows the various operations under the control of the mode register. This register can be read from as well written to. In read mode, if MR18 and MR19 are read back, they are both returned as zeros.

## MODE REGISTER (MR17–MR10) BIT DESCRIPTION

### Reset Control (MR10)

This bit is used to reset the pixel port sampling sequence. This ensures that the pixel sequence ABCD starts at A. It is reset by writing a "1" followed by a "0" followed by a "1." This bit must be run through this cycle during the initialization sequence.

### RAM-DAC Resolution Control (MR11)

When this is programmed with a "1," the RAM is 30-bits deep (10 bits each for red, green and blue) and each of the three DACs is configured for 10-bit resolution. When MR11 is programmed with a "0," the RAM is 24 bits deep (8 bits each for red, green and blue) and the DACs are configured for 8-bit resolution. The two LSBs of the 10-bit DACs are pulled down to zero in 8-bit RAM-DAC mode.

### MPU Databus Width (MR12)

This bit determines the width of the MPU port. It is configured as either a 10-bit wide (D9–D0) or 8-bit wide (D7–D0) bus. 10-bit data can be written to the device when configured in 8-bit wide mode. The 8 MSBs are first written on D7–D0, then the two LSBs are written over D1–D0. Bits D9–D8 are zeros in 8-bit mode.

### Operational Mode Control (MR14–MR13)

When MR14 is "0" and MR13 if "1," the port operates in normal mode.

### Calibrate LOADIN (MR15)

This bit automatically calibrates the on-board LOADIN/LOADOUT synchronization circuit. A "0" to "1" transition initiates calibration. This bit is set to "0" in normal operation. See "Pipeline Delay and Calibration" section. This bit must be run through this cycle during the initialization sequence.

### Palette Select Match Bits Control (MR17–MR16)

These bits allow multiple palette devices to work together. When bits PS1 and PS0 match MR17 and MR16 respectively, the device is selected. If these bits do not match, the device is not selected and the analog video outputs drive 0 mA. See Appendix 4, "Multiple Palette Applications."

## CONTROL REGISTERS

The ADV7151 has 9 control registers. To access each register, two write operations must be performed. The first write to the address register specifies which of the 9 registers is to be accessed. The second access determines the value written to that particular control register.

### Pixel Test Register (Address Reg (A7–A0) = 00H)

This register is used when the device is in test/diagnostic mode. It is an 8-bit wide read-only register which allows the MPU to read data on the pixel port (see Appendix 6, "Test Diagnostics").

### DAC Test Register (Address Reg (A7–A0) = 01H)

This register is used when the device is in test/diagnostic mode. It is a 30-bit (10 bits each for RED, GREEN and BLUE) wide read-only register which allows MPU access to the DAC port (see Appendix 6, "Test Diagnostics").

### $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and $I_{PLL}$ Test Register (Address Reg (A7–A0) = 02H)

This register is used when the device is in test/diagnostic mode. It is a 3-bit wide (3 LSBs) read/write register which allows MPU access to these particular pixel control bits (see Appendix 6, "Test Diagnostics").

### ID Register (Address Reg (A7–A0) = 03H)

This is an 8-bit wide "Identification" read-only register. For the ADV7151 it will always return the hexadecimal value 8FH.

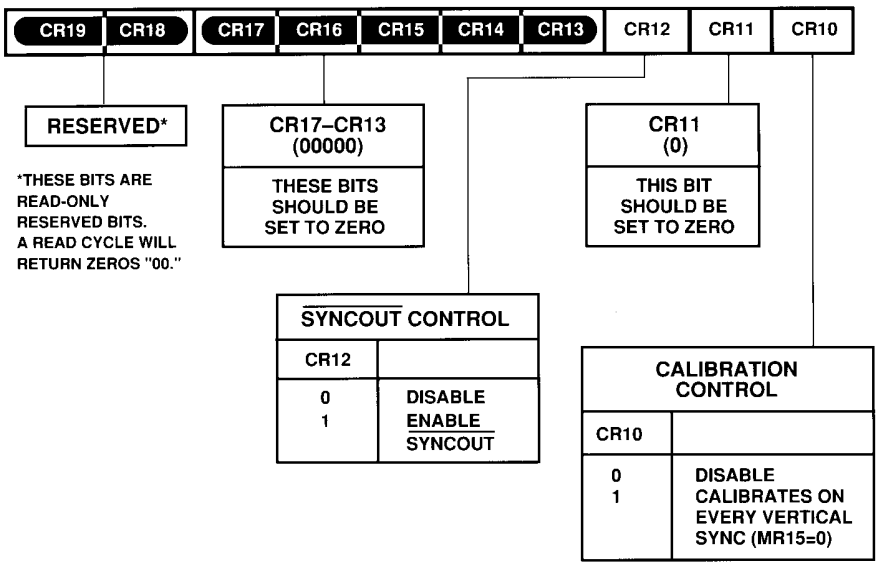
**Pixel Mask Register**
**(Address Reg (A7–A0) = 04H)**
The contents of the pixel mask register are individually bit-wise logically AND-ed with the Red, Green and Blue pixel input stream of data. It is an 8-bit read/write register with D0 corresponding to R0, G0 and B0. For normal operation, this register is set with FFH.

**COMMAND REGISTER 1 (CR1)**
**(Address Reg (A7–A0) = 05H)**
This register contains a number of control bits as shown in the diagram. CR1 is a 10-bit wide register. However for programming purposes, it may be considered as an 8-bit wide register (CR18 and CR19 are reserved).

The diagram below shows the various operations under the control of CR1. This register can be read from as well as written to. In write mode, zero should be written to CR11 and CR13 to CR17. In read mode, CR11 and CR13 to CR19 are all returned as zeros.

**COMMAND REGISTER 1 BIT DESCRIPTION**
**Calibration Control (CR10):**
This bit automatically calibrates the on-board LOADIN/ LOADOUT synchronization circuit. MR15 of Mode Register MR1 must be set to "0."

**$\overline{\text{SYNCOUT}}$ Control (CR12):**
This bit specified whether the video $\overline{\text{SYNCOUT}}$ signal is to be enabled. On power up a "0" is written to the bit and "SYNCOUT" is set three state.




*Command Register 1 (CR1) (CR19–CR10)*

## COMMAND REGISTER 2 (CR2)
**(Address Reg (A7–A0) = 06H)**

This register contains a number of control bits as shown in the diagram. CR2 is a 10-bit wide register. However for programming purposes, it may be considered as an 8-bit wide register (CR28 and CR29 are both reserved).

The diagram shows the various operations under the control of CR2. This register can be read from as well written to. In read mode, CR28 and CR29 are both returned as zeros.

## COMMAND REGISTER 2 BIT DESCRIPTION

**P2 Trigger Polarity Control (CR20)**

This bit is used when the device is in test/diagnostic mode. It determines whether the pixel data is latched into the test registers in the rising or falling edge of P2 (see Appendix 6, "Test Diagnostics").

**$I_{PLL}$ Trigger Control (CR21)**

This bit specifies whether the $I_{PLL}$ output is triggered from $\overline{BLANK}$ or $\overline{SYNC}$.

**$\overline{SYNC}$ Recognition Control (CR22)**

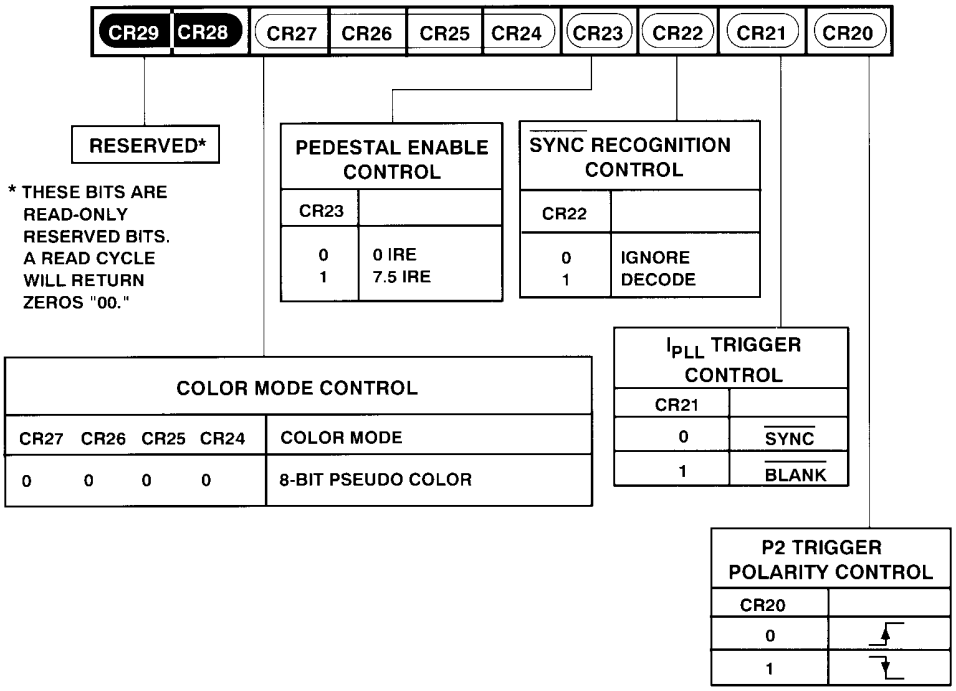
This bit specifies whether the video $\overline{SYNC}$ input is to be encoded onto the IOG analog output or ignored.

**Pedestal Enable Control (CR23)**

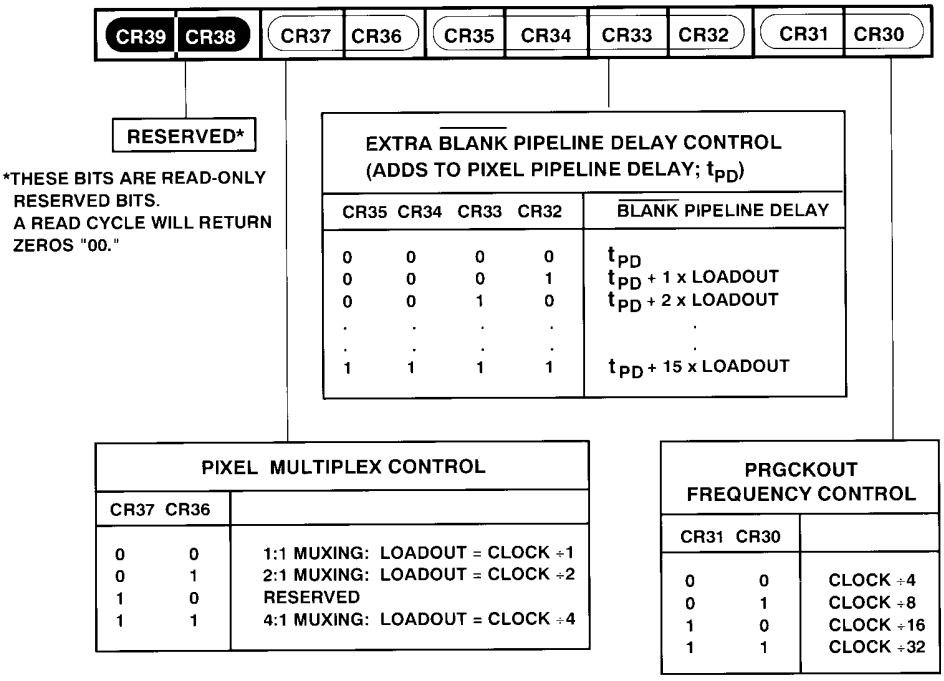
This bit specifies whether a 0 IRE or a 7.5 IRE blanking pedestal is to be generated on the video outputs.

**Color Mode Control (CR27–CR24)**

These 4 bits specify the color mode. To ensure compatibility with future products in the ADV715x product family, it is recommended that all these bits be set to a logical zero.




*Command Register 2 (CR2) (CR29–CR20)*




*Command Register 3 (CR3) (CR39–CR30)*

**COMMAND REGISTER 3 (CR3)**
**(Address Reg (A7–A0) = 07H)**
This register contains a number of control bits as shown in the diagram. CR3 is a 10-bit wide register. However for programming purposes, it may be considered as an 8-bit wide register (CR38 and CR39 are both reserved).

The diagram shows the various operations under the control of CR3. This register can be read from as well written to. In read mode, CR38 and CR39 are both returned as zeros.

**COMMAND REGISTER 3 BIT DESCRIPTION**
**PRGCKOUT Frequency Control (CR31–CR30)**
These bits specify the output frequency of the PRGCKOUT output. PRGCKOUT is a divided down version of the pixel CLOCK.

**$\overline{\text{BLANK}}$ Pipeline Delay Control (CR35–CR32)**
These bits specify the additional pipeline delay that can be added to the $\overline{\text{BLANK}}$ function, relative to the overall device pipeline delay ($t_{PD}$). As the $\overline{\text{BLANK}}$ control normally enters the video DAC from a shorter pipeline than the video pixel data, this control is useful in deskewing the pipeline differential.

**Pixel Multiplex Control (CR37–CR36)**
These bits specify the device's multiplex mode. It, therefore, also determines the frequency of the LOADOUT signal. LOADOUT is a divided down version of the pixel CLOCK.

**Revision Register**
**(Address reg (A7–A0) = 0BH):**
This register is a read only register containing the revision of silicon.

# DIGITAL-TO-ANALOG CONVERTERS (DACS) AND VIDEO OUTPUTS

The ADV7151 contains three high speed video DACs. The DAC outputs are represented as the three primary analog color signals IOR (red video), IOG (green video) and IOB (blue video). Other analog signals on the part include $I_{PLL}$ and $R_{REF}$ as well as complementary video outputs $\overline{\text{IOR}}$, $\overline{\text{IOG}}$, $\overline{\text{IOB}}$. These complementary outputs can be used to drive differentially terminated video loads, they will have equal but opposite output levels to IOR, IOG and IOB when loaded with a resistive load similar to IOR, IOG and IOB.

**DACs and Analog Outputs**
The part contains three matched 10-bit digital to analog converters. The DACs are designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either IOR, IOG, IOB (bit = "1") or $\overline{\text{IOR}}$, $\overline{\text{IOG}}$, $\overline{\text{IOB}}$ (bit = "0"). (Normally $\overline{\text{IOR}}$, $\overline{\text{IOG}}$, $\overline{\text{IOB}}$ = GND.)

The analog video outputs are high impedance current sources. Each of the these three RGB current outputs are specified to directly drive a 37.5 Ω load (doubly terminated 75 Ω).

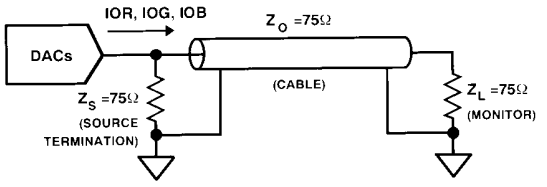



*Figure 23. DAC Output Termination (Doubly Terminated 75 Ω Load)*

**Reference Input and $R_{SET}$**

An external 1.23 V voltage reference is required to drive the analog outputs of the ADV7151. The reference voltage is connected to the $V_{REF}$ input.

A resistor $R_{SET}$ is connected between the $R_{SET}$ input of the part and ground. For specified performance, $R_{SET}$ has a value of 280 Ω. This corresponds to the generation of RS-343A video levels (with $\overline{SYNC}$ on IOG and Pedestal = 7.5 IRE) into a doubly terminated 75 Ω load. Figure 24 illustrates the resulting video waveform and the Video Output Truth Table shows the corresponding control input stimuli.

| IOR, IOB | | IOG | |
|---|---|---|---|
| mA | V | mA | V |
| 19.05 | 0.714 | 26.67 | 1.000 |
| 1.44 | 0.054 | 9.05 | 0.340 |
| 0 | 0 | 7.62 | 0.286 |
| | | 0 | 0 |

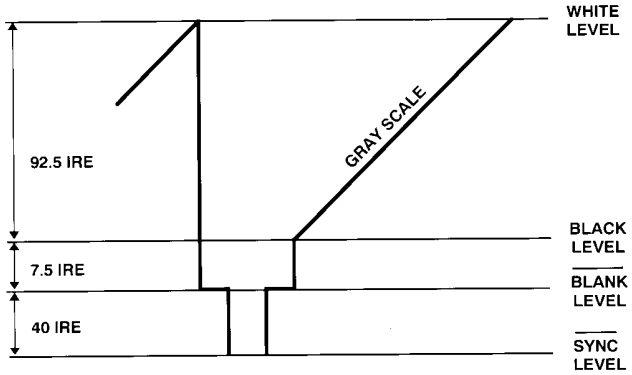



*Figure 24. Composite Video Waveform $\overline{SYNC}$ Decoded on IOG; Pedestal = IRE; $R_{SET}$ = 280 Ω*

**Table V. Video Output Truth Table**

| Description | IOG (mA) | IOR, IOB (mA) | $\overline{SYNC}$ | $\overline{BLANK}$ | DAC Input Data |
|---|---|---|---|---|---|
| WHITE LEVEL | 26.67 | 19.05 | 1 | 1 | 3FFH |
| VIDEO | Video + 9.05 | Video + 1.44 | 1 | 1 | Data |
| VIDEO to BLANK | Video + 1.44 | Video + 1.44 | 0 | 1 | Data |
| BLACK LEVEL | 9.05 | 1.44 | 1 | 1 | 000H |
| BLACK to BLANK | 1.44 | 1.44 | 0 | 1 | 000H |
| BLANK LEVEL | 7.62 | 0 | 1 | 0 | xxxH |
| $\overline{SYNC}$ LEVEL | 0 | 0 | 0 | 0 | xxxH |

**Variations on RS-343A**

Various other video output configurations can be implemented by the ADV7151, including RS-170. Values of $R_{SET}$ for particular output video formats/levels are calculated by using the equations for $R_{SET}$ given in the "Pin Configuration" section. The table shows calculated values of $R_{SET}$ for some of the most common variants on the RS-343A standard. The associated waveforms are shown in the diagrams.

**Table VI.**

| $R_{SET}$ (Ω) | Video Signal |
|---|---|
| 265 | $\overline{SYNC}$ Decoded on IOG: Pedestal = 0 IRE |
| 280 | No $\overline{SYNC}$ Decoded: Pedestal = 7.5 IRE |
| 259 | No $\overline{SYNC}$ Decoded: Pedestal = 0 IRE |

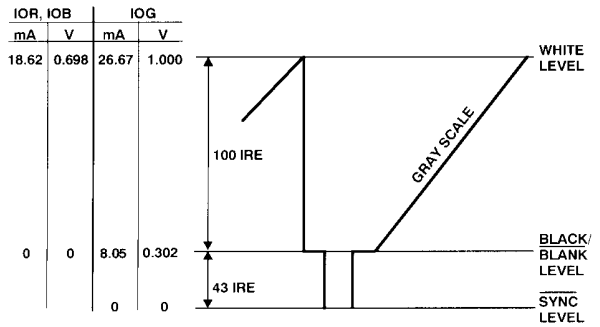



*Figure 25. Composite Video Waveform $\overline{SYNC}$ Decoded on IOG; Pedestal = 0 IRE; $R_{SET}$ = 265 Ω*

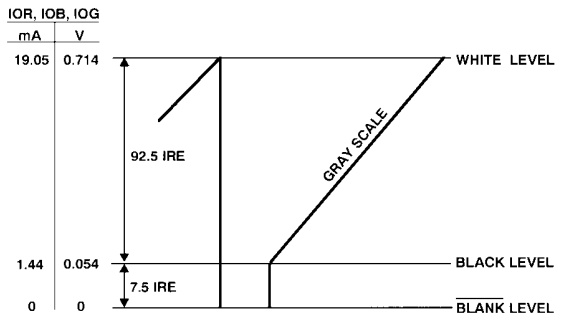



*Figure 26. Composite Video Waveform; Pedestal = 7.5 IRE; $R_{SET}$ = 280 Ω*

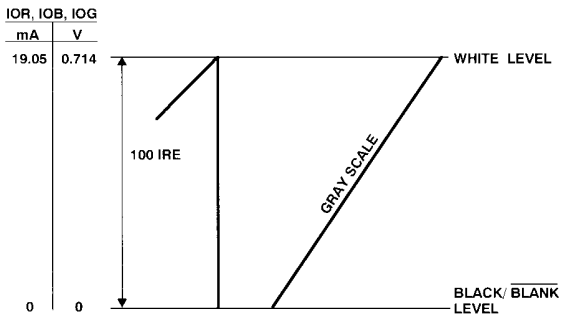



*Figure 27. Composite Video Waveform; Pedestal = 0 IRE; $R_{SET}$ = 259 Ω*

**$I_{PLL}$ Synchronization Output Control**

This output synchronization signal is used in applications where it is necessary to synchronize multiple palette devices (ADV7150 + ADV7151) to subpixel resolution. The $I_{PLL}$ output from each device is in phase with it's analog RGB output signal. If multiple devices have differing output delays, the time difference can be measured from the $I_{PLL}$ signals. This time difference is then used to phase shift the CLOCK inputs on one or other of the device inputs.

The $I_{PLL}$ signal is internally triggered by either the falling edge of $\overline{SYNC}$ or $\overline{BLANK}$ as determined by CR21 of Command Register 2.

# APPENDIX 1
## BOARD DESIGN and LAYOUT CONSIDERATIONS

The ADV7151 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design such that high speed, accurate performance is achieved. The "Recommended Analog Circuit Layout" shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV7151 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of $V_{AA}$ and GND pins should by minimized so as to minimize inductive ringing.

**Ground Planes**

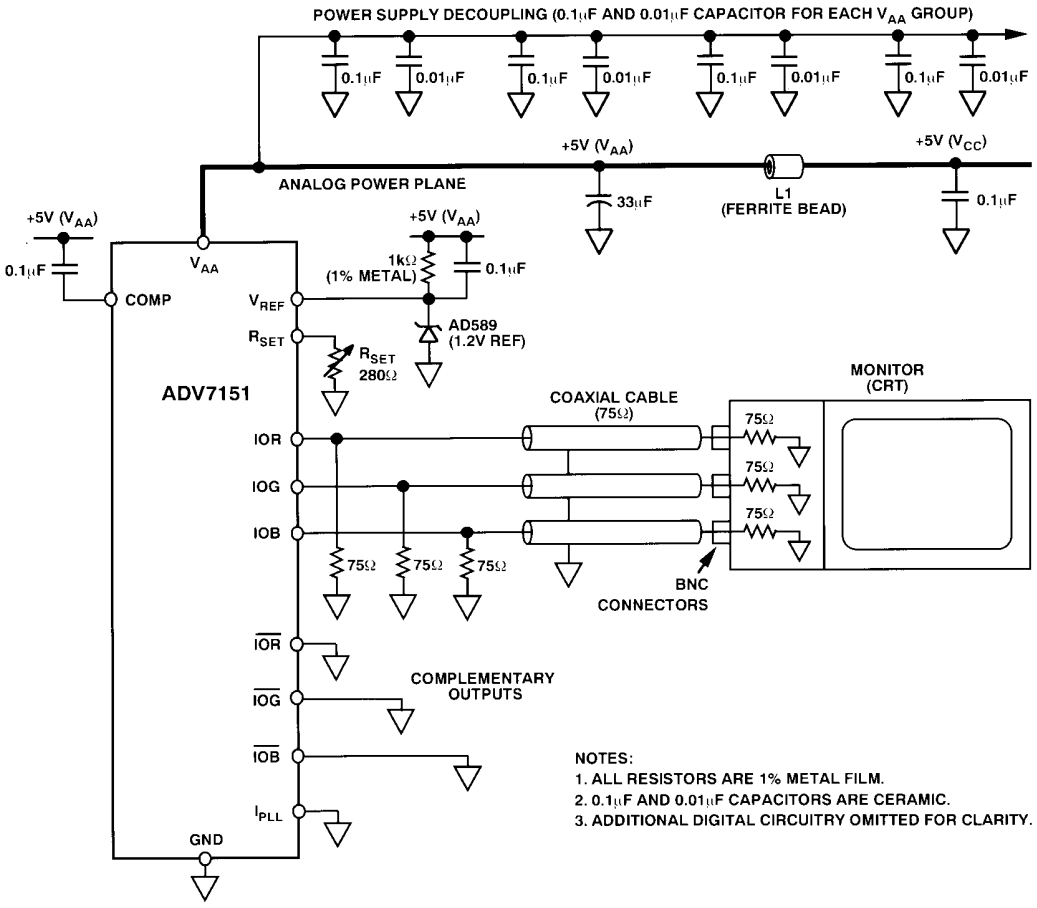
The ground plane should encompass all ADV7151 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7151, the analog output traces, and all the digital signal traces leading up to the ADV7151. The ground plane is the graphics board's common ground plane.

**Power Planes**

The ADV7151 and any associated analog circuitry should have it's own power plane, referred to as the analog power plane ($V_{AA}$). This power plane should be connected to the regular PCB power plane ($V_{CC}$) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7151.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7151 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.




*Recommended Analog Circuit Layout*

### Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 μF ceramic capacitor decoupling. Each group of $V_{AA}$ pins on the ADV7151 must have at least one 0.1 μF decoupling capacitor to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7151 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

### Digital Signal Interconnect

The digital inputs to the ADV7151 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7151 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane ($V_{CC}$), and not the analog power plane.

### Analog Signal Interconnect

The ADV7151 should be located as close as possible to the output connectors to minimize noise pick-up and reflections due to impedance mismatch.

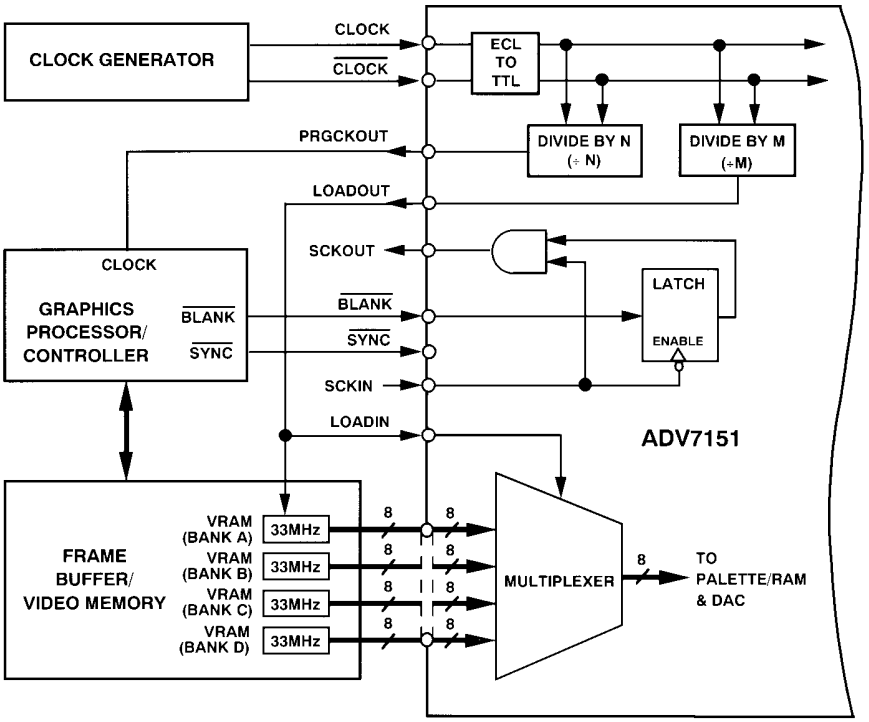
The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Digital Inputs, especially Pixel Data Inputs and clocking signals (CLOCK, LOADOUT, LOADIN etc.) should never overlay any of the analog signal circuitry and should be kept as far away as possible.

For best performance, the analog outputs (IOR, IOG, IOB) should each have a 75 Ω load resistor connected to GND. These resistors should be placed as close as possible to the ADV7151 so as to minimize reflections. Normally, the differential analog outputs ($\overline{IOR}$, $\overline{IOG}$, $\overline{IOB}$) are connected directly to GND. In some applications, improvements in performance are achieved by terminating these differential outputs with a resistive load similar in value to the video load. For a doubly terminated 75 Ω load, this means that $\overline{IOR}$, $\overline{IOG}$, $\overline{IOB}$ are each terminated with a 37.5 Ω resistor.

## APPENDIX 2

### TYPICAL FRAME BUFFER INTERFACE



# APPENDIX 3
## 10-BIT DACS AND GAMMA CORRECTION

### 10-Bit DACs

10-bit RAM-DAC resolution allows for nonlinear video correction, in particular Gamma Correction. The ADV7151 allows for an increase in color resolution from 8-bit to 10-bit effective color without the necessity of a 10-bit deep frame buffer. The part operates as an 8-bit to 10-bit color look-up table.

Up to now we have assumed that there exists a linear relationship between the actual RGB values input to a monitor and the intensity produced on the screen. This, however, is not the case. Half scale digital input (1000 0000) might correspond to only 20% output intensity on the CRT (Cathode Ray Tube). The intensity ($I_{CRT}$) produced on a CRT by an input value $I_{IN}$ is given by:

$$I_{CRT} = (I_{IN})^{\chi}$$

where $\chi$ ranges from 2.0 to 2.8.

If the individual values of $\chi$ for red, green and blue are known, then so called "Gamma Correction" can be applied to each of the three video input signals ($I_{IN}$)

therefore:

$$I_{IN(corrected)} = k(I_{IN})^{1/\chi} \qquad (k = 1, \text{ normally})$$

Traditionally, there has been a tradeoff between implementing a nonlinear graphics function, such as gamma correction, and color dynamic range. The ADV7151 overcomes this by increasing the individual color resolution of each of the red, green and blue primary colors from 8 bits per color channel to 10 bits per channel (24 bits to 30 bits).

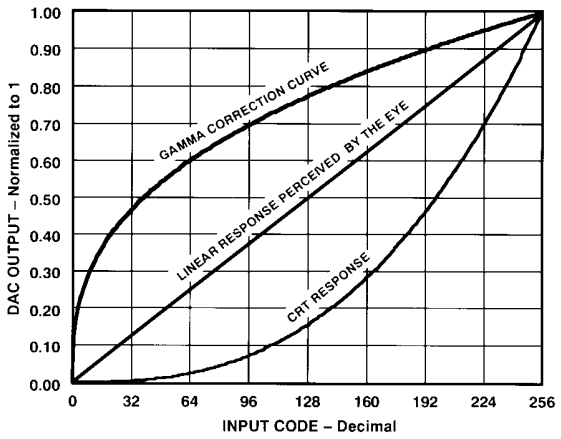
**Gamma Correction 8 Bits vs. 10 Bits**

| 8-Bit Data | Gamma Corrected (2.7) | Quantized to 8 Bits | Quantized to 10 Bits |
|---|---|---|---|
| 240 | 0.977797 | 250 | 1001 |
| 241 | 0.979304 | 250 | 1002 |
| 242 | 0.980807 | 251 | 1004 |
| 243 | 0.982306 | 251 | 1005 |
| 244 | 0.983801 | 251 | 1007 |
| 245 | 0.985292 | 252 | 1008 |
| 246 | 0.986780 | 252 | 1010 |
| 247 | 0.988264 | 252 | 1011 |
| 248 | 0.989744 | 253 | 1013 |
| 249 | 0.991220 | 253 | 1015 |
| 250 | 0.992693 | 254 | 1016 |
| 251 | 0.994161 | 254 | 1018 |
| 252 | 0.995626 | 254 | 1019 |
| 253 | 0.997088 | 255 | 1021 |
| 254 | 0.998546 | 255 | 1022 |
| 255 | 1.000000 | 255 | 1023 |

The table highlights the loss of resolution when 8-bit data is gamma-corrected to a value of 2.7 and quantized in a traditional 8-bit system. Note that there is no change in the 8-bit quantized data for linear changes in the input data over much of the transfer function. On the other hand, when quantized to 10 bits via the 10-bit RAMs and 10-bit DACs of the ADV7151, all changes on the input 8-bit data are reflected in corresponding changes in the 10-bit data.

The graph shows a typical gamma curve corresponding to a gamma value of 2.7. This is programmed to the red, green and blue RAMs of the color look-up table instead of the more traditional linear function. Different curves corresponding to any particular gamma value can be independently programmed to each of the red, green and blue RAMs.

Other applications of the 10-bit RAM-DAC include closed-loop monitor color calibration.




*Gamma Correction Curve (Gamma Value = 2.7)*

# APPENDIX 4
## MULTIPLE PALETTE APPLICATIONS

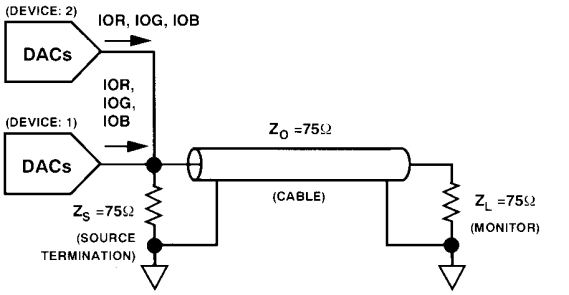
**Palette Priority Select Inputs**

The palette priority selection inputs allow up to four separate palette devices to be used in a single system to drive a single monitor. The IOR, IOG and IOB analog video output signals of each device are connected together, as shown. Signal inputs (PS0, PS1) determine on a pixel by pixel basis which palette device drives the monitor. This allows for implementation of multiple windows applications with each device acting as an independent palette. During initialization, each device is assigned two match bits, MR16 (PS0) and MR17 (PS1) in Mode Register MR1. PS0 and PS1 inputs will select one of the pre-programmed devices at any instant when PS0, PS1 matches MR16, MR17 respectively. PS0 and PS1 are multiplexed similar to the pixel data, thus allowing for subpixel resolution. The diagrams show an example of one ADV7150 (true-color RAM-DAC) operating in conjunction with three ADV7151s. Each displayed window on the monitor is driven by one of the four devices. Each device's analog output signals are connected together as shown.

Note: Only one palette device is selected at any particular instant. The analog output levels of the unselected devices will be 0 mA.

Other applications for the palette priority function using a minimum of two devices (one ADV7150 and one ADV7151) include:

Cursor Overlay on 24-Bit Graphics
Active Live Video Overlay (from Frame Grabber)
Text/Character Generation and Overlay




*Multiple Devices Termination for a Single Monitor*




*Multiple Devices Driving a Multiwindow Application*

# APPENDIX 5
## INITIALIZATION AND PROGRAMMING

### ADV7151 Initialization

After power has been supplied, the ADV7151 must be initialized. The Mode Register and Control Registers must be set. The values written to the various registers will be determined by the desired operating mode of the part, i.e., 4:1 Muxing/2:1 Muxing, etc.

The following sections give examples of initialization for the ADV7151.

***Example 1***

| | |
|---|---|
| *Color Mode:* | *8-Bit Pseudo Color* |
| *Multiplexing:* | *4:1* |
| *Databus* | *8-Bit* |
| *RAM-DAC Resolution* | *8-Bit* |
| *$\overline{SYNC}$* | *Enabled on GREEN OUT* |
| *Pedestal* | *7.5 IRE* |

| **Register Initialization** | **C1** | **C0** | **R/$\overline{W}$** | **Comment** |
|---|---|---|---|---|
| Write 09H to Mode Register (MR1) | 1 | 1 | 0 | Resets to Normal Operation, 8-Bit Bus/RAM-DAC |
| Write 08H to Mode Register (MR1) | 1 | 1 | 0 | *(Initializes Pipelining |
| Write 09H to Mode Register (MR1) | 1 | 1 | 0 | *( " |
| Write 29H to Mode Register (MR1) | 1 | 1 | 0 | *(Calibrates LOADOUT/LOADIN Timing |
| Write 09H to Mode Register (MR1) | 1 | 1 | 0 | *( " |
| Write 04H to Address Register | 0 | 0 | 0 | Address Register Points to Pixel Mask Register |
| Write FFH to Pixel Mask register | 1 | 0 | 0 | Sets the Pixel Mask to All "1s" |
| Write 05H to Address Register (A7–A0) | 0 | 0 | 0 | Address Register Points to Command Register 1 |
| Write 00H to Command Reg 1 (CR1) | 1 | 0 | 0 | |
| Write 06H to Address Register (A7–A0) | 0 | 0 | 0 | Address Register Points to Command Register 2 |
| Write 0CH to Command Reg 2 (CR2) | 1 | 0 | 0 | Sets 8-Bit Pseudo Color, 7.5 IRE, $\overline{SYNC}$ on Green |
| Write 07H to Address Register (A7–A0) | 0 | 0 | 0 | Address Register Points to Command Register 3 |
| Write C0H to Command Reg 3 (CR3) | 1 | 0 | 0 | Sets 4:1 Multiplexing, PRGCKOUT = CLOCK/4 |
| **Color Palette RAM Initialization** | **C1** | **C0** | **R/$\overline{W}$** | **Comment** |
| Write 00H to Address Register (A7–A0) | 0 | 0 | 0 | Address Register Points to Color Palette RAM |
| Write 00H (Red Data) to RAM Location (00H) | 0 | 1 | 0 | (Initializes Palette RAM |
| Write 00H (Green Data) to RAM Location (00H) | 0 | 1 | 0 | ( to a Linear Ramp** |
| Write 00H (Blue Data) to RAM Location (00H) | 0 | 1 | 0 | ( |
| Write 01H (Red Data) to RAM Location (01H) | 0 | 1 | 0 | ( |
| Write 01H (Green Data) to RAM Location (01H) | 0 | 1 | 0 | ( |
| Write 01H (Blue Data) to RAM Location (01H) | 0 | 1 | 0 | ( |
| . . . . . | . | . | . | ( |
| . . . . . | . | . | . | ( |
| Write FFH (Red Data) to RAM Location (FFH) | 0 | 1 | 0 | ( |
| Write FFH (Green Data) to RAM Location (FFH) | 0 | 1 | 0 | ( |
| Write FFH (Blue Data) to RAM Location (FFH) | 0 | 1 | 0 | (RAM Initialization Complete |

*These four command lines reset the ADV7151. The pipelines for each of the Red, Green and Blue pixel inputs are synchronously reset to the Multiplexer's "A" input. Mode Register Bit MR10 is written by a "1" followed by "0" followed by "1." LOADIN/LOADOUT timing is internally synchronized by writing a "0" followed by a "1" followed by a "0" to Mode Register MR15. The initialization must be performed in this order. These four command lines cannot be condensed into two command lines that initialize pipelining and calibrate the LOADIN/LOADOUT timing simultaneously.

**This sequence of instructions would, of course, normally be coded using some form of loop instruction.

***Example 2***

| | |
|---|---|
| Color Mode: | *8-Bit Gamma Corrected Pseudo Color (10 Bits)* |
| *Multiplexing:* | 4:1 |
| *Databus* | *10-Bit* |
| *RAM-DAC Resolution* | *10-Bit* |
| *SYNC* | *Ignored* |
| *Pedestal* | *0 IRE* |
| Calibration | Every Vertical Sync |

| **Register Initialization** | **C1** | **C0** | **R/W** | **Comment** |
|---|---|---|---|---|
| Write 0FH to Mode Register (MR1) | 1 | 1 | 0 | Resets to Normal Operation, 10-Bit Bus/RAM-DAC |
| Write 0EH to Mode Register (MR1) | 1 | 1 | 0 | *(Initializes Pipelining |
| Write 0FH to Mode Register (MR1) | 1 | 1 | 0 | *( " |
| Write 2FH to Mode Register (MR1) | 1 | 1 | 0 | *(Calibrates LOADOUT/LOADIN Timing |
| Write 0FH to Mode Register (MR1) | 1 | 1 | 0 | *( " |
| Write 04H to Address Register (A7–A0) | 0 | 0 | 0 | Address Register Points to Pixel Mask Register |
| Write FFH to Pixel Mask register | 1 | 0 | 0 | Sets the Pixel Mask to All "1s" |
| Write 05H to Address Register (A7–A0) | 0 | 0 | 0 | Address Register Points to Command Register 1 |
| Write 00H to Command Reg 1 (CR1) | 1 | 0 | 0 | Calibrates every Vertical Sync |
| Write 06H to Address Register (A7–A0) | 0 | 0 | 0 | Address Register Points to Command Register 2 |
| Write 00H to Command Reg 2 (CR2) | 1 | 0 | 0 | Sets Pseudo-Color, 0 IRE, No SYNC |
| Write 07H to Address Register (A7–A0) | 0 | 0 | 0 | Address Register Points to Command Register 3 |
| Write C1H to Command Reg 3 (CR2) | 1 | 0 | 0 | Sets 4:1 Multiplexing, PRGCKOUT = CLOCK/8 |
| **Color Palette RAM Initialization** | **C1** | **C0** | **R/W** | **Comment** |
| Write 00H to Address Register (A7–A0) | 0 | 0 | 0 | Address Register Points to Color Palette RAM |
| Write 000H (Red Data) to RAM Location (00H) | 0 | 1 | 0 | (Initializes Palette RAM |
| Write 000H (Green Data) to RAM Location (00H) | 0 | 1 | 0 | ( to a "Gamma" Ramp |
| Write 000H (Blue Data) to RAM Location (00H) | 0 | 1 | 0 | ( |
| Write xxxH (Red Data) to RAM Location (01H) | 0 | 1 | 0 | ( |
| Write xxxH (Green Data) to RAM Location (01H) | 0 | 1 | 0 | ( |
| Write xxxH (Blue Data) to RAM Location (01H) | 0 | 1 | 0 | ( |
| . . . . . | . | . | . | ( |
| . . . . . | . | . | . | ( |
| Write 3FFH (Red Data) to RAM Location (FFH) | 0 | 1 | 0 | ( |
| Write 3FFH (Green Data) to RAM Location (FFH) | 0 | 1 | 0 | ( |
| Write 3FFH (Blue Data) to RAM Location (FFH) | 0 | 1 | 0 | (RAM Initialization Complete |

*These four command lines reset the ADV7151. The pipelines for each of the Red, Green and Blue pixel inputs are synchronously reset to the Multiplexer's "A" input. Mode Register Bit MR10 is written by a "1" followed by "0" followed by "1." LOADIN/LOADOUT timing is internally synchronized by writing a "0" followed by a "1" followed by a "0" to Mode Register MR15. The initialization must be performed in this order. These four command lines cannot be condensed into two command lines that initialize pipelining and calibrate the LOADIN/LOADOUT timing simultaneously.

## REGISTER DIAGNOSTIC TESTING

The previous examples show the register initialization sequence for the ADV7151. These show control data going to the registers and palette RAM. As well as this writing function, it may also be necessary, due to system diagnostic requirements, to confirm that correct data has been transferred to each register and palette RAM location. There are two ways to incorporate register value/RAM value checking.

1. *READ after each WRITE.* After data is written to a particular register, it can be read back immediately. The following table shows an example with Command Registers CR2 and CR3.

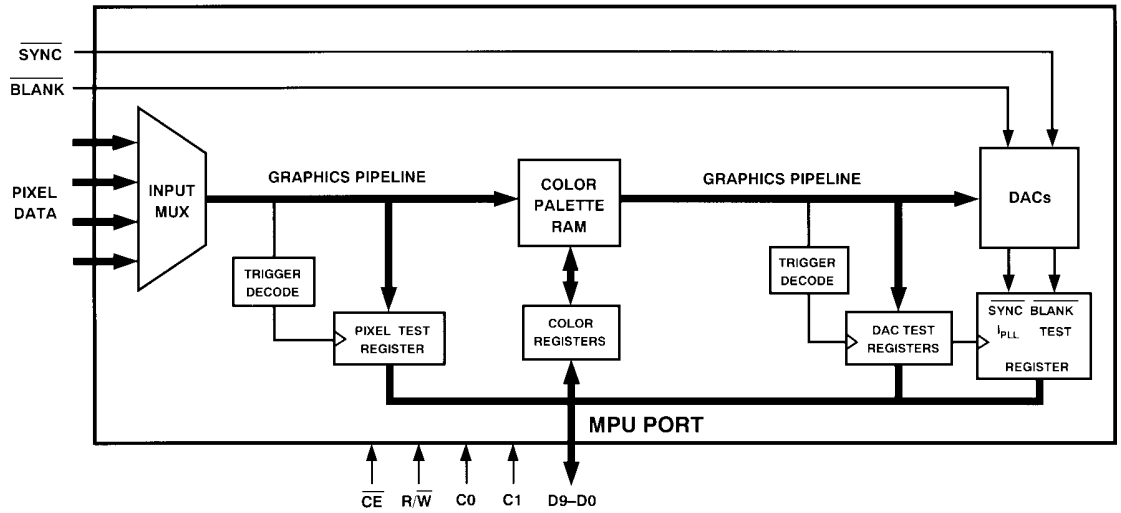
| C1 | C0 | R/W | D0–D7 | Comment |
|---|---|---|---|---|
| 0 | 0 | 0 | 06H | Select Command Register 2 (CR2) |
| 1 | 0 | 0 | 00H | Sets 8-Bit Pseudo-Color, No Pedestal, SYNC Not Recognized |
| 1 | 0 | 1 | 00H | *Command Reg 2 Value Read-Back* |
| 0 | 0 | 0 | 07H | Select Command Register 3 (CR3) |
| 1 | 0 | 0 | 40H | Set 2:1 Mux Mode |
| 1 | 0 | 1 | 40H | *Command Reg 3 Value Read-Back* |

2. *READ after all WRITEs completed.* All registers and the color palette RAM are written to and set. Once this is complete, all registers are again accessed but this time in Read-Only mode. The table below shows this method for Command Registers CR2 and CR3.

| C1 | C0 | R/W | D0–D7 | Comment |
|---|---|---|---|---|
| 0 | 0 | 0 | 06H | Select Command Register 2 (CR2) |
| 1 | 0 | 0 | 00H | Sets 8-Bit Pseudo-Color, No Pedestal, SYNC Not Recognized |
| 0 | 0 | 0 | 07H | Select Command Register 3 (CR3) |
| 1 | 0 | 0 | 40H | Set 2:1 Mux Mode |
| 0 | 0 | 0 | 06H | *Select CR2* |
| 1 | 0 | 1 | 00H | *CR2 Value Read-Back* |
| 0 | 0 | 0 | 07H | *Select CR3* |
| 1 | 0 | 1 | 40H | *CR3 Value Read-Back* |

It is clear that this latter case requires more command lines than the previous READ after each WRITE case.

# APPENDIX 6
## TEST DIAGNOSTICS




*Test/Diagnostic Block Diagram*

The ADV7151 contains on-board circuitry which enables both device and system level test diagnostics. The test circuitry can be used to test the frame buffer memory as well as the functionality of the ADV7151. A number of test registers are integrated into the part which effectively allow for monitoring of the graphics pipeline. Pixel data is read from the graphics pipeline independent of the pixel CLOCK. The pixel data itself contains the triggering information that latches data into the test registers. This allows for system diagnostics in a continuously clocked graphics system. The test register data is then read by the microprocessor over the MPU.

Access to the test registers is as described in the "Microprocessor (MPU) Port" section. This section also gives the address decode locations for the various test registers.

**Test Trigger (P2)**
The test trigger is decoded from the pixel data stream. Bit P2 [A-D] is assigned the task of latching pixel data into the test registers. A "0" to "1" or a "1" to "0" (as determined by bit CR20 of Command Register 2) transition on P2, fills the test register with the corresponding pixel data. This effectively means that a sequence of data travels along the graphics pipeline, with the test registers taking a sample only when there is a transition on bit P2. The following example shows a sequence with the ADV7151 preset to sample the graphics pipeline on a low to high transition of P2.

| | | |
|---|---|---|
| Pixel 0: | . . . . . 0000 | |
| Pixel 1: | . . . . . 0000 | |
| Pixel 2: | . . . . . 0000 | |
| Pixel 3: | . . . . . 0100 | Pixel 3 Latched to Test Register |
| Pixel 4: | . . . . . 0000 | |
| . . . . | . . . | |
| . . . . | . . . | |
| Pixel n-1: | . . . . . 1011 | |
| Pixel n: | . . . . . 1111; | Pixel n Latched to Test Register |
| Pixel n+1: | . . . . . 1111 | |

In the above sequence of pixels, there is a rising edge on P2 on Pixel 3. The data for Pixel 3 therefore gets latched into the Pixel Test Register. Pixel 3 continues down the graphics pipeline and after a number of clocks gets latched into the DAC Test Register. This data can then be read from the Pixel Test Register and the DAC Test Registers over the MPU Port. This data will remain in the Pixel Test Registers and the DAC Test Registers until the next rising edge of P2 causes new data to be latched in.

In the above example, the next rising edge of P2 occurs on the Pixel n input. Therefore the data in the Pixel Test Registers and DAC Test Registers must be read over the MPU before the Pixel n data is applied, otherwise they will be overwritten by the Pixel n data and the Pixel 3 data will be lost.

**Pixel Test Register**
The read-only Pixel Test Register is 8 bits wide. It is situated directly after the Pixel Mask Register. After data is latched into this register by a transition on P2, it is read in three cycles over the MPU Port as described in the "Microprocessor (MPU) Port" section.

**DAC Test Register**
The DAC Test Register is latched with data some CLOCKs after the Pixel Test Register. The DAC Test Register is a 30-bit wide read-only register, corresponding to 10 bits each for red, green and blue data. It is located after the Color Palette RAM. If the RAM-DAC is in 8-bit resolution mode, the upper two bits of the red green and blue data will be zero. After data is latched into the DAC Test Register by a transition on P2, it is read in three or six cycles over the MPU Port as described in the "Microprocessor (MPU) Port" section.

**$\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and $I_{PLL}$ Test Register**
This is an 8-bit wide register but with only three effective bits. The three lower bits correspond to $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and $I_{PLL}$ respectively. The upper bits should be masked in software. This register is at the same position in the graphics pipeline as the DAC Test Register. When pixel data is latched into the DAC Test Register, the corresponding status of $\overline{\text{SYNC}}$, $\overline{\text{BLANK}}$ and $I_{PLL}$ is latched into this register. It is read over the MPU Port as described in the "Microprocessor (MPU) Port" section.

(Note: If $\overline{\text{BLANK}}$ is low, the corresponding pixel data to the DAC Test Register will be all "0s".)

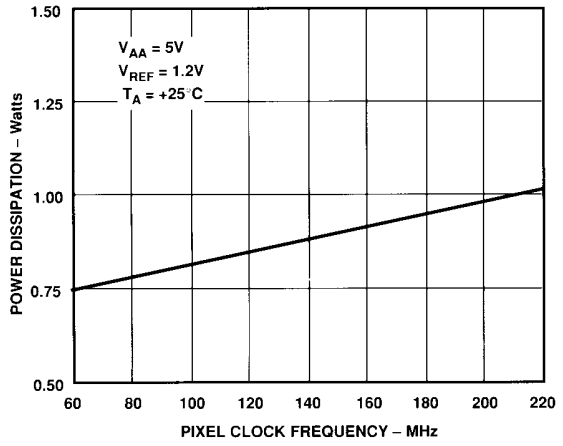
# APPENDIX 7
## THERMAL AND ENVIRONMENTAL CONSIDERATIONS

The ADV7151 is a very highly integrated monolithic silicon device. This high level of integration, in such a small package, inevitably leads to consideration of thermal and environmental conditions in which the ADV7151 must operate. Reliability of the device is significantly enhanced by keeping it as cool as possible. In order to avoid destructive damage to the device, the absolute maximum junction temperature of 150°C must never be exceeded. Certain applications, depending on pixel data rates, may require forced air cooling or external heatsinks. The following data is intended as a guide in evaluating the operating conditions of a particular application so that optimum device and system performance is achieved.

*It should be noted that information on package characteristics published herein may not be the most up to date at the time of reading this. Advances in package compounds and manufacture will inevitably lead to improvements in the thermal data. Please contact your local sales office for the most up-to-date information.*

### Power Dissipation

The diagram shows graphs of power dissipation in watts versus pixel clock frequency for the ADV7151.




* THE "WORST CASE ON-SCREEN PATTERN" CORRESPONDS TO FULL SCALE TRANSITION ON EACH PIXEL VALUE FOR EVERY CLOCK EDGE (00H, FFH, 00H,....).
THE "TYPICAL ON-SCREEN PATTERN" CORRESPONDS TO LINEAR CHANGES IN THE PIXEL INPUT (I.E., A BLACK TO WHITE RAMP). IN GENERAL, COLOR IMAGES TEND TO APPROXIMATE THIS CHARACTERISTIC.

*Typical Power Dissipation vs. Pixel Rate*

### Package Characteristics

The table of thermal characteristics shows typical information for the ADV7151 (100-Lead Plastic Power QFP) using various values of airflow.

Junction to Case ($\theta_{JC}$). Thermal resistance for this particular part is:

$\theta_{JC}$ (100-Lead Plastic Power QFP) = 1.0 °C/W
*(Note: $\theta_{JC}$ is independent of airflow.)*

**Table A. Thermal Characteristics vs. Airflow**

| Air Velocity (Linear feet/min) | 0 (Still Air) | 50 | 100 | 200 |
|---|---|---|---|---|
| $\theta_{JA}$ (°C/W) | | | | |
| No Heatsink | 35 | 31 | 28 | 25 |
| EG&G D10100-28 Heatsink | 32 | 28 | 25 | 22 |
| Thermalloy 2290 Heatsink | 25 | 21 | 18 | 15 |

The junction temperature of the device in a specific application is given by:

$$T_J = T_A + P_D (\theta_{JC} + \theta_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D (\theta_{JA}) \quad (2)$$

where:

$T_J$ = Junction Temperature of Silicon (°C)
$T_A$ = Ambient Temperature (°C)
$P_D$ = Power Dissipation (W)
$\theta_{JC}$ = Junction to Case Thermal Resistance (°C/W)
$\theta_{CA}$ = Case to Ambient Thermal Resistance (°C/W)
$\theta_{JA}$ = Junction to Ambient Thermal Resistance (°C/W)

### Package Enhancements

The standard QFP package has been enhanced to a PowerQuad2 package. This supports an improved thermal performance compared to standard QFP. In this case, the die is attached to a heatslug so that the power that is dissipated can be conducted to the external surface of the package. This provides a highly efficient path for the transfer of heat to the package surface. The package configuration also provides an efficient thermal path from the ADV7151 to the Printed Circuit Board via the leads.

### Heatsinks

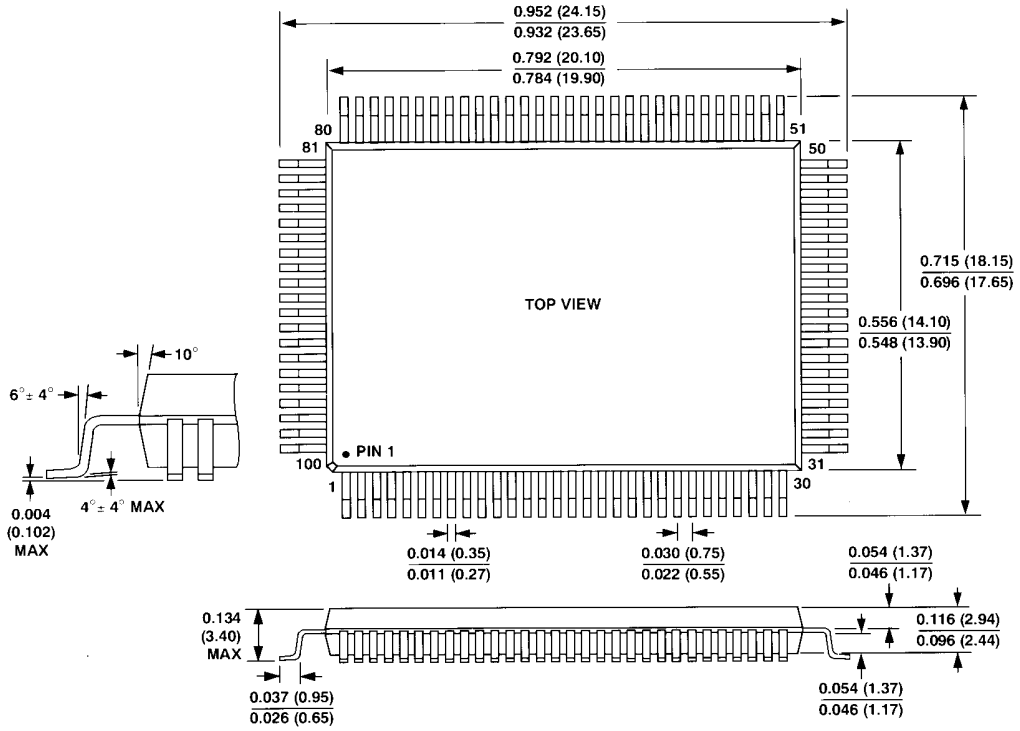
The maximum silicon junction temperature should be limited to 100°C. Temperatures greater than this will reduce long term device reliability. To ensure that the silicon junction temperature stays within prescribed limits, the addition of an external heatsink may be necessary. Heatsinks, will reduce $\theta_{JA}$ as shown in the "Thermal Characteristics vs. Airflow" table.

# APPENDIX 8

## PACKAGE OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 100-Lead Plastic Quad Flatpack
### S-100

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