

### FEATURES

- **Extremely Tight Matching**
- **Excellent Individual Amplifier Parameters**
- **Offset Voltage Match** ..... **0.18mV Max**
- **Offset Voltage Match vs Temp.** ..... **0.8 $\mu$ V/ $^{\circ}$ C Max**
- **Common-Mode Rejection Match** ..... **114dB Min**
- **Power Supply Rejection Match** ..... **100dB Min**
- **Bias Current Match** ..... **3.0nA Max**
- **Low Noise** ..... **0.6 $\mu$ V<sub>p-p</sub> Max**
- **Low Bias Current** ..... **3.0nA Max**
- **High Common-Mode Input Impedance** .... **200G $\Omega$  Typ**
- **Excellent Channel Separation** ..... **126dB Min**

### ORDERING INFORMATION†

$T_A = 25^{\circ}\text{C}$ $V_{OS}$ MAX (mV)	HERMETIC DIP 14-PIN	OPERATING TEMPERATURE RANGE
0.5	OP10AY*	MIL
0.5	OP10EY	COM
0.5	OP10Y*	MIL
0.5	OP10CY	COM

\* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages.

### GENERAL DESCRIPTION

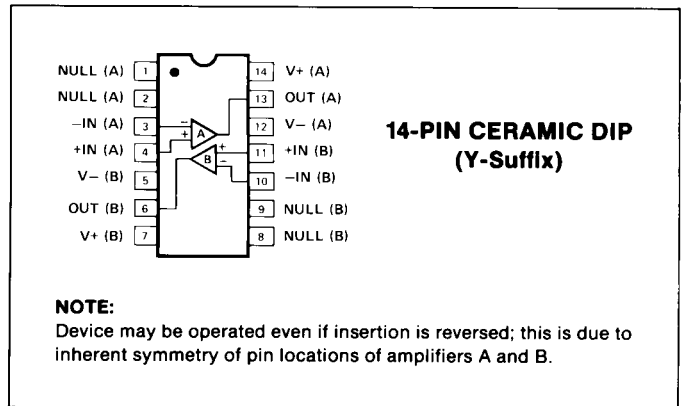
The OP-10 series of dual-matched instrumentation operational amplifiers consists of two independent monolithic high-performance operational amplifiers in a single 14-pin dual-in-line package. Tight matching of critical parameters

is provided between channels of the dual operational amplifier.

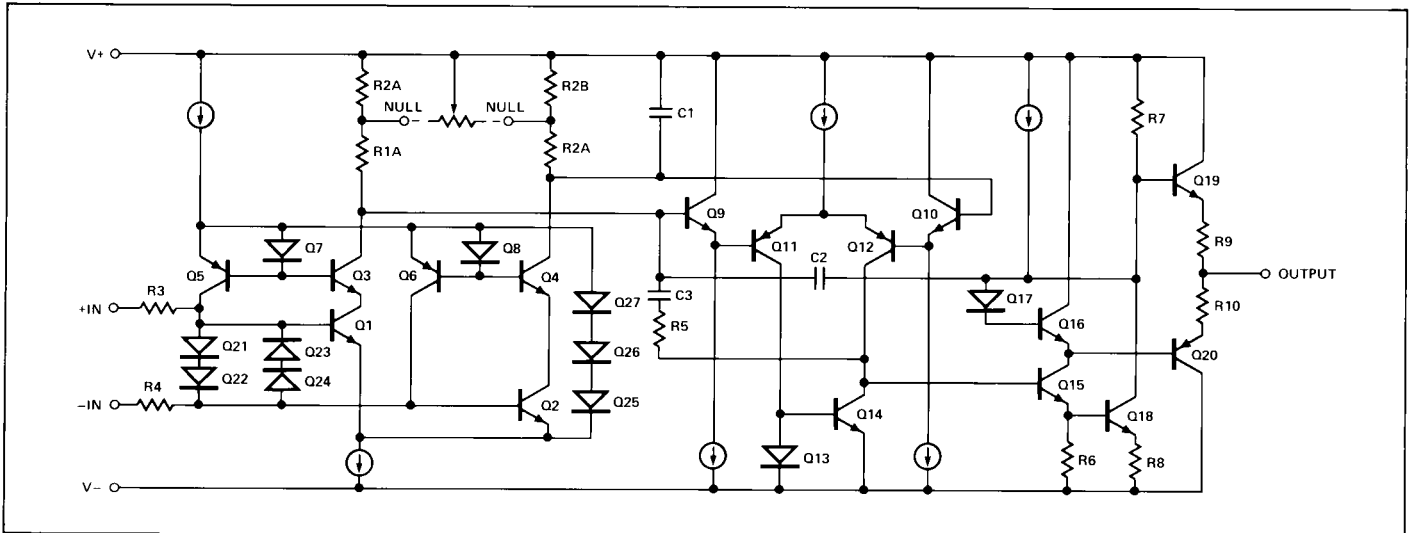
The excellent specifications of the individual amplifiers and tight matching over temperature enable construction of high-performance instrumentation amplifiers. The designer can achieve the guaranteed specifications because the common package eliminates temperature differentials which occur in designs using separately housed amplifiers.

Matching between channels is provided on all critical parameters including offset voltage, tracking of offset voltage vs. temperature, noninverting bias currents, and common-mode and power-supply rejection ratios. The individual amplifiers feature extremely low offset voltage, offset voltage drift, low noise voltage, low bias current, internal compensation and input/output protection.

### PIN CONNECTIONS



### SIMPLIFIED SCHEMATIC (1/2 OP-10)



# OP-10

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage .....	±22V
Differential Input Voltage .....	±30V
Input Voltage (Note 1) .....	±22V
Output Short-Circuit Duration .....	Indefinite
Storage Temperature Range .....	-65°C to +150°C
Operating Temperature Range	
OP-10A, OP-10 .....	-55°C to +125°C
OP-10E, OP-10C .....	0°C to +70°C

DICE Junction Temperature (T <sub>J</sub> ) .....	-65°C to +150°C
Lead Temperature Range (Soldering, 60 sec) .....	+300°C

PACKAGE TYPE	Θ <sub>JA</sub> (NOTE 2)	Θ <sub>JC</sub>	UNITS
14-Pin Hermetic DIP (Y)	108	16	°C/W

### NOTES:

- For supply voltages less than +22V, the absolute maximum input voltage is equal to the supply voltage.
- Θ<sub>JA</sub> is specified for worst case mounting conditions, i.e., Θ<sub>JA</sub> is specified for device in socket for CerDIP package.

## INDIVIDUAL AMPLIFIER CHARACTERISTICS at V<sub>S</sub> = ±15V, T<sub>A</sub> = 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	V <sub>OS</sub>		—	0.2	0.5	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	ΔV <sub>OS</sub> /Time	(Notes 1, 2)	—	0.25	1.0	—	0.25	1.0	μV/Mo
Input Offset Current	I <sub>OS</sub>		—	1.0	2.8	—	1.0	2.8	nA
Input Bias Current	I <sub>B</sub>		—	±1	±3	—	±1	±3	nA
Input Noise Voltage	e <sub>np-p</sub>	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.35	0.6	μV <sub>p-p</sub>
Input Noise Voltage Density	e <sub>n</sub>	f <sub>O</sub> = 10Hz	—	10.3	18.0	—	10.3	18.0	nV/√Hz
		(Note 2) f <sub>O</sub> = 100Hz	—	10.0	13.0	—	10.0	13.0	
		f <sub>O</sub> = 1000Hz	—	9.6	11.0	—	9.6	11.0	
Input Noise Current	i <sub>np-p</sub>	(Note 2) 0.1Hz to 10Hz	—	14	30	—	14	30	pA <sub>p-p</sub>
Input Noise Current Density	i <sub>n</sub>	f <sub>O</sub> = 10Hz	—	0.32	0.80	—	0.32	0.80	pA/√Hz
		(Note 2) f <sub>O</sub> = 100Hz	—	0.14	0.23	—	0.14	0.23	
		f <sub>O</sub> = 1000Hz	—	0.12	0.17	—	0.12	0.17	
Input Resistance — Differential-Mode	R <sub>IN</sub>	(Note 3)	20	60	—	20	60	—	MΩ
Input Resistance — Common-Mode	R <sub>INCM</sub>		—	200	—	—	200	—	GΩ
Input Voltage Range	IVR		±13	±14	—	±13	±14	—	V
Common-Mode Rejection Ratio	CMRR	V <sub>CM</sub> = ±13V	110	126	—	110	126	—	dB
Power Supply Rejection Ratio	PSRR	V <sub>S</sub> = ±3V to ±18V	—	4	10	—	4	10	μV/V
Large-Signal Voltage Gain	A <sub>VO</sub>	R <sub>L</sub> ≥ 2kΩ, V <sub>O</sub> = ±10V	200	500	—	200	500	—	V/mV
		R <sub>L</sub> ≥ 500Ω, V <sub>O</sub> = ±0.5V, V <sub>S</sub> = ±3V (Note 3)	150	500	—	150	500	—	
Output Voltage Swing	V <sub>O</sub>	R <sub>L</sub> ≥ 10kΩ	±12.5	±13.0	—	±12.5	±13.0	—	V
		R <sub>L</sub> ≥ 2kΩ	±12.0	±12.8	—	±12.0	±12.8	—	
		R <sub>L</sub> ≥ 1kΩ	±10.5	±12.0	—	±10.5	±12.0	—	
Slew Rate	SR	R <sub>L</sub> ≥ 2kΩ	—	0.17	—	—	0.17	—	V/μs
Closed-Loop Bandwidth	BW	A <sub>VCL</sub> = +1.0	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	R <sub>O</sub>	V <sub>O</sub> = 0, I <sub>O</sub> = 0	—	60	—	—	60	—	Ω
Power Consumption	P <sub>d</sub>	Each Amplifier	—	90	120	—	90	120	mW
		V <sub>S</sub> = ±3V	—	4	6	—	4	6	
Offset Adjustment Range		R <sub>P</sub> = 20kΩ	—	±4	—	—	±4	—	mV
Input Capacitance	C <sub>IN</sub>		—	8	—	—	8	—	pF

### NOTES:

- Long-Term Input Offset Voltage Stability refers to the averaged trend line of V<sub>OS</sub> vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V<sub>OS</sub> during the first 30 operating days are typically 2.5μV — refer to typical performance curves.
- Sample tested.
- Guaranteed by design.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq +125^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	0.3	0.7	—	0.3	0.7	mV
Average Input Offset Voltage Drift									
Without External Trim	$TCV_{OS}$	(Note 2)	—	0.7	2.0	—	0.7	2.0	$\mu V/^\circ C$
With External Trim	$TCV_{OSn}$	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.0	—	0.3	1.0	$\mu V/^\circ C$
Input Offset Current	$I_{OS}$		—	1.8	5.6	—	1.8	5.6	nA
Average Input Offset Current Drift	$TCI_{OS}$	(Note 2)	—	8	50	—	8	50	$pA/^\circ C$
Input Bias Current	$I_B$		—	$\pm 2$	$\pm 6$	—	$\pm 2$	$\pm 6$	nA
Average Input Bias Current Drift	$TCI_B$	(Note 2)	—	13	50	—	13	50	$pA/^\circ C$
Input Voltage Range	IVR		$\pm 13.0$	$\pm 13.5$	—	$\pm 13.0$	$\pm 13.5$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	106	123	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	5	20	—	5	20	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	150	400	—	150	400	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12.0$	$\pm 12.6$	—	$\pm 12.0$	$\pm 12.6$	—	V

**MATCHING CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$\Delta V_{OS}$		—	0.07	0.18	—	0.12	0.5	mV
Average Noninverting Bias Current	$I_{B^+}$		—	$\pm 1.0$	$\pm 3.0$	—	$\pm 1.3$	$\pm 4.5$	nA
Noninverting Offset Current	$I_{OS^+}$		—	0.8	2.8	—	1.1	4.5	nA
Inverting Offset Current	$I_{OS^-}$		—	0.8	2.8	—	1.1	4.5	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	114	123	—	106	120	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	3	10	—	4	20	$\mu V/V$
Channel Separation	CS	(Note 2)	126	140	—	126	140	—	dB

**MATCHING CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq +125^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	$\Delta V_{OS}$		—	0.1	0.3	—	0.2	0.9	mV
Input Offset Voltage Tracking									
Without External Trim	$TC\Delta V_{OS}$	(Note 2)	—	0.45	1.3	—	0.9	2.5	$\mu V/^\circ C$
With External Trim	$TC\Delta V_{OSn}$	$R_P = 20k\Omega$ (Note 3) Channel A only	—	0.3	0.8	—	0.4	1.2	$\mu V/^\circ C$

**NOTES:**

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically  $2.5\mu V$  — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

# OP-10

**MATCHING CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $-55^\circ C \leq T_A \leq +125^\circ C$ , unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-10A			OP-10			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Average Noninverting Bias Current	$I_{B^+}$		—	$\pm 2.0$	$\pm 6.0$	—	$\pm 2.4$	$\pm 8.0$	nA
Average Drift of Noninverting Bias Current	$TCI_{B^+}$	(Note 2)	—	10	40	—	15	—	$\mu A/^\circ C$
Noninverting Offset Current	$I_{OS^+}$		—	2.0	6.5	—	2.4	9.0	nA
Average Drift of Noninverting Offset Current	$TCI_{OS^+}$	(Note 2)	—	12	50	—	18	—	$\mu A/^\circ C$
Inverting Offset Current	$I_{OS^-}$		—	2.0	6.5	—	2.4	9.0	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	108	120	—	103	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	6	20	—	7	32	$\mu V/V$

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	0.2	0.5	—	0.2	0.5	mV
Long-Term Input Offset Voltage Stability	$\Delta V_{OS}/\text{Time}$	(Notes 1, 2)	—	0.3	1.5	—	0.5	—	$\mu V/\text{Mo}$
Input Offset Current	$I_{OS}$		—	1.2	3.8	—	1.8	6.0	nA
Input Bias Current	$I_B$		—	$\pm 1.2$	$\pm 4.0$	—	$\pm 1.8$	$\pm 7.0$	nA
Input Noise Voltage	$e_{np-p}$	(Note 2) 0.1Hz to 10Hz	—	0.35	0.6	—	0.38	0.65	$\mu V_{p-p}$
Input Noise Voltage Density	$e_n$	$f_O = 10\text{Hz}$	—	10.3	18.0	—	10.5	20.0	$nV/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	10.0	13.0	—	10.2	13.5	
		$f_O = 1000\text{Hz}$	—	9.6	11.0	—	9.8	11.5	
Input Noise Current	$i_{np-p}$	(Note 2) 0.1Hz to 10Hz	—	14	30	—	15	35	$\mu A_{p-p}$
Input Noise Current Density	$i_n$	$f_O = 10\text{Hz}$	—	0.32	0.80	—	0.35	0.90	$\mu A/\sqrt{\text{Hz}}$
		$f_O = 100\text{Hz}$	—	0.14	0.23	—	0.15	0.27	
		$f_O = 1000\text{Hz}$	—	0.12	0.17	—	0.13	0.18	
Input Resistance — Differential-Mode	$R_{IN}$	(Note 3)	15	50	—	8	33	—	M $\Omega$
Input Resistance — Common-Mode	$R_{INCM}$		—	160	—	—	120	—	G $\Omega$
Input Voltage Range	IVR		$\pm 13$	$\pm 14$	—	$\pm 13$	$\pm 14$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	106	123	—	100	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	10	32	$\mu V/V$
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega$ , $V_O = \pm 10V$	200	500	—	120	400	—	V/mV
		$R_L \geq 500\Omega$ , $V_O = \pm 0.5V$ , $V_S = \pm 3V$ (Note 3)	150	500	—	100	400	—	
Output Voltage Swing	$V_O$	$R_L \geq 10k\Omega$	$\pm 12.5$	$\pm 13.0$	—	$\pm 12.0$	$\pm 13.0$	—	V
		$R_L \geq 2k\Omega$	$\pm 12.0$	$\pm 12.8$	—	$\pm 11.5$	$\pm 12.8$	—	
		$R_L \geq 1k\Omega$	$\pm 10.5$	$\pm 12.0$	—	—	$\pm 12.0$	—	

**NOTES:**

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically  $2.5\mu V$  — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq +70^\circ C$ , unless otherwise noted. (Continued)

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Slewing Rate	SR	$R_L \geq 2k\Omega$	—	0.17	—	—	0.17	—	V/ $\mu$ s
Closed-Loop Bandwidth	BW	$A_{VCL} = +1.0$	—	0.6	—	—	0.6	—	MHz
Open-Loop Output Resistance	$R_O$	$V_O = 0, I_O = 0$	—	60	—	—	60	—	$\Omega$
Power Consumption	$P_d$	Each Amplifier $V_S = \pm 3V$	—	90	120	—	95	150	mW
Offset Adjustment Range		$R_P = 20k\Omega$	—	$\pm 4$	—	—	$\pm 4$	—	mV
Input Capacitance	$C_{IN}$		—	8	—	—	8	—	pF

**INDIVIDUAL AMPLIFIER CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq +70^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$V_{OS}$		—	0.25	0.6	—	0.35	1.6	mV
Average Input Offset Voltage Drift									
Without External Trim	$TCV_{OS}$	(Note 2)	—	0.7	2.0	—	1.2	4.5	$\mu$ V/ $^\circ$ C
With External Trim	$TCV_{OSn}$	$R_P = 20k\Omega$ (Note 3)	—	0.3	1.0	—	0.4	1.5	$\mu$ V/ $^\circ$ C
Input Offset Current	$I_{OS}$		—	1.4	5.3	—	2.0	8.0	nA
Average Input Offset Current Drift	$TCI_{OS}$	(Note 2)	—	8	50	—	12	50	pA/ $^\circ$ C
Input Bias Current	$I_B$		—	$\pm 1.5$	$\pm 5.5$	—	$\pm 2.2$	$\pm 9.0$	nA
Average Input Bias Current Drift	$TCI_B$	(Note 2)	—	13	50	—	18	50	pA/ $^\circ$ C
Input Voltage Range	IVR		$\pm 13.0$	$\pm 13.5$	—	$\pm 13.0$	$\pm 13.5$	—	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm 13V$	103	123	—	97	120	—	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm 3V$ to $\pm 18V$	—	7	32	—	10	51	$\mu$ V/V
Large-Signal Voltage Gain	$A_{VO}$	$R_L \geq 2k\Omega, V_O = \pm 10V$	100	400	—	100	400	—	V/mV
Output Voltage Swing	$V_O$	$R_L \geq 2k\Omega$	$\pm 12.0$	$\pm 12.6$	—	$\pm 11.0$	$\pm 12.6$	—	V

**NOTES:**

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of  $V_{OS}$  vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in  $V_{OS}$  during the first 30 operating days are typically  $2.5\mu$ V — refer to typical performance curves.
2. Sample tested.
3. Guaranteed by design.

# OP-10

**MATCHING CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $T_A = 25^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	$\Delta V_{OS}$		—	0.12	0.5	—	0.3	—	mV
Average Noninverting Bias Current	$I_{B^+}$		—	$\pm 1.3$	$\pm 4.5$	—	$\pm 2.0$	—	nA
Noninverting Offset Current	$I_{OS^+}$		—	1.1	4.5	—	1.8	—	nA
Inverting Offset Current	$I_{OS^-}$		—	1.1	4.5	—	1.8	—	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	106	120	—	—	117	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	4	20	—	5	—	$\mu V/V$
Channel Separation	CS	(Note 1)	126	140	—	120	137	—	dB

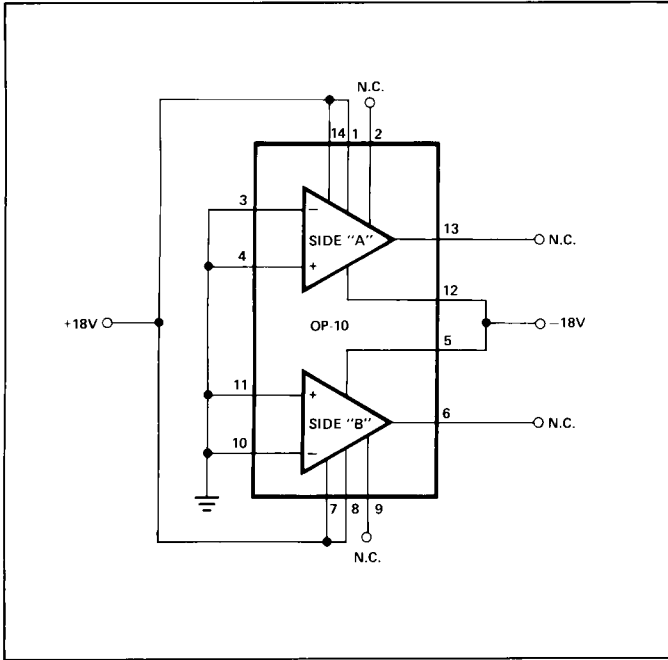
**MATCHING CHARACTERISTICS** at  $V_S = \pm 15V$ ,  $0^\circ C \leq T_A \leq +70^\circ C$ , unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-10E			OP-10C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage Match	$\Delta V_{OS}$		—	0.18	0.7	—	0.4	—	mV
Input Offset Voltage Tracking Without External Trim	$TC\Delta V_{OS}$	(Note 1)	—	0.9	2.3	—	1.3	—	$\mu V/^\circ C$
With External Trim	$TC\Delta V_{OSn}$	$R_L = 20k\Omega$ Channel A Only (Note 2)	—	0.3	0.9	—	0.6	—	$\mu V/^\circ C$
Average Noninverting Bias Current	$I_{B^+}$		—	$\pm 2.0$	$\pm 6.0$	—	$\pm 2.8$	—	nA
Average Drift of Noninverting Bias Current	$TCI_{B^+}$	(Note 1)	—	12	40	—	18	—	$pA/^\circ C$
Noninverting Offset Current	$I_{B^+}$		—	2.0	6.0	—	2.8	—	nA
Average Drift of Noninverting Offset Current	$TCI_{OS^+}$	(Note 1)	—	15	50	—	20	—	$pA/^\circ C$
Input Offset Current	$I_{OS^-}$		—	2.0	6.0	—	2.8	—	nA
Common-Mode Rejection Ratio Match	$\Delta CMRR$	$V_{CM} = \pm 13V$	103	117	—	—	114	—	dB
Power Supply Rejection Ratio Match	$\Delta PSRR$	$V_S = \pm 3V$ to $\pm 18V$	—	6	32	—	8	—	$\mu V/V$

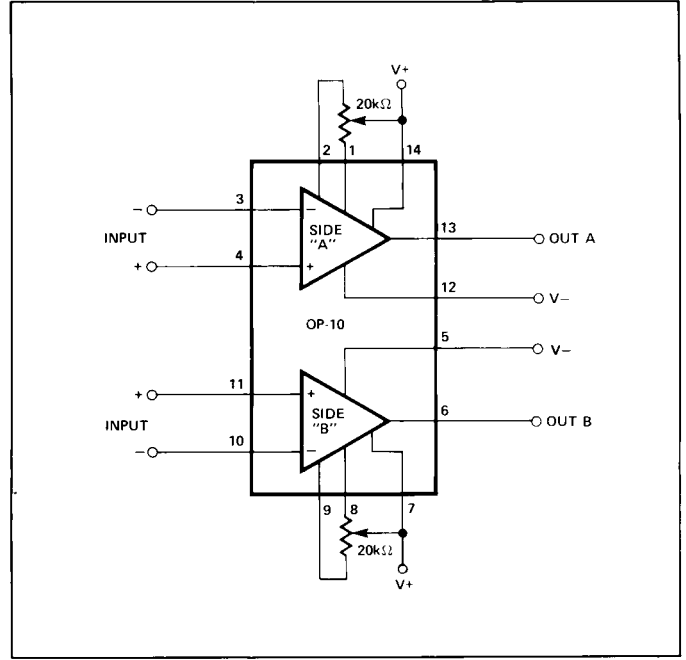
**NOTES:**

1. Sample tested.
2. Guaranteed by design.

**BURN-IN CIRCUIT**

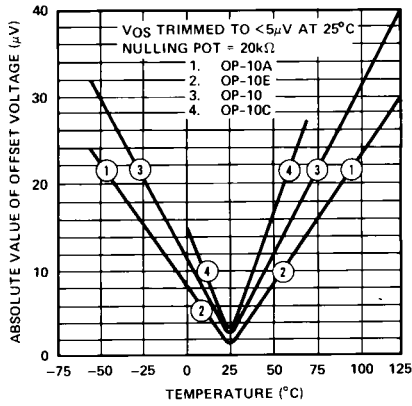


**OFFSET NULLING CIRCUIT**

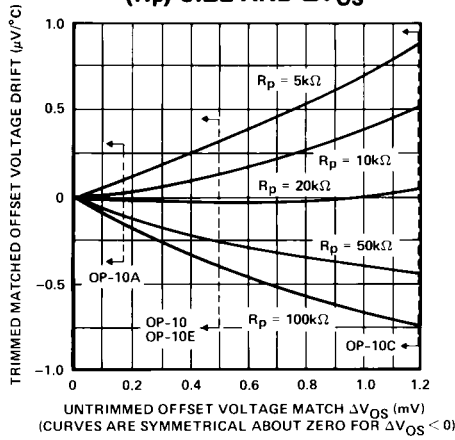


**TYPICAL PERFORMANCE CHARACTERISTICS**

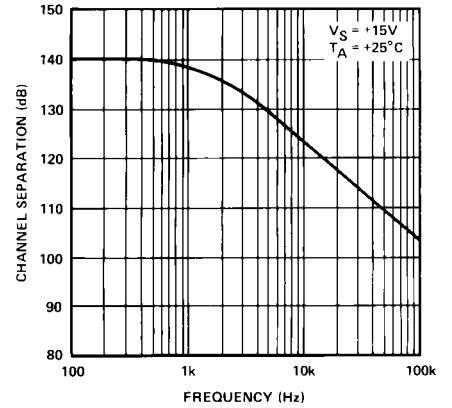
**MATCHING CHARACTERISTICS  
TRIMMED OFFSET VOLTAGE  
MATCH vs TEMPERATURE**



**MATCHING CHARACTERISTICS  
TRIMMED MATCHED OFFSET  
VOLTAGE DRIFT AS A  
FUNCTION OF TRIMMING POT  
( $R_p$ ) SIZE AND  $\Delta V_{OS}$**



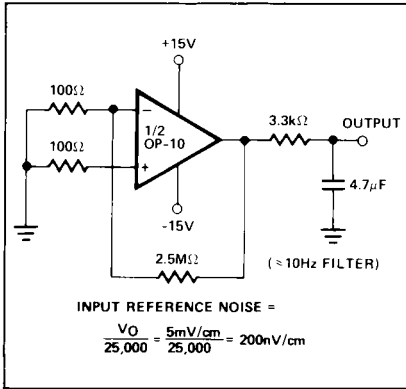
**MATCHING CHARACTERISTICS  
CHANNEL SEPARATION  
vs FREQUENCY**



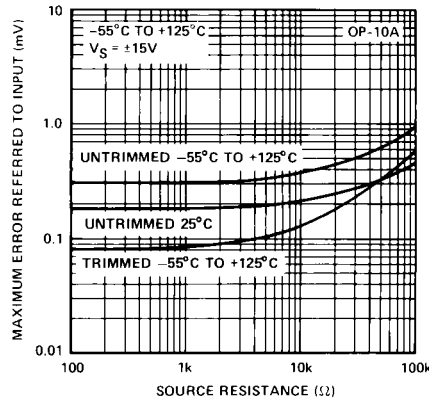
# OP-10

## TYPICAL PERFORMANCE CHARACTERISTICS

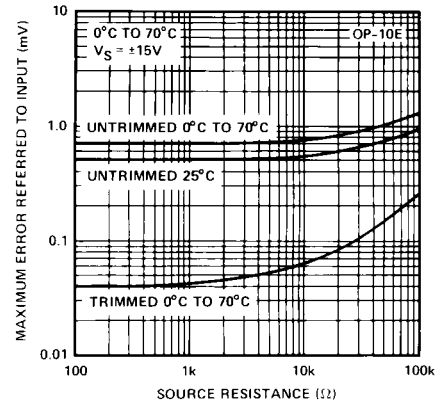
**TYPICAL LOW-FREQUENCY NOISE TEST CIRCUIT**



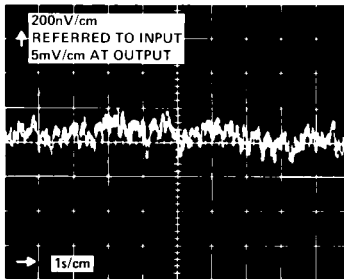
**MATCHING CHARACTERISTIC  
MAXIMUM INPUT ERROR vs  
SOURCE RESISTANCE**



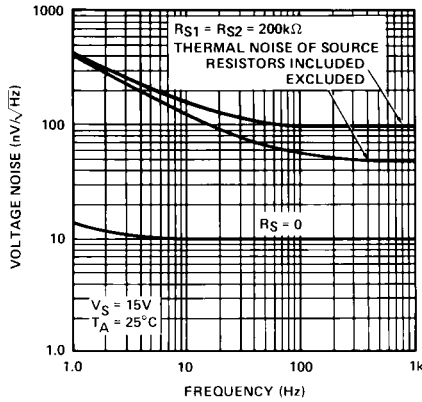
**MATCHING CHARACTERISTIC  
MAXIMUM INPUT ERROR vs  
SOURCE RESISTANCE**



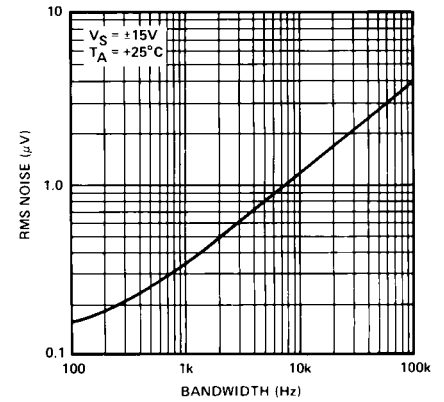
**OP-10 LOW FREQUENCY NOISE**



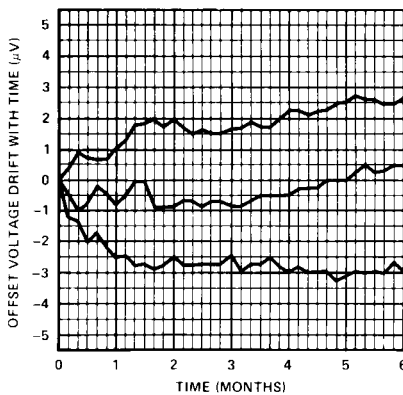
**VOLTAGE NOISE DENSITY  
vs FREQUENCY**



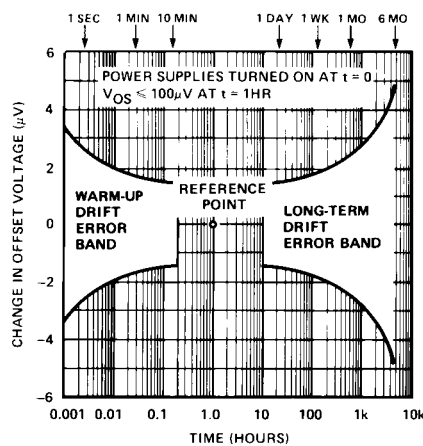
**INPUT WIDEBAND NOISE  
vs BANDWIDTH  
(0.1Hz TO FREQUENCY  
INDICATED)**



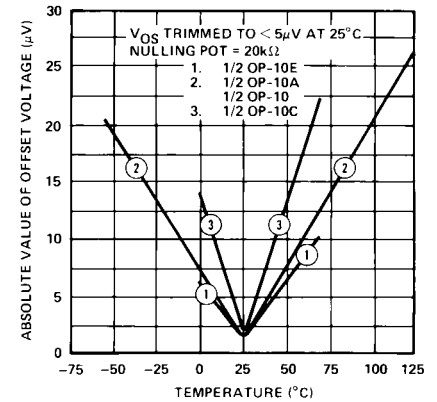
**TYPICAL OFFSET VOLTAGE  
STABILITY vs TIME**



**OFFSET VOLTAGE DRIFT  
WITH TIME**



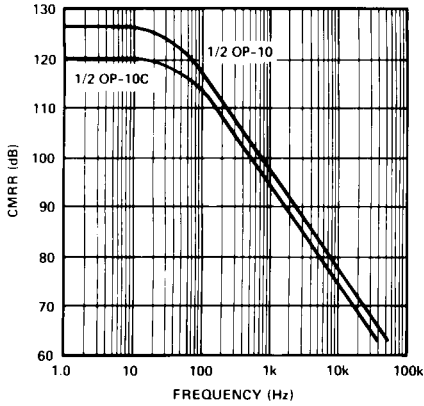
**TRIMMED OFFSET VOLTAGE  
vs TEMPERATURE**



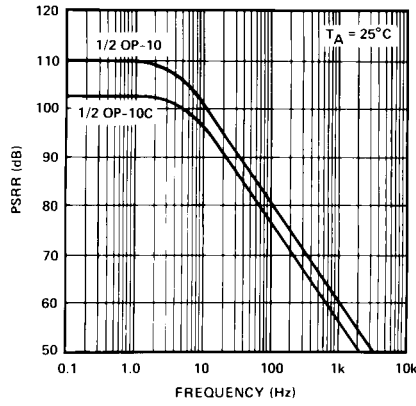


TYPICAL PERFORMANCE CHARACTERISTICS

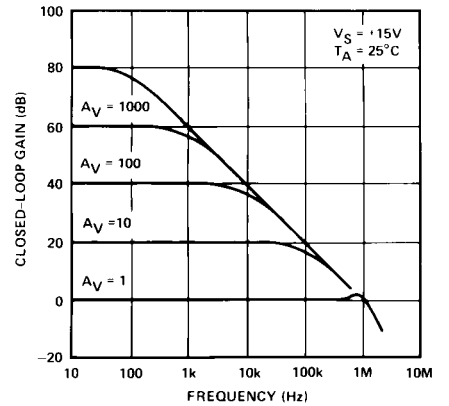
CMRR vs FREQUENCY



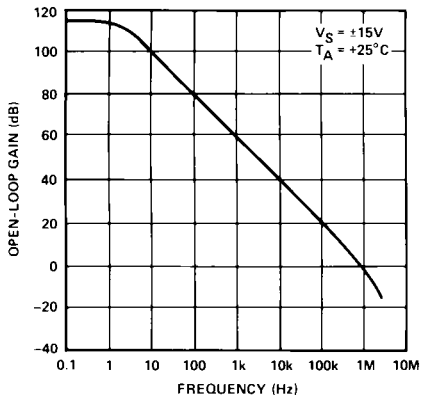
PSRR vs FREQUENCY



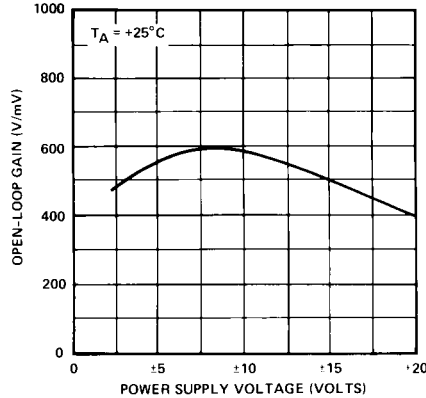
CLOSED-LOOP GAIN vs FREQUENCY



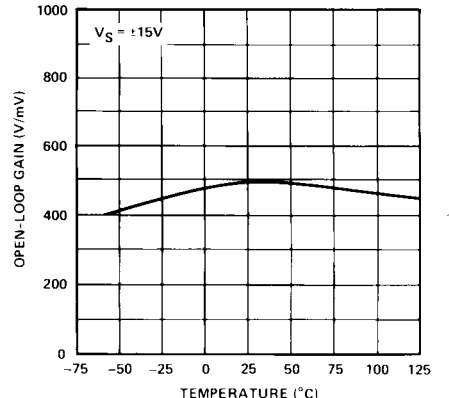
OPEN-LOOP GAIN vs FREQUENCY



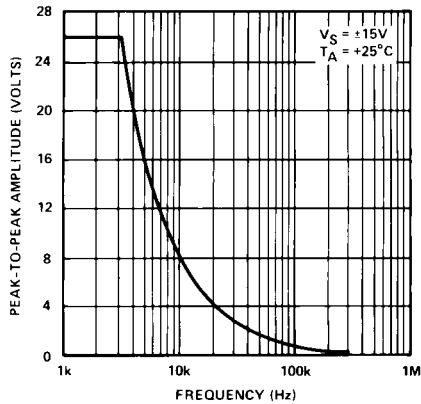
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



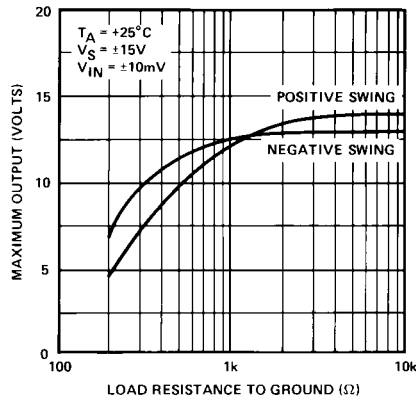
OPEN-LOOP GAIN vs TEMPERATURE



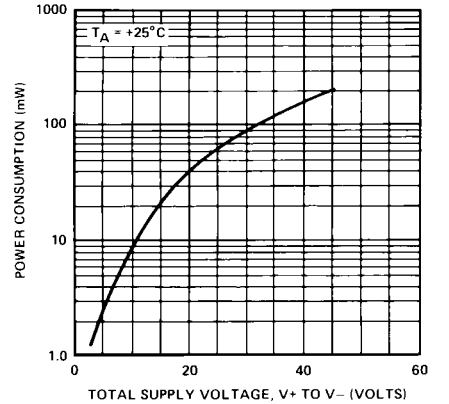
MAXIMUM OUTPUT SWING vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



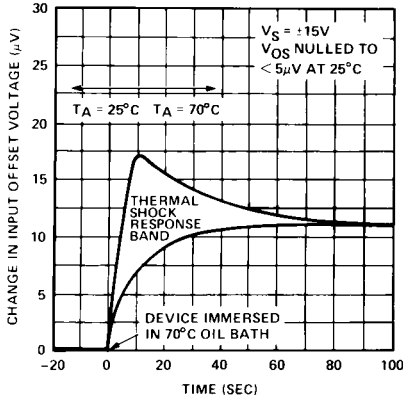
POWER CONSUMPTION vs POWER SUPPLY



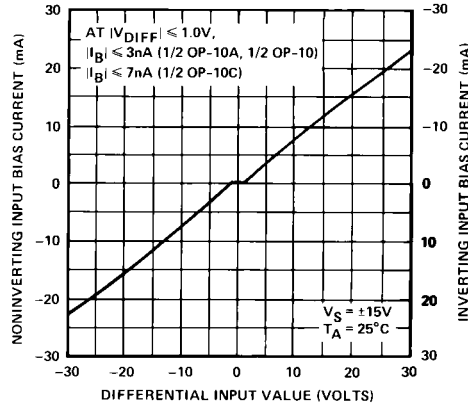
# OP-10

## TYPICAL PERFORMANCE CHARACTERISTICS

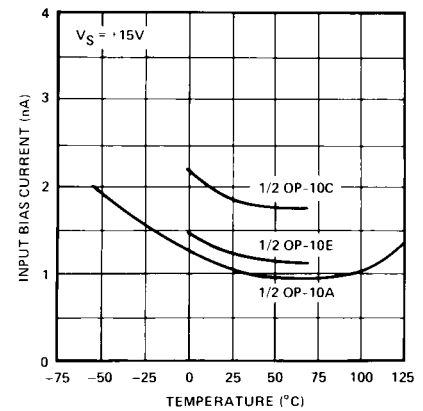
**OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK**



**INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE**



**INPUT BIAS CURRENT vs TEMPERATURE**



## APPLICATIONS INFORMATION

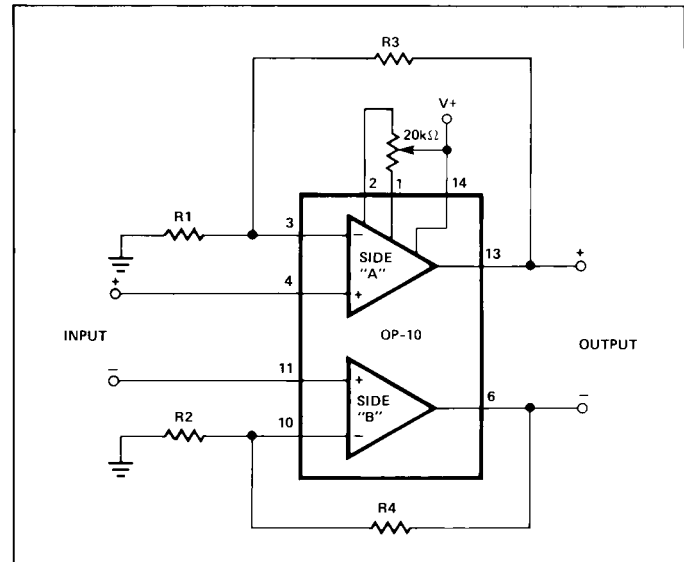
### ADVANTAGES OF DUAL MATCHED OPERATIONAL AMPLIFIERS

Dual matched operational amplifiers provide a powerful tool for the solution of some difficult circuit design problems. Circuits include true instrumentation amplifiers, extremely low drift, high common-mode rejection DC amplifiers, low DC drift active filters, dual tracking voltage references and many other demanding applications. These designs all require good matching between two operational amplifiers.

The adjacent circuit, a differential-in, differential-out amplifier, shows how errors can be reduced. Assuming the resistors used are matched, the gain of each side will be identical; if the offset voltage of each amplifier is matched, then the net differential voltage at the amplifiers output will be zero. Note that the output offset error of this amplifier is not a function of the offset voltage of the individual amplifiers, but only a function of the **difference** between the amplifiers' offset voltages. This error-cancellation principle holds for a number of input-referred error parameters — offset voltage, offset voltage drift, inverting and noninverting bias currents, common-mode and power supply rejection ratios. Note also that the impedances of each input, both common-mode and differential-mode, are extremely high, an important feature not possible with single operational amplifier circuits. Common-mode rejection can be made very high; this is especially important in instrumentation amplifiers where errors due to large common-mode voltages can be far greater than errors due to noise or drift with temperature.

For example, consider the case of two op amps, each with 80dB ( $100\mu\text{V/V}$ ) CMRR. If the CMRR of one device is  $+100\mu\text{V/V}$  while CMRR of the other is  $-100\mu\text{V/V}$ , then the net

CMRR will be  $200\mu\text{V/V}$ , a 6dB degradation. The matching of CMRR increases the effective CMRR when used as an instrumentation input stage.



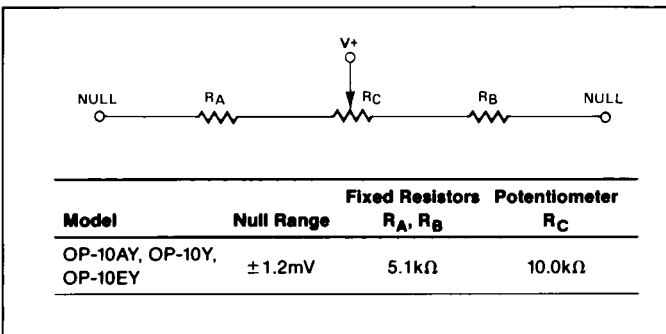
### POWER SUPPLIES

The  $V+$  supply terminals are completely independent and may be powered by separate supplies if desired (this approach, however, would sacrifice the advantages of the power supply rejection ratio matching). The  $V-$  supply terminals are both connected to the common substrate and must be tied to the same voltage.

**OFFSET TRIMMING**

Offset trimming terminals are provided for each amplifier of the OP-10. Guaranteed performance over temperature is obtained by trimming only one side (side A) to match the offset of the other; a net differential offset of zero results. This procedure is used during factory testing of the devices; however, essentially the same results may be obtained by trimming side B to match side A, or by nulling each side individually.

The OP-10 provides lowest drift when trimmed with a 20kΩ potentiometer; this value provides about ±4mV of adjustment range which should be more than adequate for most applications. Where finer trimming resolution is desired, or where unwanted changes in potentiometer position with time and temperature could create unacceptable offsets, the adjustment sensitivity may be reduced by using the circuit shown below.



**INSTRUMENTATION AMPLIFIERS USING OP-10**

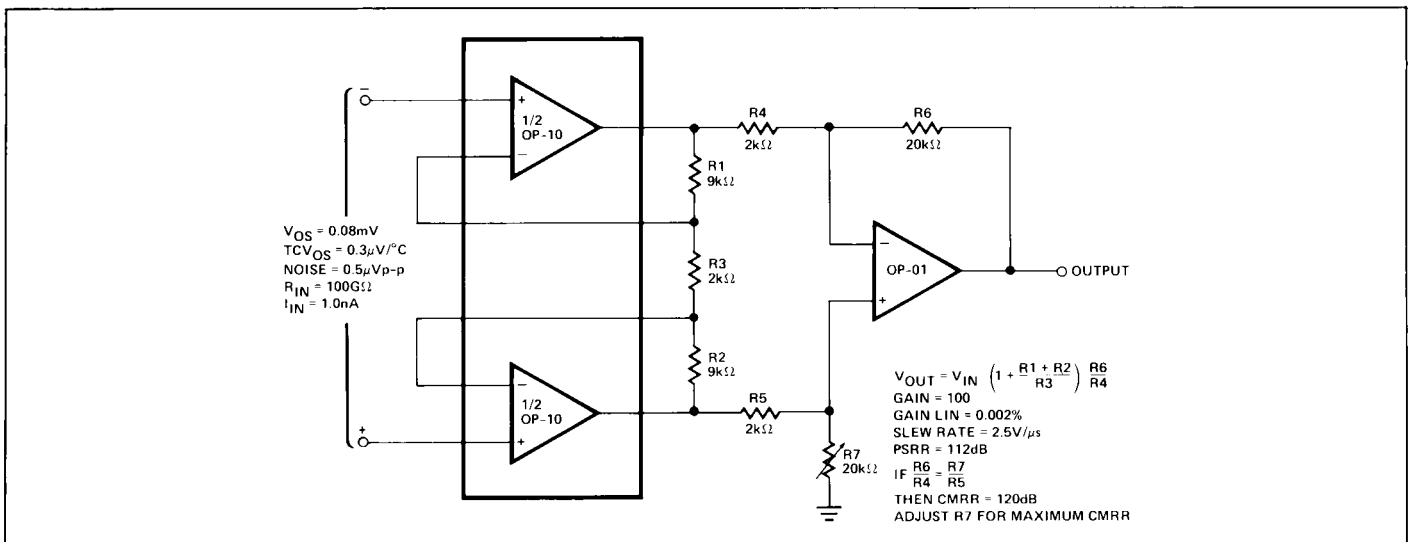
Instrumentation amplifiers with excellent performance can be easily built using the OP-10. Typical performance for a two and three-amplifier design are given in the table. The three-amplifier design, while more complex, has the advantages of simple gain adjustment by trimming a single resistor (R3) and

wide common-mode voltage capability at any gain, plus improved gain linearity. Slew rate, small-signal bandwidth, and full power bandwidth are also superior. Speed will be improved by using an OP-01 for the output stage.

**TYPICAL PERFORMANCE OF INSTRUMENTATION AMPLIFIERS  
GAIN = 100**

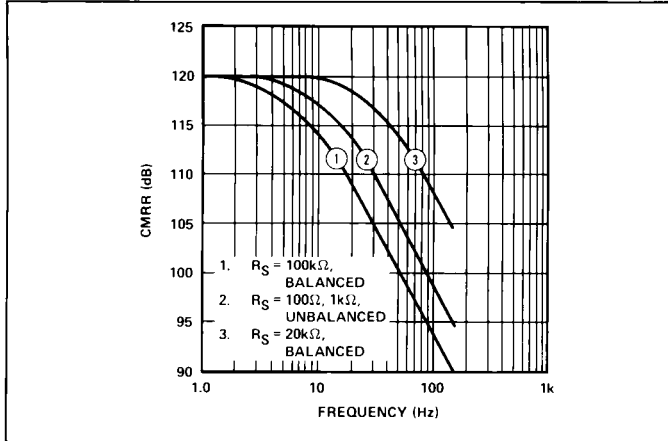
PARAMETER	2 OP AMP DESIGN	3 OP AMP DESIGN
Gain Nonlinearity	0.004%	0.001% (OP-05) 0.002% (OP-01)
Initial Input Offset Voltage	70μV	75μV
vs. Temperature (amplifier A nulled with 20k pot)	0.3μV/°C	0.3μV/°C
vs. Time	3.5μV/month	3.5μV/month
Input Bias Current	±1nA	±1nA
vs. Temperature	10pA/°C	10pA/°C
Input Offset Current	0.8nA	0.8nA
vs. Temperature	12pA/°C	12pA/°C
Input Impedance		
Differential	80GΩ	100GΩ
Common-Mode	100GΩ	100GΩ
Input Noise Voltage (0.1 to 10Hz)	0.5μVp-p	0.5μVp-p
Input Noise Current (0.1 to 10Hz)	14pAp-p	14pAp-p
Common-Mode Rejection	120dB	120dB
Power Supply Rejection	112dB	112dB
Frequency Response		
Small-Signal (-3dB)	6.0Hz	26kHz (OP-05) 85kHz (OP-01)
Full Power	2.5Hz	4.3kHz (OP-05) 43kHz (OP-01)
Slew Rate	0.17V/μs	0.17V/μs (OP-05) 4.0V/μs (OP-01)

**TRIPLE OP-AMP INSTRUMENTATION AMPLIFIER**

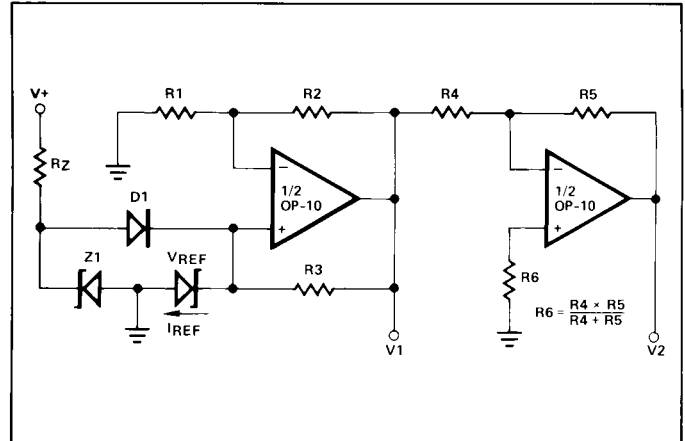


# OP-10

## CMRR vs FREQUENCY INSTRUMENTATION AMPLIFIER (3 OP-AMP DESIGN)



## PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10



## PRECISION DUAL TRACKING VOLTAGE REFERENCES USING OP-10

Precision dual tracking voltage references using a single reference source are easily constructed using OP-10. These references exhibit low noise, excellent stability vs. temperature and time, and have excellent power supply rejection.

In the circuit shown,  $R_3$  should be adjusted to set  $I_{REF}$  to operate  $V_{REF}$  at its minimum temperature coefficient current. Proper circuit start-up is assured by  $R_Z$ ,  $Z_1$ , and  $D_1$ .

$$V_{Z1} \leq V_{REF} + 2V \quad V1 = V_{REF} \left(1 + \frac{R2}{R1}\right)$$

$$I_{REF} = (V1 - V_{REF})/R3 \quad V2 = V1 \left(\frac{-R5}{R4}\right)$$

Output Impedance ( $\Delta I_L: 1.0mA-5.0mA$ ) .....  $0.25 \times 10^{-3}\Omega$

## INSTRUMENTATION AMPLIFIER (2 OP-AMP DESIGN)

