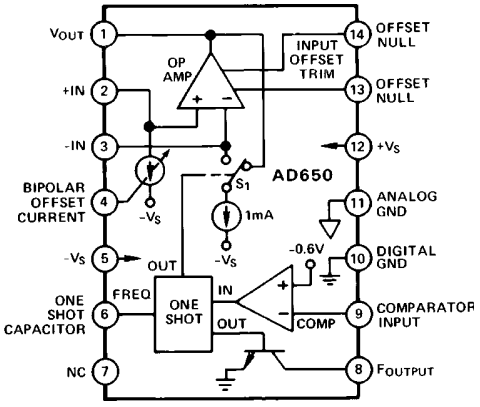
Voltage-to-Frequency and Frequency-to-Voltage Converter

AD650

FEATURES
V/F Conversion to 1 MHz
Reliable Monolithic Construction
Very Low Nonlinearity
0.002% typ at 10 kHz
0.005% typ at 100 kHz
0.07% typ at 1 MHz
Input Offset Trimmable to Zero
CMOS or TTL Compatible
Unipolar, Bipolar, or Differential V/F
V/F or F/V Conversion
Available in Surface Mount
MIL-STD-883 Compliant Versions Available

PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD650 V/F/V (voltage-to-frequency or frequency-to-voltage converter) provides a combination of high frequency operation and low nonlinearity previously unavailable in monolithic form. The inherent monotonicity of the V/F transfer function makes the AD650 useful as a high-resolution analog-to-digital converter. A flexible input configuration allows a wide variety of input voltage and current formats to be used, and an open-collector output with separate digital ground allows simple interfacing to either standard logic families or opto-couplers.

The linearity error of the AD650 is typically 20 ppm (0.002% of full scale) and 50 ppm (0.005%) maximum at 10 kHz full scale. This corresponds to approximately 14-bit linearity in an analog-to-digital converter circuit. Higher full-scale frequencies or longer count intervals can be used for higher resolution conversions. The AD650 has a useful dynamic range of six decades allowing extremely high resolution measurements. Even at 1 MHz full scale, linearity is guaranteed less than 1000 ppm (0.1%) on the AD650KN, KP, BD and SD grades.

In addition to analog-to-digital conversion, the AD650 can be used in isolated analog signal transmission applications, phased locked-loop circuits, and precision stepper motor speed controllers. In the F/V mode, the AD650 can be used in precision tachometer and FM demodulator circuits.

The input signal range and full-scale output frequency are user-programmable with two external capacitors and one resistor. Input offset voltage can be trimmed to zero with an external potentiometer.

The AD650JN and AD650KN are offered in a plastic 14-pin DIP package. The AD650JP and AD650KP are available in a 20-pin plastic leaded chip carrier (PLCC). Both plastic packaged versions of the AD650 are specified for the commercial (0°C to +70°C) temperature range. For industrial temperature range (–25°C to +85°C) applications, the AD650AD and AD650BD are offered in a ceramic package. The AD650SD is specified for the full –55°C to +125°C extended temperature range.

PRODUCT HIGHLIGHTS

1. In addition to very high linearity, the AD650 can operate at full-scale output frequency up to 1 MHz. The combination of these two features makes the AD650 an inexpensive solution for applications requiring high resolution monotonic A/D conversion.
2. The AD650 has a very versatile architecture that can be configured to accommodate bipolar, unipolar, or differential input voltages, or unipolar input currents.
3. TTL or CMOS compatibility is achieved using an open collector frequency output. The pull-up resistor can be connected to voltages up to +30 V, or +15 V or +5 V for conventional CMOS or TTL logic levels.
4. The same components used for V/F conversion can also be used for F/V conversion by adding a simple logic biasing network and reconfiguring the AD650.
5. The AD650 provides separate analog and digital grounds. This feature allows prevention of ground loops in real-world applications.
6. The AD650 is available in versions compliant with MIL-STD-883. Refer to the Analog Devices Military Products Databook or current AD650/883B data sheet for detailed specifications.

REV. A

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AD650—SPECIFICATIONS (@ + 25°C, with V_S = ±15 V, unless otherwise noted)

Model	AD650J/AD650A Min	AD650J/AD650A Typ	AD650J/AD650A Max	AD650K/AD650B Min	AD650K/AD650B Typ	AD650K/AD650B Max	AD650S Min	AD650S Typ	AD650S Max	Units
DYNAMIC PERFORMANCE										
Full-Scale Frequency Range			1			1			1	MHz
Nonlinearity[1] f_{MAX} = 10 kHz		0.002	0.005		0.002	0.005		0.002	0.005	%
f_{MAX} = 100 kHz		0.005	**0.02**		0.005	**0.02**		0.005	**0.02**	%
f_{MAX} = 500 kHz		0.02	0.05		0.02	0.05		0.02	0.05	%
f_{MAX} = 1 MHz		0.1			0.05	**0.1**		0.05	**0.1**	%
Full-Scale Calibration Error[2], 100 kHz		±5			±5			±5		%
1 MHz		±10			±10			±10		%
vs. Supply[3]	–0.015		**+0.015**	–0.015		**+0.015**	–0.015		**+0.015**	% of FSR/V
vs. Temperaturc										
A, B, and S Grades										
at 10 kHz			±75			±75			**±75**	ppm/°C
at 100 kHz			±150			±150			**±150**	ppm/°C
J and K Grades										
at 10 kHz		±75			±75					ppm/°C
at 100 kHz		±150			±150					ppm/°C
BIPOLAR OFFSET CURRENT										
Activated by 1.24 kΩ Between Pins 4 and 5	0.45	0.5	0.55	0.45	0.5	0.55	0.45	0.5	0.55	mA
DYNAMIC RESPONSE										
Maximum Settling Time for Full Scale										
Step Input	1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			
Overload Recovery Time										
Step Input	1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			1 Pulse of New Frequency Plus 1 µs			
ANALOLG INPUT AMPLIFIER (V/F Conversion)										
Current Input Range (Figure 1)	0		+0.6	0		+0.6	0		+0.6	mA
Voltage Input Range (Figure 5)	–10		0	–10		0	–10		0	V
Differential Impedance	2 MΩ‖10 pF			2 MΩ‖10 pF			2 MΩ‖10 pF			
Common-Mode Impedance	1000 MΩ‖10 pF			1000 MΩ‖10 pF			1000 MΩ‖10 pF			
Input Bias Current										
Noninverting Input		40	**100**		40	**100**		40	**100**	nA
Inverting Input		±8	**±20**		±8	**±20**		±8	**±20**	nA
Input Offset Voltage										
(Trimmable to Zero)			**±4**			**±4**			**±4**	mV
vs. Temperature (T_{MIN} to T_{MAX})		±30				±30			±30	µV/°C
Safe Input Voltage		$\pm V_S$			$\pm V_S$			$\pm V_S$		C
COMPARATOR (F/V Conversion)										
Logic "0" Level	$-V_S$		–1	$-V_S$		–1	$-V_S$		+1	V
Logic "1" Level	0		$+V_S$	0		$+V_S$	0		$+V_S$	V
Pulse Width Range[4]	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	0.1		$(0.3 \times t_{OS})$	µs
Input Impedance		250			250			250		kΩ
OPEN COLLECTOR OUTPUT (V/F Conversion)										
Output Voltage in Logic "0"										
$I_{SINK} \leq 8$ mA, T_{MIN} to T_{MAX}			0.4			0.4			0.4	V
Output Leakage Current in Logic "1"			**100**			**100**			**100**	nA
Voltage Range[5]	0		+36	0		+36	0		+36	V
AMPLIFIER OUTPUT (F/V Conversion)										
Voltage Range (1500 Ω min Load Resistance)	0		+10	0		+10	0		+10	V
Source Current (750 Ω max Load Resistance)	10			10			10			mA
Capacitive Load (Without Oscillation)			100			100			100	pF
POWER SUPPLY										
Voltage, Rated Performance	±9		**±18**	±9		**±18**	±9		**±18**	V
Quiescent Current			**8**			**8**			**8**	mA
TEMPERATURE RANGE										
Rated Performance – N Package	0		+70	0		+70				°C
D Package	–25		+85	–25		+85	–55		+125	°C
Storage – N Package	–25		+85	–25		+85				°C
D Package	–65		+150	–65		+150	–65		+150	°C
PACKAGE OPTIONS[6]										
PLCC (P-20A)		AD650JP			AD650KP					
Plastic DIP (N-14)		AD650JN			AD650KN					
Ceramic DIP (D-14)		AD650AD			AD650BD			AD650SD		

NOTES

[1]Nonlinearity is defined as deviation from a straight line from zero to full scale, expressed as a fraction of full scale.

[2]Full-scale calibration error adjustable to zero.

[3]Measured at full-scale output frequency of 100 kHz.

[4]Refer to F/V conversion section of the text.

[5]Referred to digital ground.

[6]D = Ceramic DIP; N = Plastic DIP; P = Plastic Leaded Chip Carrier.

Specifications subject to change without notice.

Specifications shown in **boldface** are tested on all production units at final electrical test. Results from those test are used to calculate outgoing quality levels. All min and max specifications are guaranteed, although only those shown in **boldface** are tested on all production units.

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage . . . . . 36 V
Storage Temperature Ceramic . . . . . –55°C to +165°C
Plastic . . . . . –25°C to +125°C
Differential Input Voltage (Pins 2 and 3) . . . . . ±10 V
Maximum Input Voltage . . . . . $\pm V_S$
Open Collector Output Voltage Above Digital GND . . . . . 36 V
Current . . . . . 50 mA
Amplifier Short Circuit to Ground . . . . . Indefinite
Comparator Input Voltage (Pin 9) . . . . . $\pm V_S$

ORDERING GUIDE

Model[1]	Gain Tempco ppm/ °C 100 kHz	1 MHz Linearity	Specified Temperature Range °C	Package
AD650JN	150 typ	0.1% typ	0 to +70	Plastic DIP
AD650KN	150 typ	0.1% max	0 to +70	Plastic DIP
AD650JP	150 typ	0.1% typ	0 to +70	PLCC
AD650KP	150 typ	0.1% max	0 to +70	PLCC
AD650AD	150 max	0.1% typ	–25 to +85	Ceramic
AD650BD	150 max	0.1% max	–25 to +85	Ceramic
AD650SD	150 max	0.1% max	–55 to +125	Ceramic

NOTE
[1]For details on grade and package offerings screened in accordance with MIL-STD-883B, refer to the Analog Devices Military Products Databook or current AD650/883B data sheet.

CIRCUIT OPERATION

UNIPOLAR CONFIGURATION

The AD650 is a *charge balance* voltage-to-frequency converter. In the connection diagram shown in Figure 1, or the block diagram of Figure 2a, the input signal is converted into an equivalent current by the input resistance R_{IN}. This current is *exactly* balanced by an internal feedback current delivered in short, timed bursts from the switched 1 mA internal current source. These bursts of current may be thought of as precisely defined packets of charge. The required number of charge packets, each producing one pulse of the output transistor, depends upon the amplitude of the input signal. Since the number of charge packets delivered per unit time is dependent on the input signal amplitude, a linear voltage-to-frequency transformation will be accomplished. The frequency output is furnished via an open collector transistor.

A more rigorous analysis demonstrates how the charge balance voltage-to-frequency conversion takes place.

A block diagram of the device arranged as a V-to-F converter is shown in Figure 2a. The unit is comprised of an input integrator, a current source and steering switch, a comparator and a one-shot. When the output of the one-shot is low, the current steering switch S_1 diverts all the current to the output of the op amp; this is called the Integration Period. When the one-shot has been triggered and its output is high, the switch S_1 diverts all the current to the summing junction of the op amp; this is called the Reset Period. The two different states are shown in Figure 2 along with the various branch currents. It should be noted that the output current from the op amp is the same for either state, thus minimizing transients.

PIN CONFIGURATION

PIN NO.	"D" CERAMIC DIP	PACKAGE "N" PLASTIC DIP	"P" PLCC
1	V_{OUT}	V_{OUT}	NC
2	+IN	+IN	V_{OUT}
3	–IN	–IN	+IN
4	BIPOLAR OFFSET CURRENT	BIPOLAR OFFSET CURRENT	–IN
5	$-V_S$	$-V_S$	NC
6	ONE SHOT CAPACITOR	ONE SHOT CAPACITOR	BIPOLAR OFFSET CURRENT
7	NC	NC	NC
8	F_{OUTPUT}	F_{OUTPUT}	$-V_S$
9	COMPARATOR INPUT	COMPARATOR INPUT	ONE SHOT CAPACITOR
10	DIGITAL GND	DIGITAL GND	NC
11	ANALOG GND	ANALOG GND	NC
12	$+V_S$	$+V_S$	F_{OUTPUT}
13	OFFSET NULL	OFFSET NULL	COMPARATOR INPUT
14	OFFSET NULL	OFFSET NULL	DIGITAL GND
15			NC
16			ANALOG GND
17			NC
18			$+V_S$
19			OFFSET NULL
20			OFFSET NULL

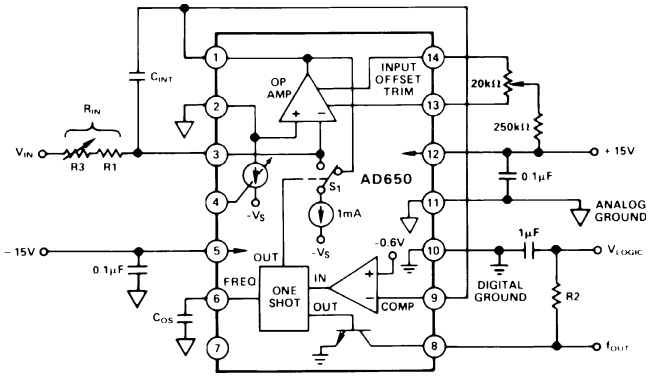


Figure 1. Connection Diagram for V/F Conversion, Positive Input Voltage

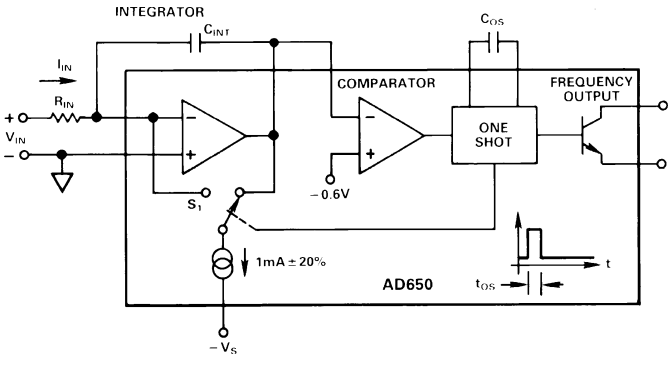


Figure 2a. Block Diagram

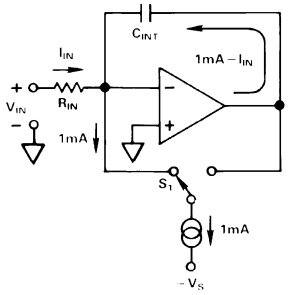


Figure 2b. Reset Mode

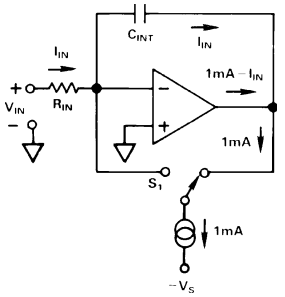


Figure 2c. Integrate Mode

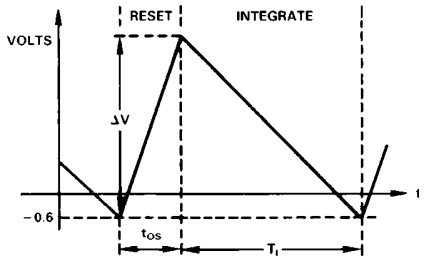


Figure 2d. Voltage Across C_{INT}

The positive input voltage develops a current ($I_{IN} = V_{IN}/R_{IN}$) which charges the integrator capacitor C_{INT}. As charge builds up on C_{INT}, the output voltage of the integrator ramps downward towards ground. When the integrator output voltage (Pin 1) crosses the comparator threshold (–0.6 volt) the comparator triggers the one shot, whose time period, t_{OS} is determined by the one shot capacitor C_{OS}.

Specifically, the one shot time period is:

$$t_{OS} = C_{OS} \times 6.8 \times 10^3 \text{ sec}/F + 3.0 \times 10^{-7} \text{ sec} \quad (1)$$

The Reset Period is initiated as soon as the integrator output voltage crosses the comparator threshold, and the integrator ramps upward by an amount:

$$\Delta V = t_{OS} \bullet \frac{dV}{dt} = \frac{t_{OS}}{C_{INT}}\left(1\,mA - I_N\right) \quad (2)$$

After the Reset Period has ended, the device starts another Integration Period, as shown in Figure 2, and starts ramping downward again. The amount of time required to reach the comparator threshold is given as:

$$T_I = \frac{\Delta V}{\frac{dV}{dt}} = \frac{t_{OS}/C_{INT}(1\,mA - I_{IN})}{I_N/C_{INT}} = t_{OS}\left(\frac{1\,mA}{I_{IN}} - 1\right) \quad (3)$$

The output frequency is now given as:

$$f_{OUT} = \frac{1}{t_{OS} + T_I} = \frac{I_{IN}}{t_{OS} \times 1\,mA} = 0.15\,\frac{F \bullet Hz}{A}\,\frac{V_{IN}/R_{IN}}{C_{OS} + 4.4 \times 10^{-11} F} \quad (4)$$

Note that C_{INT}, the integration capacitor has no effect on the transfer relation, but merely determines the amplitude of the sawtooth signal out of the integrator.

One Shot Timing

A key part of the preceding analysis is the one shot time period that was given in equation (1). This time period can be broken down into approximately 300 ns of propagation delay, and a second time segment dependent linearly on timing capacitor C_{OS}. When the one shot is triggered, a voltage switch that holds Pin 6 at analog ground is opened allowing that voltage to change. An internal 0.5 mA current source connected to Pin 6 then draws its current out of C_{OS}, causing the voltage at Pin 6 to decrease linearly. At approximately –3.4 V, the one shot resets itself, thereby ending the timed period and starting the V/F conversion cycle over again. The total one shot time period can be written mathematically as:

$$t_{OS} = \frac{\Delta V\, C_{OS}}{I_{DISCHARGE}} + T_{GATE\ DELAY} \quad (5)$$

substituting actual values quoted above,

$$t_{OS} = \frac{-3.4\,V \times C_{OS}}{-0.5 \times 10^{-3} A} + 300 \times 10^{-9} \text{ sec} \quad (6)$$

This simplifies into the timed period equation given above.

COMPONENT SELECTION

Only four component values must be selected by the user. These are input resistance R_{IN}, timing capacitor C_{OS}, logic resistor R2, and integration capacitor C_{INT}. The first two determine the input voltage and full-scale frequency, while the last two are determined by other circuit considerations.

Of the four components to be selected, R2 is the easiest to define. As a pull-up resistor, it should be chosen to limit the current through the output transistor to 8 mA if a TTL maximum V_{OL} of 0.4 V is desired. For example, if a 5 V logic supply is used, R2 should be no smaller than 5 V/8 mA or 625 Ω. A larger value can be used if desired.

R_{IN} and C_{OS} are the only two parameters available to set the full-scale frequency to accommodate the given signal range. The "swing" variable that is affected by the choice of R_{IN} and C_{OS} is nonlinearity. The selection guide of Figure 3 shows this quite graphically. In general, larger values of C_{OS} and lower full-scale input currents (higher values of R_{IN}) provide better linearity. In Figure 3, the implications of four different choices of R_{IN} are shown. Although the selection guide is set up for a unipolar configuration with a zero to 10 V input signal range, the results can be extended to other configurations and input signal ranges. For a full scale frequency of 100 kHz (corresponding to 10 V input), you can see that among the available choices, R_{IN} = 20 k and C_{OS} = 620 pF gives the lowest nonlinearity, 0.0038%. Also, if you wish to use the highest frequency that will give the 20 ppm minimum nonlinearity, it is approximately 33 kHz (40.2 kΩ and 1000 pF).

For input signal spans other than 10 V, the input resistance must be scaled proportionately. For example, if 100 kΩ is called out for a 0 V–10 V span, 10k would be used with a 0 V–1 V span, or 200 kΩ with a ±10 V bipolar connection.

The last component to be selected is the integration capacitor C_{INT}. In almost all cases, the best value for C_{INT} can be calculated using the equation:

$$C_{INT} = \frac{10^{-4} F/\text{sec}}{f_{MAX}}\,(1000\ pF\ minimum) \quad (7)$$

When the proper value for C_{INT} is used, the charge balance architecture of the AD650 provides continuous integration of the input signal, hence large amounts of noise and interference

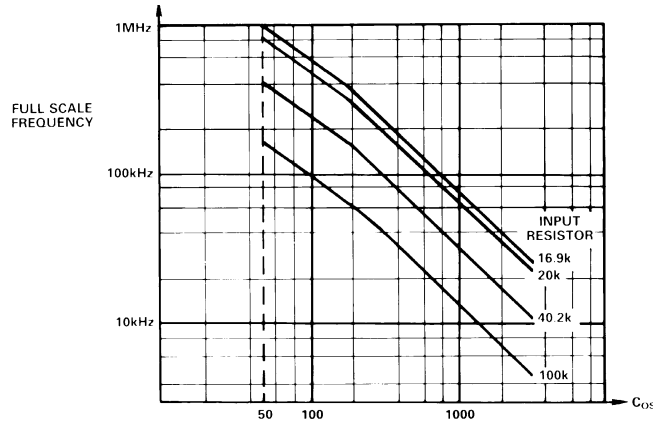


Figure 3a. Full-Scale Frequency vs. C_{OS}

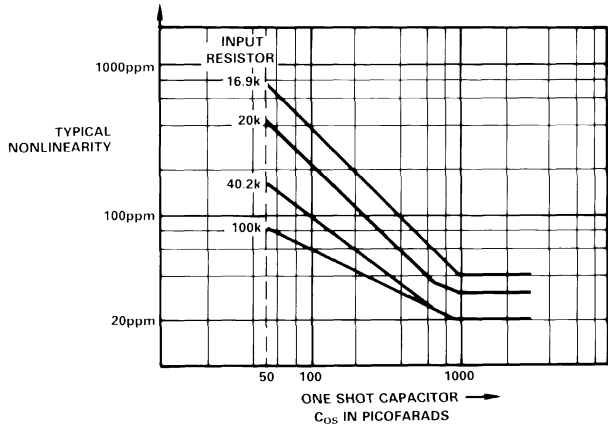


Figure 3b. Typical Nonlinearity vs. C_{OS}

can be rejected. If the output frequency is measured by counting pulses during a constant gate period, the integration provides infinite normal-mode rejection for frequencies corresponding to the gate period and its harmonics. However, if the integrator stage becomes saturated by an excessively large noise pulse, the continuous integration of the signal will be interrupted, allowing the noise to appear at the output. If the approximate amount of noise that will appear on C_{INT} is known (V_{NOISE}), the value of C_{INT} can be checked using the following inequality:

$$C_{INT} > \frac{t_{OS} \times 1 \times 10^{-3} A}{+V_S - 3V - V_{NOISE}} \quad (8)$$

For example, consider an application calling for a maximum frequency of 75 kHz, a 0 volt–1 volt signal range, and supply voltages of only ±9 volts. The component selection guide of Figure 3 is used to select 2.0 kΩ for R_{IN} and 1000 pF for C_{OS}. This results in a one shot time period of approximately 7 µs. Substituting 75 kHz into equation 7 yields a value of 1300 pF for C_{INT}. When the input signal is near zero, 1 mA flows through the integration capacitor to the switched current sink during the reset phase, causing the voltage across C_{INT} to increase by approximately 5.5 volts. Since the integrator output stage requires approximately 3 volts head room for proper operation, only 0.5 volt margin remains for integrating extraneous noise on the signal line. A negative noise pulse at this time might saturate the integrator, causing an error in signal integration. Increasing C_{INT} to 1500 pF or 2000 pF will provide much more noise margin, thereby eliminating this potential trouble spot.

BIPOLAR V/F

Figure 4 shows how the internal bipolar current sink is used to provide a half-scale offset for a ±5 V signal range, while providing a 100 kHz maximum output frequency. The nominally 0.5 mA (±10%) offset current sink is enabled when a 1.24 kΩ resistor is connected between Pins 4 and 5. Thus, with the grounded 10 kΩ nominal resistance shown, a –5 V offset is developed at Pin 2. Since Pin 3 must also be at –5 V, the current through R_{IN} is 10 V/40 kΩ = +0.25 mA at V_{IN} = +5 V, and 0 mA at V_{IN} = –5 V.

Components are selected using the same guidelines outlined for the unipolar configuration with one alteration. The voltage across the total signal range must be equated to the maximum

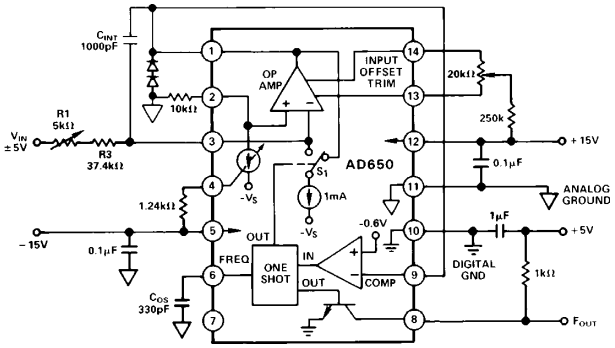


Figure 4. Connections for ±5 V Bipolar V/F with 0 to 100 kHz TTL Output

input voltage in the unipolar configuration. In other words, the value of the input resistor R_{IN} is determined by the input voltage span, not the maximum input voltage. A diode from Pin 1 to ground is also recommended. This is discussed further under "Other Circuit Conditions".

As in the unipolar circuit, R_{IN} and C_{OS} must have low temperature coefficients to minimize the overall gain drift. The 1.24 kΩ resistor used to activate the 0.5 mA offset current should also have a low temperature coefficient. The bipolar offset current has a temperature coefficient of approximately –200 ppm/°C.

UNIPOLAR V/F, NEGATIVE INPUT VOLTAGE

Figure 5 shows the connection diagram for V/F conversion of negative input voltages. In this configuration full-scale output frequency occurs at negative full-scale input, and zero output frequency corresponds with zero input voltage.

A very high impedance signal source may be used since it only drives the noninverting integrator input. Typical input impedance at this terminal is 1 GΩ or higher. For V/F conversion of positive input signals using the connection diagram of Figure 1, the signal generator must be able to source the integration current to drive the AD650. For the negative V/F conversion circuit of Figure 5, the integration current is drawn from ground through R1 and R3, and the active input is high impedance.

Circuit operation for negative input voltages is very similar to positive input unipolar conversion described in a previous section. For best operating results use component equations listed in that section.

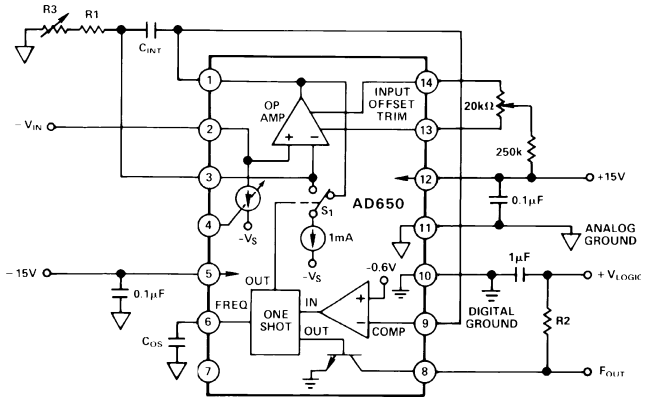


Figure 5. Connection Diagram for V/F Conversion, Negative Input Voltage

F/V CONVERSION

The AD650 also makes a very linear frequency-to-voltage converter. Figure 6 shows the connection diagram for F/V conversion with TTL input logic levels. Each time the input signal crosses the comparator threshold going negative, the one shot is activated and switches 1 mA into the integrator input for a measured time period (determined by C_{OS}). As the frequency increases, the amount of charge injected into the integration capacitor increase proportionately. The voltage across the integration capacitor is stabilized when the leakage current through R1 and R3 equals the average current being switched into the integrator. The net result of these two effects is an average output voltage which is proportional to the input frequency. Optimum performance can be obtained by selecting components using the same guidelines and equations listed in the V/F Conversion section.

The circuit of Figure 6 can be biased to accommodate almost any input signal waveform. With a TTL input, the 1000 pF coupling capacitor and 2.2 kΩ resistor creates a clean negative spike that triggers the one shot on negative going edges. For input signals with slower edges, a larger capacitor and/or resistor may be used as long as the comparator is never exposed to a voltage lower than –0.6 V for longer than the one shot time period. If this happens, the one shot will trigger itself more than once per cycle, creating discontinuities in the F/V transfer function. An input pulse greater than 100 ns but less than $0.3 \times t_{OS}$ is recommended (t_{OS} is defined by equation 1 in the circuit operation section, unipolar configuration).

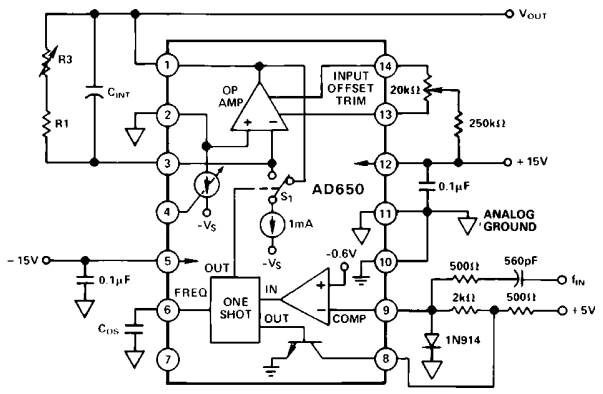


Figure 6. Connection Diagram for F/V Conversion

HIGH FREQUENCY OPERATION

Proper RF techniques must be observed when operating the AD650 at or near its maximum frequency of 1 MHz. Lead lengths must be kept as short as possible, especially on the one shot and integration capacitors, and at the integrator summing junction. In addition, at maximum output frequencies above 500 kHz, a 3.6 kΩ pull-down resistor from Pin 1 to $-V_S$ is required (see Figure 7). The additional current drawn through the pull-down resistor reduces the op amp's output impedance and improves its transient response.

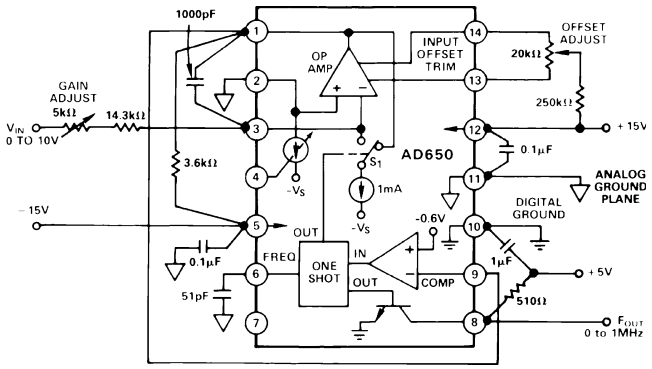


Figure 7. 1 MHz V/F Connection Diagram

DECOUPLING AND GROUNDING

It is good engineering practice to use bypass capacitors on the supply-voltage pins and to insert small-valued resistors (10 Ω to 100 Ω) in the supply lines to provide a measure of decoupling between the various circuits in a system. Ceramic capacitors of 0.1 μF to 1.0 μF should be applied between the supply-voltage pins and analog signal ground for proper bypassing on the AD650.

In addition, a larger board level decoupling capacitor of 1 μF to 10 μF should be located relatively close to the AD650 on each power supply line. Such precautions are imperative in high resolution data acquisition applications where one expects to exploit the full linearity and dynamic range of the AD650. Although some types of circuits may operate satisfactorily with power supply decoupling at only one location on each circuit board, such practice is strongly discouraged in high accuracy analog design.

Separate digital and analog grounds are provided on the AD650. The emitter of the open collector frequency output transistor is the only node returned to the digital ground. All other signals are referred to analog ground. The purpose of the two separate grounds is to allow isolation between the high precision analog signals and the digital section of the circuitry. As much as several hundred millivolts of noise can be tolerated on the digital ground without affecting the accuracy of the VFC. Such ground noise is inevitable when switching the large currents associated with the frequency output signal.

At 1 MHz full scale, it is necessary to use a pull-up resistor of about 500 Ω in order to get the rise time fast enough to provide well defined output pulses. This means that from a 5 volt logic supply, for example, the open collector output will draw 10 mA.

This much current being switched will surely cause ringing on long ground runs due to the self inductance of the wires. For instance, #20 gauge wire has an inductance of about 20 nH per inch; a current of 10 mA being switched in 50 ns at the end of

12 inches of 20 gauge wire will produce a voltage spike of 50 mV. The separate digital ground of the AD650 will easily handle these types of switching transients.

A problem will remain from interference caused by radiation of electro-magnetic energy from these fast transients. Typically, a voltage spike is produced by inductive switching transients; these spikes can capacitively couple into other sections of the circuit. Another problem is ringing of ground lines and power supply lines due to the distributed capacitance and inductance of the wires. Such ringing can also couple interference into sensitive analog circuits. The best solution to these problems is proper bypassing of the logic supply at the AD650 package. A 1 μF to 10 μF tantalum capacitor should be connected directly to the supply side of the pull-up resistor and to the digital ground—Pin 10. The pull-up resistor should be connected directly to the frequency output—Pin 8. The lead lengths on the bypass capacitor and the pull up resistor should be as short as possible. The capacitor will supply (or absorb) the current transients, and large ac signals will flow in a physically small loop through the capacitor, pull up resistor, and frequency output transistor. It is important that the loop be physically small for two reasons: first, there is less self-inductance if the wires are short, and second, the loop will not radiate RFI efficiently.

The digital ground (Pin 10) should be separately connected to the power supply ground. Note that the leads to the digital power supply are only carrying dc current and cannot radiate RFI. There may also be a dc ground drop due to the difference in currents returned on the analog and digital grounds. This will not cause any problem. In fact, the AD650 will tolerate as much as 0.25 volt dc potential difference between the analog and digital grounds. These features greatly ease power distribution and ground management in large systems. Proper technique for grounding requires separate digital and analog ground returns to the power supply. Also, the signal ground must be referred directly to analog ground (Pin 11) at the package. All of the signal grounds should be tied directly to Pin 11, especially the one-shot capacitor. More information on proper grounding and reduction of interference can be found in Reference 1.

TEMPERATURE COEFFICIENTS

The drift specifications of the AD650 do not include temperature effects of any of the supporting resistors or capacitors. The drift of the input resistors R1 and R3 and the timing capacitor C_{OS} directly affect the overall temperature stability. In the application of Figure 2, a 10 ppm/°C input resistor used with a 100 ppm/°C capacitor may result in a maximum overall circuit gain drift of:

150 ppm/°C (AD650A) + 100 ppm/°C (C_{OS}) + 10 ppm/°C (R_{IN}) 260 ppm/°C

In bipolar configuration, the drift of the 1.24 kΩ resistor used to activate the internal bipolar offset current source will directly affect the value of this current. This resistor should be matched to the resistor connected to the op amp noninverting input (Pin 2), see Figure 4. That is, the temperature coefficients of these two resistors should be equal. If this is the case, then the effects of the temperature coefficients of the resistors cancel each other, and the drift of the offset voltage developed at the op amp noninverting input will be determined solely by the AD650. Under these conditions the TC of the bipolar offset voltage is typically –200 ppm/°C and is a maximum of –300 ppm/°C. The offset voltage always decreases in magnitude as temperature is increased.

Other circuit components do not directly influence the accuracy of the VFC over temperature changes as long as their actual values are not so different from the nominal value as to preclude operation. This includes the integration capacitor, C_{INT}. A change in the capacitance value of C_{INT} simply results in a different rate of voltage change across the capacitor. During the Integration Phase (refer to Figure 2), the rate of voltage change across C_{INT} has the opposite effect that it does during the Reset Phase. The result is that the conversion accuracy is unchanged by either drift or tolerance of C_{INT}. The net effect of a change in the integrator capacitor is simply to change the peak to peak amplitude of the sawtooth waveform at the output of the integrator.

The gain temperature coefficient of the AD650 is not a constant value. Rather the gain TC is a function of both the full-scale frequency and the ambient temperature. At a low full-scale frequency, the gain TC is determined primarily by the stability of the internal reference—a buried Zener reference. This low speed gain TC can be quite good; at 10 kHz full scale, the gain TC near 25°C is typically 0 ± 50 ppm/°C. Although the gain TC changes with ambient temperature (tending to be more positive at higher temperatures), the drift remains within a ±75 ppm/°C window over the entire military temperature range. At full-scale frequencies higher than 10 kHz dynamic errors become much more important than the static drift of the dc reference. At a full-scale frequency of 100 kHz and above, these timing errors dominate the gain TC. For example, at 100 kHz full-scale frequency (R_{IN} = 40 k and C_{OS} = 330 pF) the gain TC near room temperature is typically –80 ± 50 ppm/°C, but at an ambient temperature near +125°C, the gain TC tends to be more positive and is typically +15 ± 50 ppm/°C. This information is presented in a graphical form in Figure 8. The gain TC always tends to become more positive at higher temperatures. Therefore, it is possible to adjust the gain TC of the AD650 by using a one-shot capacitor with an appropriate TC to cancel the drift of the circuit. For example, consider the 100 kHz full-scale frequency. An average drift of –100 ppm/°C means that as temperature is increased, the circuit will produce a lower frequency in response to a given input voltage. This means that the one-shot capacitor must decrease in value as temperature increases in order to compensate the gain TC of the AD650; that is, the capacitor must have a TC of –100 ppm/°C. Now consider the 1 MHz full-scale frequency.

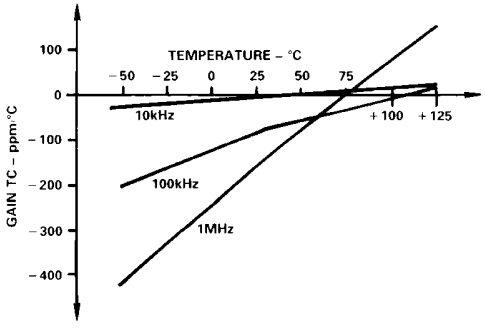


Figure 8. Gain TC vs. Temperature

[1]"Noise Reduction Techniques in Electronic Systems," by H. W. OTT, (John Wiley, 1976).

It is not possible to achieve very much improvement in performance unless the expected ambient temperature range is known. For example, in a constant low temperature application such as gathering data in an Arctic climate (approximately –20°C), a C_{OS} with a drift of –310 ppm/°C is called for in order to compensate the gain drift of the AD650. However, if that circuit should see an ambient temperature of +75°C, the C_{OS} cap would change the gain TC from approximately 0 ppm to +310 ppm/°C.

The temperature effects of the components described above are the same when the AD650 is configured for negative or bipolar input voltages, and for F/V conversion as well.

NONLINEARITY SPECIFICATION

The linearity error of the AD650 is specified by the endpoint method. That is, the error is expressed in terms of the deviation from the ideal voltage to frequency transfer relation after calibrating the converter at full scale and "zero". The nonlinearity will vary with the choice of one-shot capacitor and input resistor (see Figure 3). Verification of the linearity specification requires the availability of a switchable voltage source (or a DAC) having a linearity error below 20 ppm, and the use of very long measurement intervals to minimize count uncertainties. Every AD650 is automatically tested for linearity, and it will not usually be necessary to perform this verification, which is both tedious and time consuming. If it is required to perform a nonlinearity test either as part of an incoming quality screening or as a final product evaluation, an automated "bench-top" tester would prove useful. Such a system based on the Analog Devices' LTS-2010 is described in Reference 2.

The voltage-to-frequency transfer relation is shown in Figure 9 with the nonlinearity exaggerated for clarity. The first step in determining nonlinearity is to connect the endpoints of the operating range (typically at 10 mV and 10 V) with a straight line. This straight line is then the ideal relationship which is desired from the circuit. The second step is to find the difference between this line and the actual response of the circuit at a few points between the endpoints—typically ten intermediate points will suffice. The difference between the actual and the ideal response is a frequency error measured in hertz. Finally, these frequency errors are normalized to the full-scale frequency and expressed either as parts per million of full scale (ppm) or parts per hundred of full scale (%). For example, on a 100 kHz full scale, if the maximum frequency error is 5 Hz, the nonlinearity would be specified as 50 ppm or 0.005%. Typically on the 100 kHz scale, the nonlinearity is positive and the maximum value occurs at about midscale (Figure 9a). At higher full-scale frequencies, (500 kHz to 1 MHz), the nonlinearity becomes "S" shaped and the maximum value may be either positive or negative. Typically, on the 1 MHz scale (R_{IN} = 16.9k, C_{OS} = 51 pF) the nonlinearity is positive below about 2/3 scale and is negative above this point. This is shown graphically in Figure 9b.

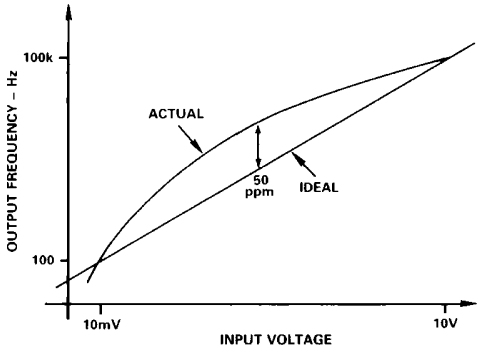


Figure 9a. Exaggerated Nonlinearity at 100 kHz Full Scale

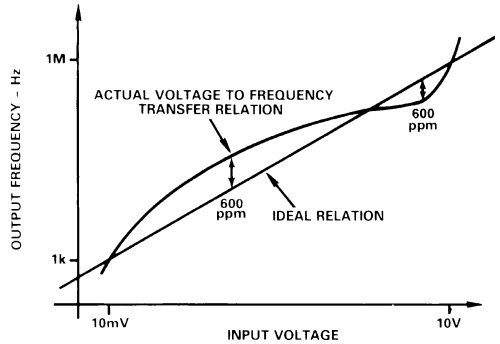


Figure 9b. Exaggerated Nonlinearity at 1 MHz Full Scale

[2]"V-F Converters Demand Accurate Linearity Testing," by L. DeVito, (Electronic Design, March 4, 1982).

PSRR

The power supply rejection ratio is a specification of the change in gain of the AD650 as the power supply voltage is changed. The PSRR is expressed in units of parts-per-million change of the gain per percent change of the power supply—ppm/%. For example, consider a VFC with a 10 volt input applied and an output frequency of exactly 100 kHz when the power supply potential is ±15 volts. Changing the power supply to ±12.5 volts is a 5 volt change out of 30 volts, or 16.7%. If the output frequency changes to 99.9 kHz, the gain has changed 0.1% or 1000 ppm. The PSRR is 1000 ppm divided by 16.7% which equals 60 ppm/%.

The PSRR of the AD650 is a function of the full-scale operating frequency. At low full-scale frequencies the PSRR is determined by the stability of the reference circuits in the device and can be very good. At higher frequencies there are dynamic errors which become more important than the static reference signals, and consequently the PSRR is not quite as good. The values of PSRR are typically 0 ± 20 ppm/% at 10 kHz full-scale frequency (R_{IN} = 40 k, C_{OS} = 3300 pF). At 100 kHz (R_{IN} = 40k, C_{OS} = 330 pF) the PSRR is typically +80 ± 40 ppm/%, and at 1 MHz (R_{IN} = 16.9 kΩ, C_{OS} = 51 pF) the PSRR is +350 ± 50 ppm/%. This information is summarized graphically in Figure 10.

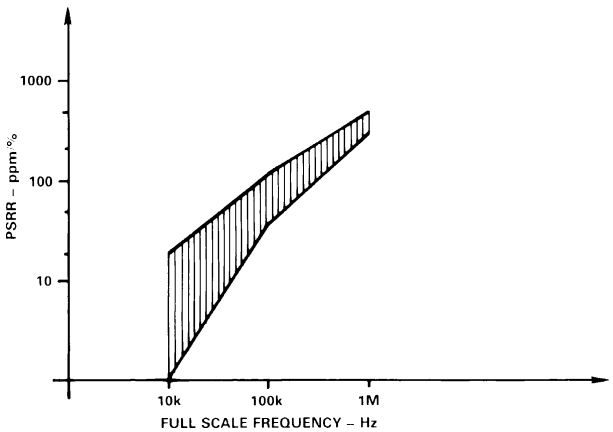


Figure 10. PSRR vs. Full-Scale Frequency

OTHER CIRCUIT CONSIDERATIONS

The input amplifier connected to Pins 1, 2 and 3 is not a standard operational amplifier. Rather, the design has been optimized for simplicity and high speed. The single largest difference between this amplifier and a normal op amp is the lack of an integrator (or level shift) stage. Consequently the voltage on the output (Pin 1) must always be more positive than 2 volts below the inputs (Pins 2 and 3). For example, in the F-to-V conversion mode, see Figure 6, the noninverting input of the op amp (Pin 2) is grounded, which means that the output (Pin 1) will not be able to go below –2 volts. Normal operation of the circuit as shown in the figure will never call for a negative voltage at the output but one may imagine an arrangement calling for a bipolar output voltage (say ±10 volts) by connecting an extra resistor from Pin 3 to a positive voltage. This will not work.

Care should be taken under conditions where a high positive input voltage exists at or before power up. These situations can cause a latch up at the integrator output (Pin 1). This is a nondestructive latch and, as such, normal operation can be restored by cycling the power supply. Latch up can be prevented by connecting two diodes (e.g., 1N914 or 1N4148) as shown in Figure 4, thereby, preventing Pin 1 from swinging below Pin 2.

A second major difference is that the output will only sink 1 mA to the negative supply. There is no pulldown stage at the output other than the 1 mA current source used for the V-to-F conversion. The op amp will source a great deal of current from the positive supply, and it is internally protected by current limiting. The output of the op amp may be driven to within 3 volts of the positive supply when it is not sourcing external current. When sourcing 10 mA the output voltage may be driven to within 6 volts of the positive supply.

A third difference between this op amp and a normal device is that the inverting input, Pin 3, is bias current compensated and the noninverting input is not bias current compensated. The bias current at the inverting input is nominally zero, but may be as much as 20 nA in either direction. The noninverting input typically has a bias current of 40 nA that always flows into the node (an npn input transistor). Therefore, it is not possible to match input voltage drops due to bias currents by matching input resistors.

The op amp has provisions for trimming the input offset voltage. A potentiometer of 20 kΩ is connected to Pins 13 and 14 and the wiper is connected to the positive supply through a 250 kΩ resistor. A potential of about 0.6 volt is established across the 250 kΩ resistor, and the 3 μA current is injected into the null pins. It is also possible to null the op amp offset voltage by using only one of the null pins and use a bipolar current either into or out of the null pin. The amount of current required will be very small—typically less than 3 μA. This technique is shown in the applications section of this data sheet: the auto-zero circuit uses this technique.

The bipolar offset current is activated by connecting a 1.24 kΩ resistor between Pin 4 and the negative supply. The resultant current delivered to the op amp noninverting input is nominally 0.5 mA and has a tolerance of ±10%. This current is then used to provide an offset voltage when Pin 2 is tied to ground through a resistor. The 0.5 mA which appears at Pin 2 is also flowing through the 1.24 kΩ resistor and this current may be by observing the voltage across the 1.24 kΩ resistor. An external resistor is used to activate the bipolar offset current source to provide the lowest tolerance and temperature drift of the resultant offset voltage. It is possible to use other values of resistance between Pin 4 and $-V_S$ to obtain a bipolar offset current different than 0.5 mA. Figure 11 is a graph of the relationship between the bipolar offset current and the value of the resistor used to activate the source.

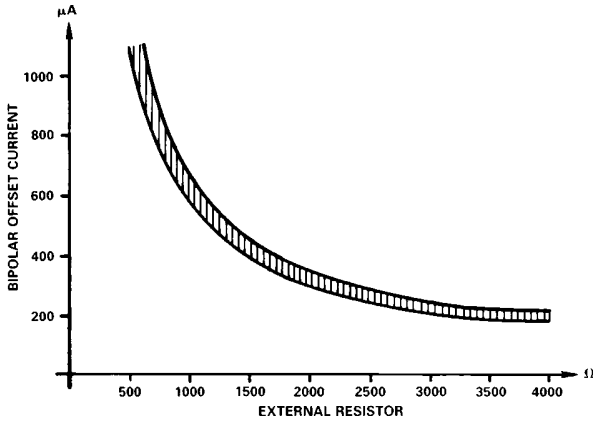


Figure 11. Bipolar Offset Current vs. External Resistor

APPLICATIONS

DIFFERENTIAL VOLTAGE-TO-FREQUENCY CONVERSION

The circuit of Figure 12 accepts a true floating differential input signal. The common-mode input, V_{CM}, may be in the range +15 to –5 volts with respect to analog ground. The signal input, V_{IN}, may be ±5 volts with respect to the common-mode input. Both inputs are low impedance: the source which drives the common-mode input must supply the 0.5 mA drawn by the bipolar offset current source and the source which drives the signal input must supply the integration current.

If less common-mode voltage range is required, a lower voltage Zener may be used. For example, if a 5 volt Zener is used, the V_{CM} input may be in the range +10 to –5 volt. If the Zener is not used at all, the common-mode range will be ±5 volts with respect to analog ground. If no Zener is used, the 10k pulldown resistor is not needed and the integrator output (Pin 1) is connected directly to the comparator input (Pin 9).

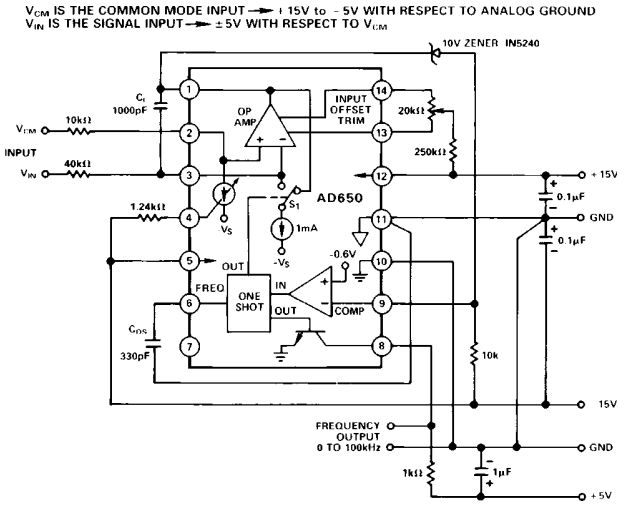


Figure 12. AD650 Differential Input

AUTO ZERO CIRCUIT

In order to exploit the full dynamic range of the AD650 VFC, very small input voltages will need to be converted. For example, a six decade dynamic range based on a full scale of 10 volts will require accurate measurement of signals down to 10 μV. In these situations a well-controlled input offset voltage is imperative. A constant offset voltage will not affect dynamic range but simply shift all of the frequency readings by a few hertz. However, if the offset should change, then it will not be possible to distinguish between a small change in a small input voltage and a drift of the offset voltage. Hence, the usable dynamic range is less. The circuit shown in Figure 13 provides automatic adjustment of the op amp offset voltage. The circuit uses an AD582 sample and hold amplifier to control the offset and the input voltage to the VFC is switched between ground and the signal to be measured via an AD7512DI analog switch. The offset of the AD650 is adjusted by injecting a current into or drawing a current out of Pin 13. Note that only one of the offset null pins is used. During the "VFC Norm" mode, the SHA is in the hold mode and the hold capacitor is very large, 0.1 μF, to hold the AD650 offset constant for a long period of time.

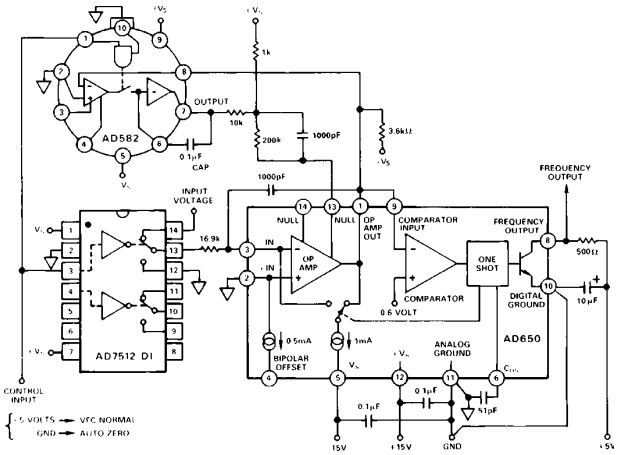


Figure 13. Auto-Zero Circuit for AD650 Voltage-to-Frequency Converter

When the circuit is in the "Auto Zero" mode the SHA is in sample mode and behaves like an op amp. The circuit is a variation of the classical two amplifier servo loop, where the output of the Device Under Test (DUT)—here the DUT is the AD650 op amp—is forced to ground by the feedback action of the control amplifier—the SHA. Since the input of the VFC circuit is connected to ground during the auto zero mode, the input current which can flow is determined by the offset voltage of the AD650 op amp. Since the output of the integrator stage is forced to ground it is known that the voltage is not changing (it is equal to ground potential). Hence if the output of the integrator is constant, its input current must be zero, so the offset voltage has been forced to be zero. Note that the output of the DUT could have been forced to any convenient voltage other than ground. All that is required is that the output voltage be known to be constant. Note also that the effect of the bias current at the inverting input of the AD650 op amp is also nulled in this circuit. The 1000 pF capacitor shunting the 200 kΩ resistor is compensation for the two amplifier servo loop. Two integrators in a loop requires a single zero for compensation. Note that the 3.6 kΩ resistor from Pin 1 of the AD650 to the negative supply *is not* part of the auto-zero circuit, but rather it is required for VFC operation at 1 MHz.

PHASE LOCKED LOOP F/V CONVERSION

Although the F/V conversion technique shown in Figure 6 is quite accurate and uses only a few extra components, it is very limited in terms of signal frequency response and carrier feedthrough. If the carrier (or input) frequency changes instantaneously, the output cannot change very rapidly due to the integrator time constant formed by C_{INT} and R_{IN}. While it is possible to decrease the integrator time constant to provide faster settling of the F-to-V output voltage, the carrier feedthrough will then be larger. For signal frequency response in excess of 2 kHz, a phase locked F/V conversion technique such as the one shown in Figure 14 is recommended.

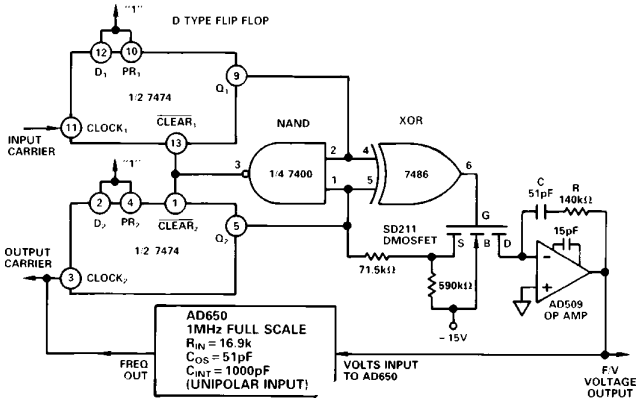


Figure 14. Phase Locked Loop F/V Conversion

In a phase locked loop circuit, the oscillator is driven to a frequency and phase equal to an input reference signal. In applications such as a synthesizer, the oscillator output frequency is first processed through a programmable "divide by N" before being applied to the phase detector as feedback. Here the oscillator frequency is forced to be equal to "N times" the reference frequency and it is this frequency output which is the desired output signal and not a voltage. In this case, the AD650 offers compact size and wide dynamic range.

In signal recovery applications of a PLL, the desired output signal is the voltage applied to the oscillator. In these situations a linear relationship between the input frequency and the output voltage is desired; the AD650 makes a superb oscillator for FM demodulation. The wide dynamic range and outstanding linearity of the AD650 VFC allow simple embodiment of high performance analog signal isolation or telemetry systems. The circuit shown in Figure 14 uses a digital phase detector which also provides proper feedback in the event of unequal frequencies. Such phase-frequency detectors (PFDs) are available in integrated form. For a full discussion of phase lock loop circuits see Reference 3.

An analysis of this circuit must begin at the 7474 dual D flip flop. When the input carrier matches the output carrier in both phase and frequency, the Q outputs of the flip flops will rise at exactly the same time. With two zeros, then two ones on the inputs of the exclusive or (XOR) gate, the output will remain low keeping the DMOS FET switched off. Also, the NAND gate will go low resetting the flip-flops to zero. Throughout the

[3]"Phase lock Techniques," 2nd Edition, by F.M. Gardner, (John Wiley and Sons, 1979)

entire cycle just described, the DMOS integrator gate remained off, allowing the voltage at the integrator output to remain unchanged from the previous cycle. However, if the input carrier leads the output carrier by a few degrees, the XOR gate will be turned on for the small time span that the two signals are mismatched. Since Q_2 will be low during the mismatch time, a negative current will be fed into the integrator, causing its output voltage to rise. This in turn will increase the frequency of the AD650 slightly, driving the system towards synchronization. In a similar manner, if the input carrier lags the output carrier, the integrator will be forced down slightly to synchronize the two signals.

Using a mathematical approach, the ±25 µA pulses from the phase detector are incorporated into the phase detector gain, K_d.

$$K_d = \frac{25\,\mu A}{2\pi} = 4\times10^{-6} \quad amperes/radian \tag{9}$$

Also, the V/F converter is configured to produce 1 MHz in response to a 10 volt input, so its gain K_o, is:

$$K_o = \frac{2\,\pi\times1\times10^{6}\ Hz}{10\ V} = 6.3\times10^{5}\ \frac{radians}{volt\ \bullet\ \sec} \tag{10}$$

The dynamics of the phase relationship between the input and output signals can be characterized as a second order system with natural frequency ω_n:

$$\omega_n = \sqrt{\frac{K_o K_d}{C}} \tag{11}$$

and damping factor

$$\zeta = \frac{R\sqrt{C\,K_o K_d}}{2} \tag{12}$$

For the values shown in Figure 14, these relations simplify to a natural frequency of 35 kHz with a damping factor of 0.8.

For those desiring a simple approach to determining component values for other PLL frequencies and VFC full-scale voltage, the following cookbook steps can be used:

1. Determine K_o (in units of radians per volt second) from the maximum input carrier frequency F_{MAX} (in hertz) and the maximum output voltage V_{MAX}.

$$K_o = \frac{2\,\pi\times F_{MAX}}{V_{MAX}} \tag{13}$$

2. Calculate a value for C based upon the desired loop bandwidth, f_n. Note that this is the desired frequency range of the output signal. The loop bandwidth (f_n) is *not* the maximum carrier frequency (f_{MAX}): the signal may be very narrow even though it is transmitted over a 1 MHz carrier.

$$C = \frac{K_o}{f_n^2}\bullet1\times10^{-7}\frac{V\bullet F}{Rad\bullet\sec} \qquad \begin{array}{l}\text{C units FARADS}\\ \text{f}_\text{n}\text{ units HERTZ}\\ \text{K}_\text{o}\text{ units RAD/VOLT•SEC}\end{array} \tag{14}$$

3. Calculate R to yield a damping factor of approximately 0.8 using this equation:

$$R = \frac{f_n}{K_o}\bullet2.5\times10^{6}\,\frac{Rad\bullet\Omega}{V} \qquad \begin{array}{l}\text{R units OHMS}\\ \text{f}_\text{n}\text{ units HERTZ}\\ \text{K}_\text{o}\text{ units RAD/VOLT•SEC}\end{array} \tag{15}$$

If in actual operation the PLL overshoots or hunts excessively before reaching a final value, the damping factor may be raised by increasing the value of R. Conversely, if the PLL is overdamped, a smaller value of R should be used.

PLL PERFORMANCE

The performance of the PLL circuit is demonstrated by the system shown in Figure 15; an analog signal is converted into a frequency, and then this frequency is converted back into an analog voltage by the PLL.

The source of the frequency input signal used to drive the PLL is an AD650 with two separate inputs: one for dc to set the carrier frequency, and one for ac to establish a modulation. Note how the summing junction input to the AD650 allows such flexibility. The output frequency is then relayed to the PLL via a

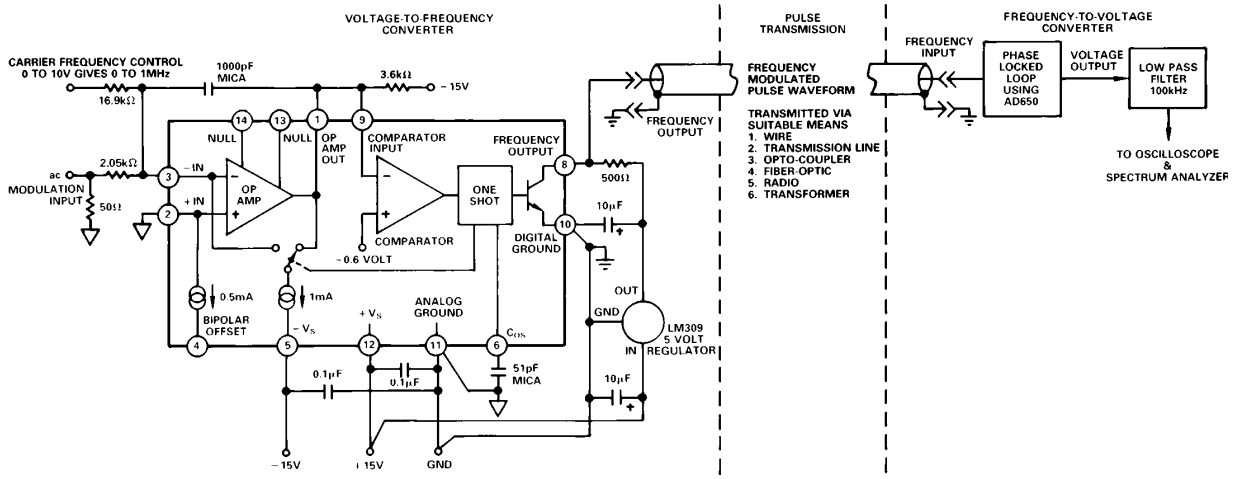


Figure 15.

jumper cable. The signal at this point is a 5 volt digital pulse train and as such may be transmitted in any fashion suitable to the application at hand. For example, galvanic isolation is achieved with a simple transformer or opto-isolator; extremely high voltage isolation or transmission through severe RF environments can be accomplished with a fiber-optic link; telemetry can be accomplished with a radio link. The actual method of conveying the pulses is not crucial to the system performance. The PLL is the circuit shown in Figure 14, and the filter shown on the output signal is simply to attenuate carrier feedthrough to allow easy interpretation of the signal with an oscilloscope and spectrum analyzer.

The step response of the system is shown in Figure 16a. The signal output is swinging between 5 volts and 10 volts, for an input step of 500 kHz to 1 MHz. Note that the AD650 is actually overshooting to 1.1 MHz and the response remains well controlled. Note the slight irregularity during the transition: this is caused by cycle slipping during the slew where feedback is lost temporarily and the PLL actually loses phase lock. The frequency response of the system when driven with sine wave excitation is shown in Figure 16b. Here the output level is set to 2 volts peak-to-peak, and the carrier is 800 kHz. Note that the –3 dB bandwidth is about 70 kHz, which is consistent with a damping factor of 0.8 and a natural frequency of 35 kHz.[4] When an unmodulated carrier is applied to the PLL, the noise that appears at the output determines the dynamic range of the system. The spectrum of the noise at the output of the PLL is shown in Figure 16c. By comparing this with Figure 16b, the dynamic range of the system is seen to be 80 dB. The harmonic distortion of the system is shown in Figure 16d. The output is a 2 V p-p sine wave at 5 kHz, and the amplitude of the first harmonic is seen to be 48 dB below the fundamental. The harmonic distortion can be improved to the level of 60 dB by reducing the amplitude of the modulation, but this is at the expense of dynamic range since the intensity of the noise floor remains constant.

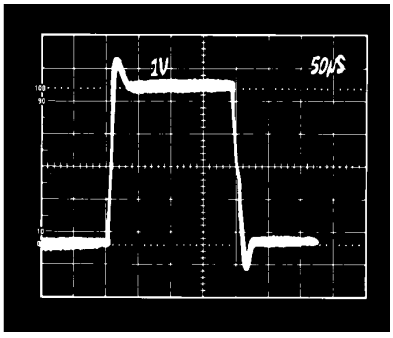


Figure 16a. Step Response

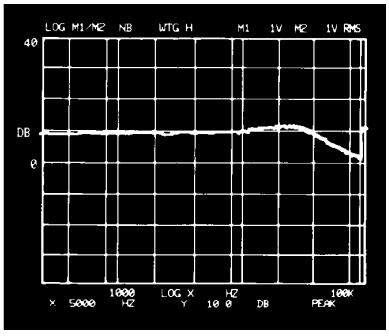


Figure 16b. Frequency Response

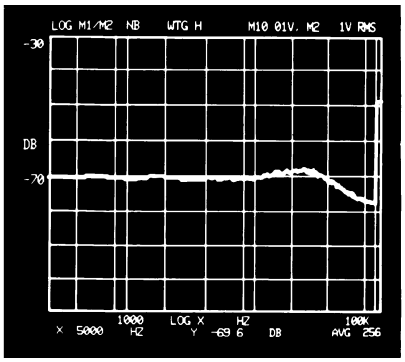


Figure 16c. Noise Output from PLL

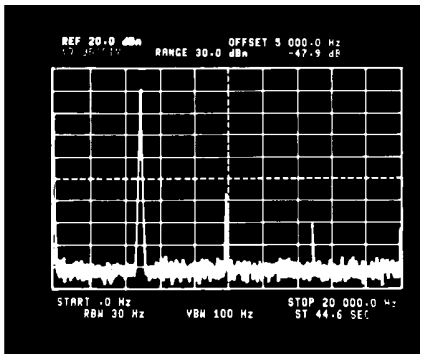
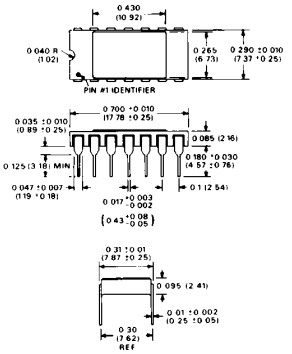


Figure 16d. Harmonic Distortion of PLL System

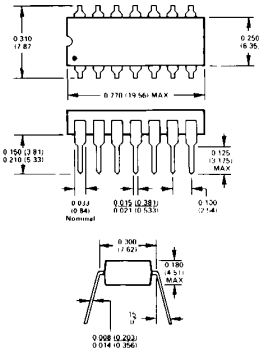
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

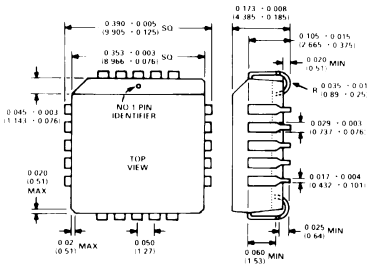
"D" Package (TO-116) Ceramic DIP



"N" Package Plastic DIP



"P" Package PLCC



[4]See page 13 of reference 3.

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