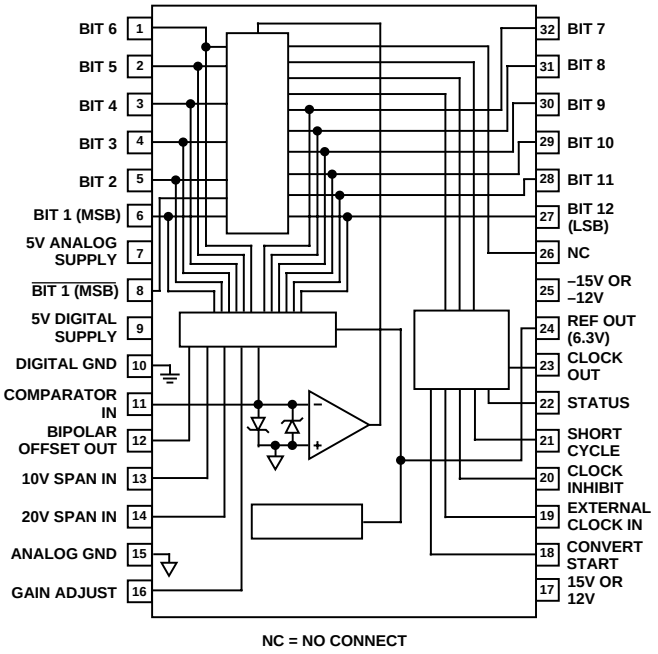
12-Bit Successive-Approximation Integrated Circuit A/D Converter

AD ADC80

FEATURES

True 12-Bit Operation: Max Nonlinearity ±0.012%
Low Gain T.C.: ±30 ppm/°C Max
Low Power: 800 mW
Fast Conversion Time: 25 μs
Precision 6.3 V Reference for External Application
Short-Cycle Capability
Parallel Data Output
Monolithic DAC with Scaling Resistors for Stability
Low Chip Count—High Reliability
Industry Standard Pinout
"Z" Models for ±12 V Supplies

FUNCTIONAL BLOCK DIAGRAM



NC = NO CONNECT

PRODUCT DESCRIPTION

The AD ADC80 is a complete 12-bit successive-approximation analog-to-digital converter that includes an internal clock, reference, and comparator. Its hybrid IC design uses MSI digital and linear monolithic chips in conjunction with a 12-bit monolithic DAC to provide modular performance and versatility with IC size, price, and reliability.

Important performance characteristics of the AD ADC80 include a maximum linearity error at 25°C of ±0.012%, max gain T.C. of 30 ppm/°C, typical power dissipation of 800 mW, and max conversion time of 25 μs. Monotonic operation of the feedback D/A converter guarantees no missing codes over the temperature range of –25°C to +85°C.

The design of the AD ADC80 includes scaling resistors that provide analog signal ranges of ±2.5 V, ±5.0 V, ±10 V, 0 V to 5.0 V, or 0 V to 10.0 V. The 6.3 V precision reference may be used for external applications. All digital signals are fully DTL and TTL compatible; output data is in parallel form.

The AD ADC80 is available in grades specified for use over the –25°C to +85°C temperature range and is available in a 32-lead ceramic DIP.

PRODUCT HIGHLIGHTS

1. The AD ADC80 is a complete 12-bit A/D converter. No external components are required to perform a conversion.
2. A monolithic 12-bit feedback DAC is used for reduced chip count and higher reliability.
3. The internal buried Zener reference is laser trimmed to 6.3 V. The reference voltage is available externally and can supply up to 1.5 mA beyond that required for the reference and bipolar offset current.
4. The scaling resistors are included on the monolithic DAC for exceptional thermal tracking.
5. The AD ADC80 directly replaces other devices of this type with significant increases in performance.
6. The fast conversion rate of the AD ADC80 makes it an excellent choice for applications requiring high system throughput rates.
7. The short cycle and external clock options are provided for applications requiring faster conversion speeds or lower resolutions.

REV. B

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

AD ADC80–SPECIFICATIONS (Typical @ 25°C, ±15 V, and +5 V, unless otherwise noted.)

Model	AD ADC80-12	Unit
RESOLUTION	12	Bits
ANALOG INPUTS		
Voltage Ranges		
Bipolar	±2.5, ±5, ±10	V
Unipolar	0, +5, +10	V
Impedance (Direct Input)	0 to +5, ±2.5	V
	0 to +10, ±5	V
	±10	V
DIGITAL INPUTS[1]		
Convert Command	Positive Pulse 100 ns Wide (min)	
("0" to "1" Initiates Conversion)		
Logic Loading	1	TTL Load
External Clock	1	TTL Load
TRANSFER CHARACTERISTICS ERROR		
Gain Error[2]	±0.1	% of FSR[3]
Offset[2]		
Unipolar	±0.05	% of FSR
Bipolar	±0.1	% of FSR
Linearity Error (max)[4]	±0.012	% of FSR
Inherent Quantization Error	±1/2	LSB
Differential Linearity Error	±1/2	LSB
No Missing Codes Temperature Range	–25 to +85	°C
Power Supply Sensitivity		
±15 V	±0.0030	% of FSR/% V_S
+5 V	±0.0015	% of FSR/% V_S
DRIFT		
Specification Temperature Range	–25 to +85	°C
Gain (max)	±30	ppm/°C
Offset		
Unipolar	±3	ppm of FSR/°C
Bipolar	±15	ppm of FSR/°C
Linearity (max)	±3	ppm of FSR/°C
Monotonicity	GUARANTEED	
CONVERSION SPEED[5]	22, 25	µs min, µs max
DIGITAL OUTPUT (All Codes Complementary)		
Parallel		
Output Codes[6]		
Unipolar	CSB	
Bipolar	COB, CTC	
Output Drive	2	TTL Loads
Status	Logic "1" During Conversion	
Status Output Drive	2	TTL Loads
Internal Clock		
Clock Output Drive	2	TTL Loads
Frequency[7]	575	kHz
INTERNAL REFERENCE VOLTAGE	+6.3, ±10	V ± mV
Max External Current		
(With No Degradation of Specifications)	1.5	mA
Tempco of Drift	±10, ±20	ppm/°C typ, ppm/°C max

Model	AD ADC80-12	Unit
POWER REQUIREMENTS		
Rated Voltages	±15, +5	V
Range for Rated Accuracy	4.75 to 5.25 and ±14.0 to ±16.0	V
Z Models[8]	4.75 to 5.25 and ±11.4 to ±16.0	V
Supply Drain +15 V	+10	mA
–15 V	–20	mA
+5 V	+70	mA
TEMPERATURE RANGE		
Specification	–25 to +85	°C
Operating (Derated Specifications)	–55 to +100	°C
Storage	–55 to +125	°C
PACKAGE OPTION[9]		
DH-32D	AD ADC80-12	

NOTES
[1]DTL/TTL compatible, i.e., Logic "0" = 0.8 V max, Logic "1" = 2.0 V min for digital inputs, Logic "0" = 0.4 V max, and Logic "1" = 2.4 V min digital outputs.
[2]Adjustable to zero with external trimpots.
[3]FSR means Full-Scale Range, i.e., unit connected for ±10 V range has 20 V FSR.
[4]Error shown is the same as ±1/2 LSB max for resolution of A/D converter.
[5]Conversion time with internal clock.
[6]See Table I. CSB—Complementary Straight Binary
COB—Complementary Offset Binary
CTC—Complementary Twos Complement
[7]For conversion speeds specified.
[8]For Z models order AD ADC80Z-12.
[9]For package outline information see Package Information section.

Specifications subject to change without notice.

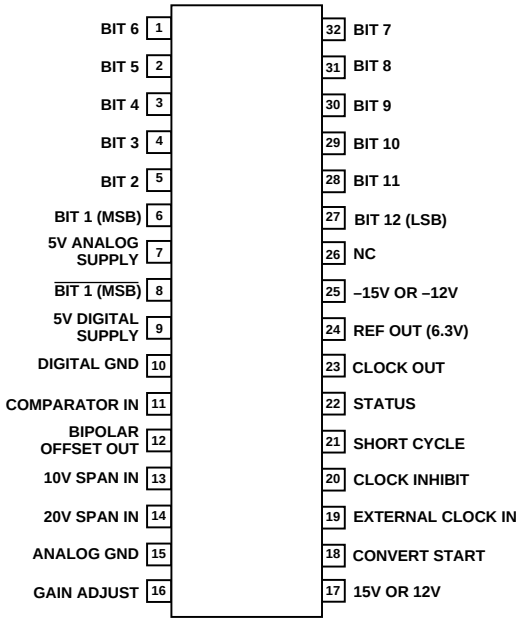
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD ADC80-12	–25°C to +85°C	32-Lead Ceramic DIP	DH-32D
AD ADC80-Z-12	–25°C to +85°C	32-Lead Ceramic DIP	DH-32D

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD ADC80 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

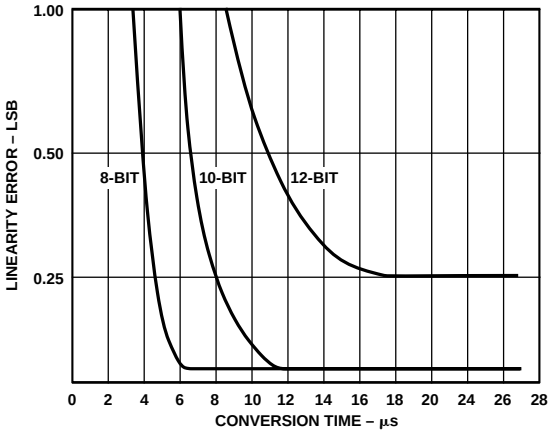
PIN CONFIGURATION



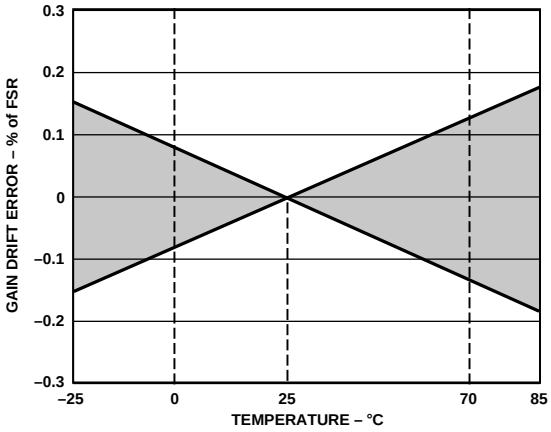
NC = NO CONNECT

PIN FUNCTION DESCRIPTIONS

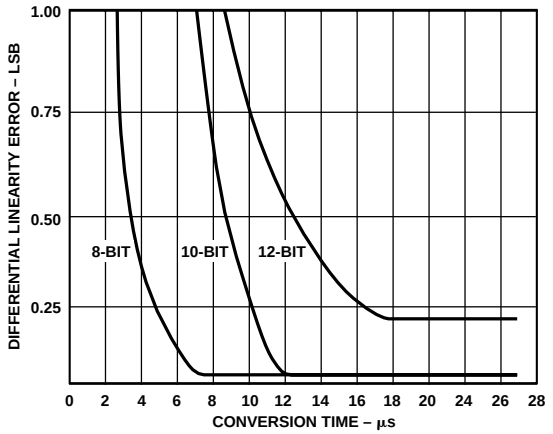
Pin No.	Mnemonic	Function
1–6	BIT 6–BIT 1 (MSB)	Digital Outputs
7	5 V ANALOG SUPPLY	Analog Positive Supply (nominally ±0.25 V)
8	$\overline{\text{BIT 1 (MSB)}}$	$\overline{\text{MSB}}$ Inverted Digital Output
9	5 V DIGITAL SUPPLY	Digital Positive Supply (nominally ±0.25 V)
10	DIGITAL GND	Digital Ground
11	COMPARATOR IN	Offset Adjust
12	BIPOLAR OFFSET OUT	Bipolar Offset Output
13	10 V SPAN IN	Analog Input 10 V Signal Range
14	20 V SPAN IN	Analog Input 20 V Signal Range
15	ANALOG GND	Analog Ground
16	GAIN ADJUST	Gain Adjust
17	15 V OR 12 V	Analog Positive Supply (nominally ±1.0 V for 15 V or ±0.6 V for 12 V)
18	CONVERT START	Enables Conversion
19	EXTERNAL CLOCK IN	External Clock Input
20	CLOCK INHIBIT	Clock Inhibit
21	SHORT CYCLE	Shortens Conversion Cycle to Desired Resolution
22	STATUS	Logic High, ADC Converting/Logic Low, ADC Data Valid
23	CLOCK OUT	Internal Clock Output
24	REF OUT (6.3 V)	6.3 V Reference Output
25	–15 V OR –12 V	Analog Negative Supply (nominally ±1.0 V for –15 V or ±0.6 V for –12 V)
26	NC	No Connection
27–32	BIT 12 (LSB)–BIT 7	Digital Outputs



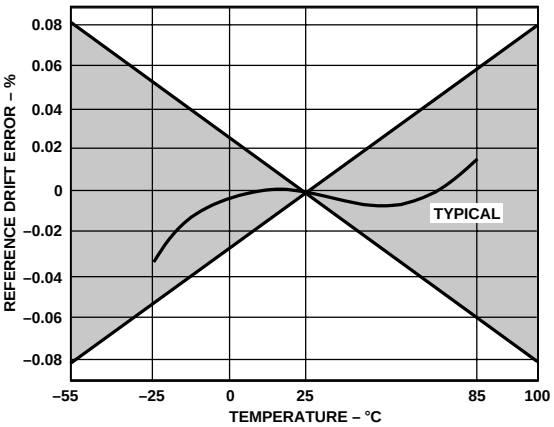
TPC 1. Linearity Error vs. Conversion Time (Normalized)



TPC 3. Maximum Gain Drift Error, % of FSR vs. Temperature



TPC 2. Differential Linearity Error vs. Conversion Time (Normalized)



TPC 4. Reference Drift, % Error vs. Temperature

THEORY OF OPERATION

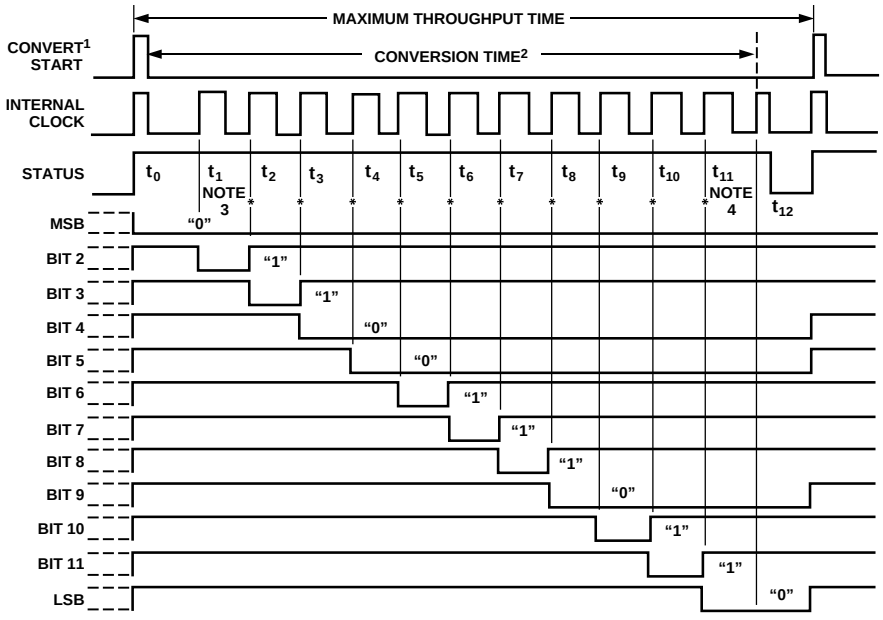
On receipt of a CONVERT START command, the AD ADC80 converts the voltage at its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 1. Receipt of a CONVERT START signal sets the STATUS flag, indicating conversion in progress. This, in turn, removes the inhibit applied to the gated clock, permitting it to run through 13 cycles. All SAR parallel bit and STATUS flip-flops are initialized on the leading edge, and the gated clock inhibit signal is removed on the trailing edge of the CONVERT START signal. At time t_0, B_1 is reset and B_2–B_{12} are set unconditionally. At t_1, the Bit 1 decision is made (keep) and Bit 2 is unconditionally reset. At t_2, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t_{12}. After a 40 ns delay period, the STATUS flag is reset, indicating that the conversion is complete and that the parallel output data is valid. Resetting the STATUS flag restores the gated clock inhibit signal, forcing the clock output to the Logic "0" state.

Parallel data bits become valid on the positive-going clock edge (see Figure 1).

Incorporation of this 40 ns delay guarantees that the parallel data is valid at the Logic "l" to "0" transition of the STATUS flag, permitting parallel data transfer to be initiated by the trailing edge of the STATUS signal.



NOTES
[1]THE CONVERT START PULSEWIDTH IS 100ns MIN AND MUST REMAIN LOW DURING A CONVERSION; THE CONVERSION IS INITIATED BY THE "RISING EDGE" OF THE CONVERT COMMAND
[2]25μs FOR 12 BITS AND 21μs FOR 10 BITS (MAX)
[3]MSB DECISION
[4]LSB DECISION 40ns PRIOR TO THE STATUS GOING LOW
*BIT DECISIONS

Figure 1. Timing Diagram (Binary Code 011001110110)

DIGITAL OUTPUT DATA

Parallel data from TTL storage registers is in negative true form. Parallel data output coding is complementary binary for unipolar ranges and either complementary offset binary or complementary twos complement binary, depending on whether Bit 1 (Pin 6) or its logical inverse Bit 1 (Pin 8) is used as the MSB. Parallel data becomes valid approximately 40 ns before the STATUS flag returns to Logic "0," permitting parallel data transfer to be clocked on the "1" to "0" transition of the STATUS flag.

Parallel data outputs change state on positive-going clock edges. There are 13 negative-going clock edges in the complete 12-bit conversion cycle, as shown in Figure 1. The first edge shifts an invalid bit into the register, which is shifted out on the 13th negative-going clock edge.

Short Cycle Input

A Short Cycle Input, Pin 21, permits the timing cycle shown in Figure 1 to be terminated after any number of desired bits has been converted, permitting somewhat shorter conversion times in applications not requiring full 12-bit resolution. When 10-bit resolution is desired, Pin 21 is connected to Bit 11, output Pin 28. The conversion cycle then terminates, and the STATUS flag resets after the Bit 10 decision (t_{10} + 40 ns in timing diagram of Figure 1). Short Cycle pin connections and associated maximum 12-, 10-, and 8-bit conversion times are summarized in Table I. When 12-bit resolution is required, Pin 21 is connected to 5 V (Pin 9).

INPUT SCALING

The AD ADC80 input should be scaled as close to the maximum input signal range as possible to use the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 2 for circuit details.

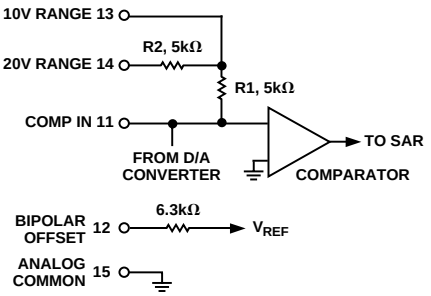


Figure 2. Input Scaling Circuit

Table I. Short Cycle Connections

Connect Short Cycle Pin 21 to Pin	Resolution Bits	(% FSR)	Maximum Conversion Time (μs)	Status Flag Reset
9	12	0.024	25	t_{12} + 40 ns
28	10	0.100	21	t_{10} + 40 ns
30	8	0.390	17	t_8 + 40 ns

Table II. Input Scaling Connections

Input Signal Range	Output Code	Connect Pin 12 to Pin	Connect Pin 14 to	Connect Input Signal to
±10 V	COB or CTC	11	Input Signal	14
±5 V	COB or CTC	11	Open	13
±2.5 V	COB or CTC	11	Pin 11	13
0 V to 5 V	CSB	15	Pin 11	13
0 V to 10 V	CSB	15	Open	13

Table III. Input Voltages and Code Definitions

Binary (BIN) Output Analog Input Voltage Range	Defined As:	±10 V	±5 V	±2.5 V	0 V to 10 V	0 V to 5 V
Code Designation		COB[1] or CTC[2]	COB[1] or CTC[2]	COB[1] or CTC[2]	CSB[3]	CSB[3]
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20\ V}{2^n}$	$\frac{10\ V}{2^n}$	$\frac{5\ V}{2^n}$	$\frac{10\ V}{2^n}$	$\frac{5\ V}{2^n}$
	n = 8	78.13 mV	39.06 mV	19.53 mV	39.06 mV	19.53 mV
	n = 10	19.53 mV	9.77 mV	4.88 mV	9.77 mV	4.88 mV
	n = 12	4.88 mV	2.44 mV	1.22 mV	2.44 mV	1.22 mV

Transition Values MSB LSB						
000 . . . . 000[4]	+Full Scale	10 V – 3/2 LSB	5 V – 3/2 LSB	2.5 V – 3/2 LSB	10 V – 3/2 LSB	5 V – 3/2 LSB
011 111	Midscale	0	0	0	5 V	2.5 V
111 110	–Full Scale	–10 V + 1/2 LSB	–5 V + 1/2 LSB	–2.5 V + 1/2 LSB	0 V + 1/2 LSB	0 V + 1/2 LSB

NOTES
[1]COB = Complementary Offset Binary
[2]CTC = Complementary Twos Complement—obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on Pin 8.
[3]CSB = Complementary Straight Binary
[4]Voltages given are the nominal value for transition to the code specified.

OFFSET ADJUSTMENT

The zero adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 1.8 MΩ resistor to Comparator Input Pin 11 for all ranges. As shown in Figure 3 the tolerance of this fixed resistor is not critical, and a carbon composition type is generally adequate. Using a carbon composition resistor having a –1200 ppm/°C tempco contributes a worst-case offset tempco of $8 \times 244 \times 10^{-6} \times 1200$ ppm/°C = 2.3 ppm/°C of FSR, if the OFFSET ADJ potentiometer is set at either end of its adjustment range. Since the maximum offset adjustment required is typically no more than ±4 LSB, use of a carbon composition offset summing resistor typically contributes no more than 1 ppm/°C of FSR offset tempco.

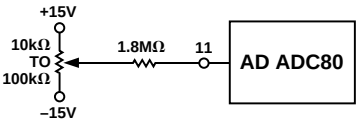


Figure 3. Offset Adjustment Circuit

An alternate offset adjust circuit, which contributes negligible offset tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 4.

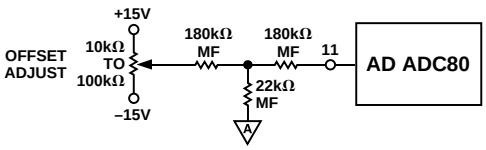


Figure 4. Low Tempco Zero Adjustment Circuit

In either zero adjust circuit, the fixed resistor connected to Pin 11 should be located close to this pin to keep the Pin 11 connection runs short. Comparator Input Pin 11 is quite sensitive to external noise pickup.

GAIN ADJUSTMENT

The gain adjust circuit consists of a potentiometer connected across $\pm V_S$ with its slider connected through a 10 MΩ resistor to the gain adjust Pin 16 as shown in Figure 5.

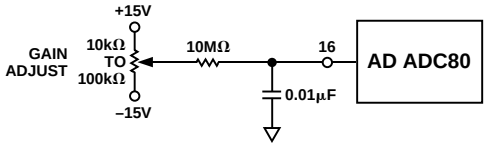


Figure 5. Gain Adjustment Circuit

An alternate gain adjust circuit, which contributes negligible gain tempco if metal film resistors (tempco <100 ppm/°C) are used, is shown in Figure 6.

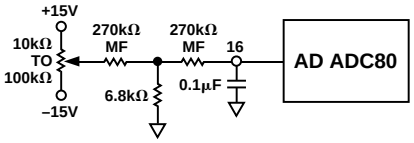


Figure 6. Low Tempco Gain Adjustment Circuit

CALIBRATION

External ERO ADJ and GAIN ADJ potentiometers, connected as shown in Figures 7 and 8, are used for device calibration. To prevent interaction of these two adjustments, Zero is always adjusted first and then Gain. Zero is adjusted with the analog input near the most negative end of the analog range (0 for unipolar and –FS for bipolar input ranges). Gain is adjusted with the analog input near the most positive end of the analog range.

0 to 10 V Range

Set analog input to +1 LSB = 0.0024 V. Adjust Zero for digital output = 111111111110. Zero is now calibrated. Set analog input to +FSR – 2 LSB = 9.9952 V. Adjust Gain for 000000000001 digital output code. Full-scale (Gain) is now calibrated. For half-scale calibration check set analog input to 5.0000 V; digital output code should be 011111111111.

–10 V to +10 V Range

Set analog input to –9.9951 V, adjust Zero for 111111111110 digital output (complementary offset binary) code. Set analog input to +9.9902 V, adjust Gain for 000000000001 digital output (complementary offset binary) code. For half-scale calibration check, set analog input to 0.0000 V; digital output (complementary offset binary) code should be 011111111111.

Other Ranges

Representative digital coding for 0 V to 10 V and –10 V to +10 V ranges is given above. Coding relationships and calibration points for 0 V to 5 V, –2.5 V to +2.5 V, and –5 V to +5 V ranges can be found by halving the corresponding code equivalents listed for the 0 V to 10 V and –10 V to +10 V ranges, respectively.

Zero and full-scale calibration can be accomplished to a precision of approximately ±1/4 LSB using the static adjustment procedure described above. By summing a small sine- or triangular-wave voltage with the signal applied to the analog input, the output can be cycled through each of the calibration codes of interest to more accurately determine the center (or end points) of each discrete quantization level. A detailed description of this dynamic calibration technique is presented in "A/D Conversion Notes," D. Sheingold, Analog Devices, Inc., 1977, Part II, Chapter 3.

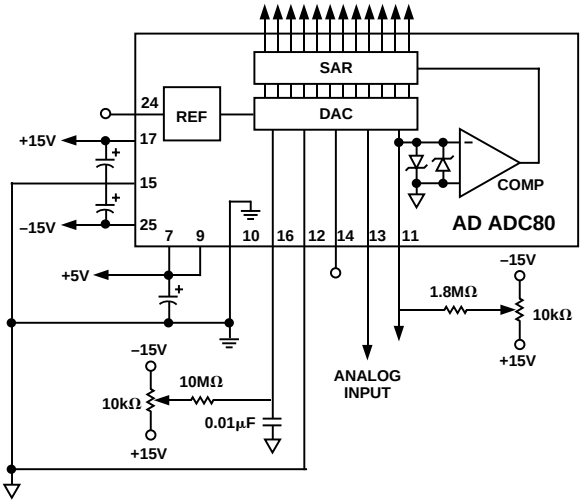


Figure 7. Analog and Power Connections for Unipolar 0 V–10 V Input Range

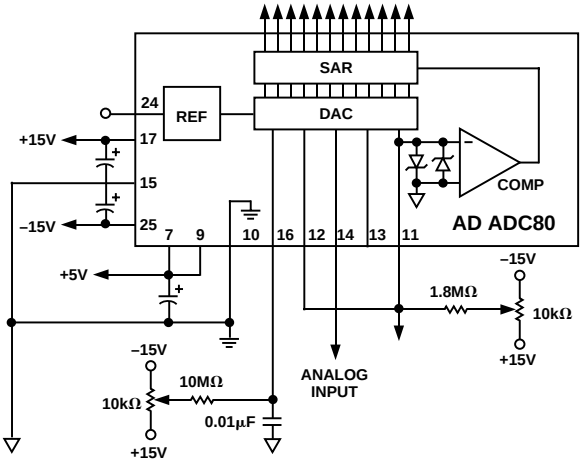


Figure 8. Analog and Power Connections for Bipolar ±10 V Input Range

GROUNDING

Many data-acquisition components have two or more ground pins that are not connected together within the device. These "grounds" are usually referred to as the Logic Power Return, Analog Common (Analog Power Return), and Analog Signal Ground. These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground is desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD ADC80. Therefore, separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point, and the two device grounds should be tied together. In this way, supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

Each of the AD ADC80's supply terminals should be capacitively decoupled as close to the AD ADC80 as possible. A large value capacitor such as 1 µF in parallel with a 0.1 µF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Power Return pin and the logic supply is bypassed to the Logic Power Return pin.

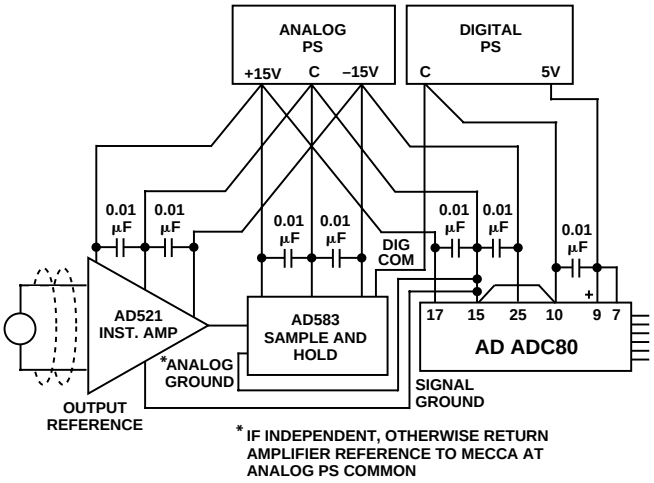


Figure 9. Basic Grounding Practice

CONTROL MODES

The timing sequence of the AD ADC80 allows the device to be easily operated in a variety of systems with different control modes. The most common control modes are illustrated in Figures 10 through 12.

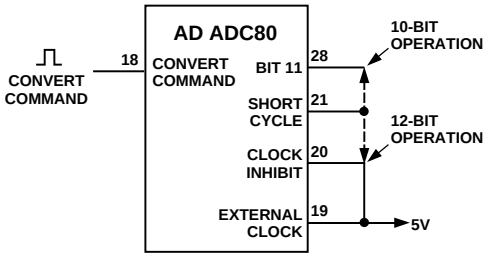


Figure 10. Internal Clock—Normal Operating Mode. Conversion Initiated by the Rising Edge of the Convert Command. The Internal Clock Runs Only During Conversion.

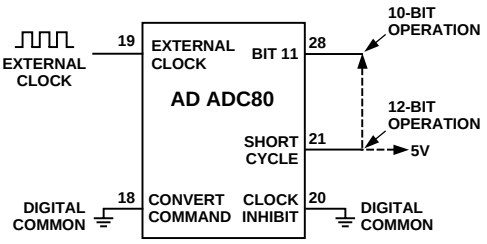


Figure 11. Continuation Conversion with External Clock. Conversion Is Initiated by 14th Clock Pulse. Clock Runs Continuously.

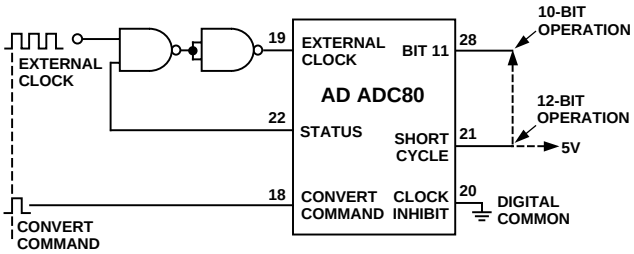
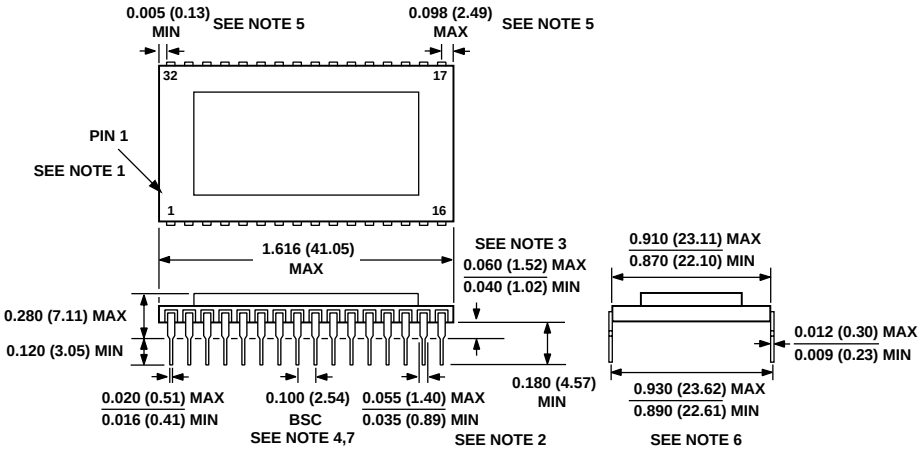


Figure 12. Continuous External Clock. Conversion Initiated by Rising Edge of Convert Command. The Convert Command Must Be Synchronized with Clock.

OUTLINE DIMENSIONS

32-Lead Side Brazed Ceramic DIP for Hybrid [Medium Cavity]
(DH-32D)

Dimensions shown in inches and (millimeters)



NOTES
1. INDEX AREA; A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE
2. THE MINIMUM LIMIT FOR THE DIMENSION MAY BE 0.023" (0.58 MM) FOR ALL FOUR CORNER LEADS ONLY
3. THE DIMENSION SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE
4. THE BASIC PIN SPACING IS 0.100" (2.54 MM) BETWEEN CENTER LINES
5. APPLIES TO ALL FOUR CORNERS
6. THE DIMENSION SHALL BE MEASURED AT THE CENTER LINE OF THE LEADS
7. THIRTY SPACES

Revision History

Location	Page
9/02—Data Sheet changed from REV. A to REV. B.	
Edit to Figure 1	6
OUTLINE DIMENSIONS Replaced	11

C01202–0–9/02(B)

PRINTED IN U.S.A.