

FEATURES

High DC Precision

- 75 μV Max Offset Voltage
- 1 $\mu\text{V}/^\circ\text{C}$ Max Offset Voltage Drift
- 150 pA Max Input Bias Current
- 0.2 pA/ $^\circ\text{C}$ Typical I_B Drift

Low Noise

- 0.5 μV p-p Typical Noise, 0.1 Hz to 10 Hz

Low Power

- 600 μA Max Supply Current per Amplifier
- MIL-STD-883B Processing Available
- Available in Tape and Reel in Accordance with EIA-481A Standard
- Dual Version: AD706

APPLICATIONS

- Industrial/Process Controls
- Weigh Scales
- ECG/EKG Instrumentation
- Low Frequency Active Filters

PRODUCT DESCRIPTION

The AD704 is a quad, low power bipolar op amp that has the low input bias current of a BiFET amplifier but which offers a significantly lower I_B drift over temperature. It utilizes super-beta bipolar input transistors to achieve picoampere input bias current levels (similar to FET input amplifiers at room temperature), while its I_B typically only increases by $5\times$ at 125°C (unlike a BiFET amp, for which I_B doubles every 10°C resulting in a $1000\times$ increase at 125°C). Furthermore, the AD704 achieves 75 μV offset voltage and low noise characteristics of a precision bipolar input op amp.

Since it has only 1/20 the input bias current of an AD OP07, the AD704 does not require the commonly used "balancing" resistor. Furthermore, the current noise is 1/5 that of the AD OP07 which makes the AD704 usable with much higher source impedances. At 1/6 the supply current (per amplifier) of the AD OP07, the AD704 is better suited for today's higher density circuit boards and battery-powered applications.

The AD704 is an excellent choice for use in low frequency active filters in 12- and 14-bit data acquisition systems, in precision instrumentation, and as a high quality integrator. The AD704 is internally compensated for unity gain and is available in five performance grades. The AD704J and AD704K are rated over the commercial temperature range of 0°C to 70°C . The AD704A is rated over the industrial temperature of -40°C to $+85^\circ\text{C}$. The AD704T is rated over the military temperature range of -55°C to $+125^\circ\text{C}$ and is available processed to MIL-STD-883B, Rev. C.

CONNECTION DIAGRAMS

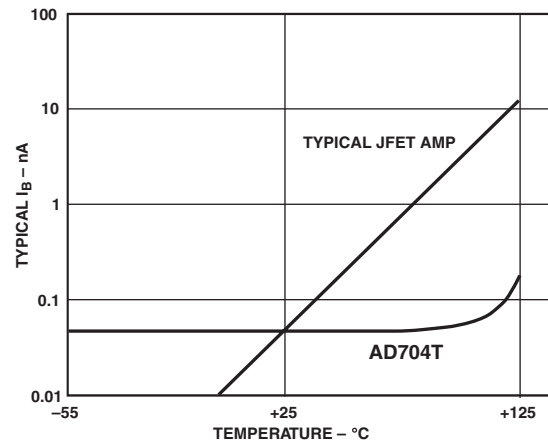
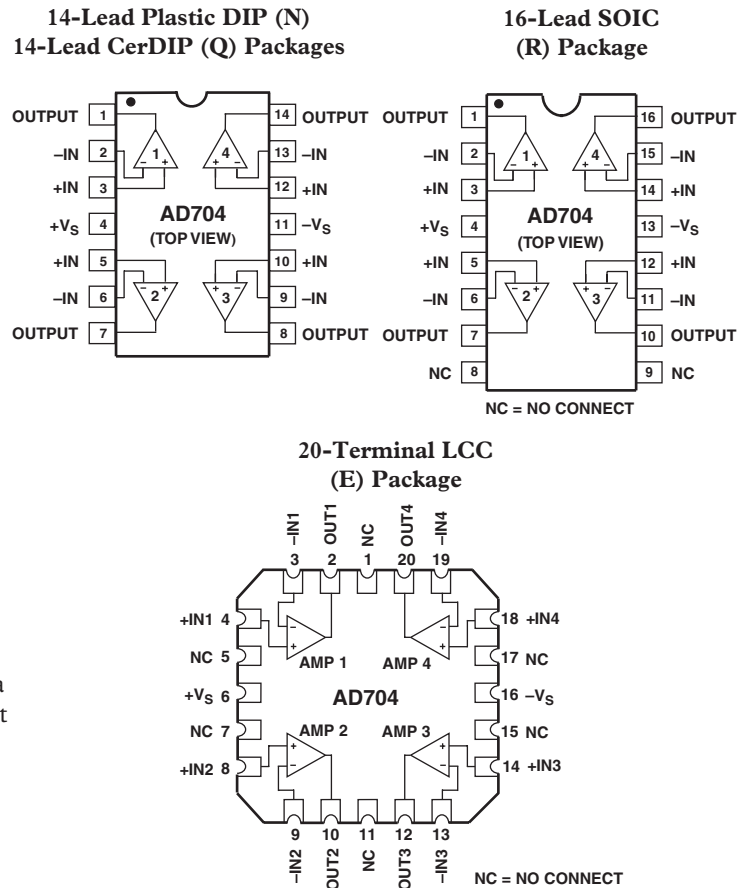


Figure 1. Input Bias Current Over Temperature

REV. C

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AD704—SPECIFICATIONS (@ $T_A = 25^\circ\text{C}$, $V_{CM} = 0\text{ V}$, and $\pm 15\text{ V}$ dc, unless otherwise noted.)

Parameters	Conditions	AD704J/A			AD704K			AD704T			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
INPUT OFFSET VOLTAGE											
Initial Offset			50	150		30	75		30	100	μV
Offset	$T_{\text{MIN}}-T_{\text{MAX}}$		100	250		50	150		80	150	μV
vs. Temp, Average TC			0.2	1.5		0.2	1.0			1.0	$\mu\text{V}/^\circ\text{C}$
vs. Supply (PSRR)	$V_S = \pm 2$ to $\pm 18\text{ V}$	100	132		112	132		112	132		dB
$T_{\text{MIN}}-T_{\text{MAX}}$	$V_S = \pm 2.5$ to $\pm 18\text{ V}$	100	126		108	126		108	126		dB
Long-Term Stability			0.3			0.3			0.3		$\mu\text{V}/\text{month}$
INPUT BIAS CURRENT¹											
	$V_{CM} = 0\text{ V}$		100	270		80	150		80	200	pA
	$V_{CM} = \pm 13.5\text{ V}$			300			200			250	pA
vs. Temp, Average TC			0.3			0.2			1.0		$\text{pA}/^\circ\text{C}$
$T_{\text{MIN}}-T_{\text{MAX}}$	$V_{CM} = 0\text{ V}$			300			200			600	pA
	$V_{CM} = \pm 13.5\text{ V}$			400			300			700	pA
INPUT OFFSET CURRENT											
	$V_{CM} = 0\text{ V}$		80	250		30	100		50	150	pA
	$V_{CM} = \pm 13.5\text{ V}$			300			150			200	pA
vs. Temp, Average TC			0.6			0.4			0.4		$\text{pA}/^\circ\text{C}$
$T_{\text{MIN}}-T_{\text{MAX}}$	$V_{CM} = 0\text{ V}$		100	300		80	200		80	400	pA
	$V_{CM} = \pm 13.5\text{ V}$		100	400		80	300		100	500	pA
MATCHING CHARACTERISTICS											
Offset Voltage				250			130			150	μV
	$T_{\text{MIN}}-T_{\text{MAX}}$			400			200			250	μV
Input Bias Current ²				500			300			400	pA
	$T_{\text{MIN}}-T_{\text{MAX}}$			600			400			600	pA
Common-Mode Rejection ³		94			110			104			dB
	$T_{\text{MIN}}-T_{\text{MAX}}$	94			104			104			dB
Power Supply Rejection ⁴		94			110			110			dB
	$T_{\text{MIN}}-T_{\text{MAX}}$	94			106			106			dB
Crosstalk ⁵	$f = 10\text{ Hz}$ $R_{\text{LOAD}} = 2\text{ k}\Omega$		150			150			150		dB
FREQUENCY RESPONSE											
UNITY GAIN											
Crossover Frequency			0.8			0.8			0.8		MHz
Slew Rate, Unity Gain	$G = -1$		0.15			0.15			0.15		$\text{V}/\mu\text{s}$
Slew Rate	$T_{\text{MIN}}-T_{\text{MAX}}$		0.1			0.1			0.1		$\text{V}/\mu\text{s}$
INPUT IMPEDANCE											
Differential			40 2			40 2			40 2		$\text{M}\Omega \text{pF}$
Common-Mode			300 2			300 2			300 2		$\text{G}\Omega \text{pF}$
INPUT VOLTAGE RANGE											
Common-Mode Voltage			± 13.5	± 14		± 13.5	± 14		± 13.5	± 14	V
Common-Mode Rejection Ratio	$V_{CM} = \pm 13.5\text{ V}$	100	132		114	132		110	132		dB
	$T_{\text{MIN}}-T_{\text{MAX}}$	98	128		108	128		108	128		dB
INPUT CURRENT NOISE											
	0.1 to 10 Hz		3			3			3		pA p-p
	$f = 10\text{ Hz}$		50			50			50		$\text{fA}/\sqrt{\text{Hz}}$
INPUT VOLTAGE NOISE											
	0.1 to 10 Hz		0.5			0.5	2.0		0.5	2.0	$\mu\text{V p-p}$
	$f = 10\text{ Hz}$		17			17			17		$\text{nV}/\sqrt{\text{Hz}}$
	$f = 1\text{ kHz}$		15	22		15	22		15	22	$\text{nV}/\sqrt{\text{Hz}}$
OPEN-LOOP GAIN											
	$V_O = \pm 12\text{ V}$		200	2000		400	2000		400	2000	V/mV
	$R_{\text{LOAD}} = 10\text{ k}\Omega$										V/mV
	$T_{\text{MIN}}-T_{\text{MAX}}$		150	1500		300	1500		300	1500	V/mV
	$V_O = \pm 10\text{ V}$		200	1000		300	1000		200	1000	V/mV
	$R_{\text{LOAD}} = 2\text{ k}\Omega$										V/mV
	$T_{\text{MIN}}-T_{\text{MAX}}$		150	1000		200	1000		100	1000	V/mV

Parameters	Conditions	AD704J/A			AD704K			AD704T			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OUTPUT CHARACTERISTICS											
Voltage Swing	$R_{LOAD} = 10\text{ k}\Omega$	± 13	± 14		± 13	± 14		± 13	± 14		V
Current	$T_{MIN}-T_{MAX}$ Short Circuit		± 15			± 15			± 15		mA
CAPACITIVE LOAD											
Drive Capability	Gain = 1		10,000			10,000			10,000		pF
POWER SUPPLY											
Rated Performance			± 15			± 15			± 15		V
Operating Range		± 2.0		± 18	± 2.0		± 18	± 2.0		± 18	V
Quiescent Current			1.5	2.4		1.5	2.4		1.5	2.4	mA
	$T_{MIN}-T_{MAX}$		1.6	2.6		1.6	2.6		1.6	2.6	mA
TRANSISTOR COUNT	# of Transistors		180			180			180		

NOTES

¹Bias current specifications are guaranteed maximum at either input.

²Input bias current match is the maximum difference between corresponding inputs of all four amplifiers.

³CMRR match is the difference of $\Delta V_{OS}/\Delta V_{CM}$ between any two amplifiers, expressed in dB.

⁴PSRR match is the difference between $\Delta V_{OS}/\Delta V_{SUPPLY}$ for any two amplifiers, expressed in dB.

⁵See Figure 2a for test circuit.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

AD704

ABSOLUTE MAXIMUM RATINGS¹

Supply Voltage	±18 V
Internal Power Dissipation (25°C)	See Note 2
Input Voltage	±V _S
Differential Input Voltage ³	±0.7 V
Output Short-Circuit Duration (Single Input)	Indefinite
Storage Temperature Range	
Q	-65°C to +150°C
N, R	-65°C to +125°C
Operating Temperature Range	
AD704J/K	0°C to 70°C
AD704A	-40°C to +85°C
AD704T	-55°C to +125°C
Lead Temperature Range (Soldering 10 seconds)	300°C

NOTES

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

²Specification is for device in free air:

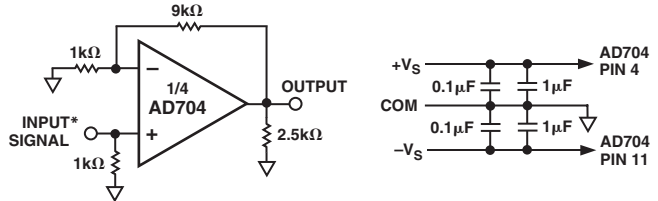
14-Lead Plastic Package: $\theta_{JA} = 150^\circ\text{C}/\text{W}$

14-Lead Cerdip Package: $\theta_{JA} = 110^\circ\text{C}/\text{W}$

16-Lead SOIC Package: $\theta_{JA} = 100^\circ\text{C}/\text{W}$

20-Terminal LCC Package: $\theta_{JA} = 150^\circ\text{C}/\text{W}$

³The input pins of this amplifier are protected by back-to-back diodes. If the differential voltage exceeds ±0.7 volts, external series protection resistors should be added to limit the input current to less than 25 mA.



ALL 4 AMPLIFIERS ARE CONNECTED AS SHOWN

*THE SIGNAL INPUT (SUCH THAT THE AMPLIFIER'S OUTPUT IS AT MAX AMPLITUDE WITHOUT CLIPPING OR SLEW LIMITING) IS APPLIED TO ONE AMPLIFIER AT A TIME. THE OUTPUTS OF THE OTHER THREE AMPLIFIERS ARE THEN MEASURED FOR CROSSTALK.

Figure 2a. Crosstalk Test Circuit

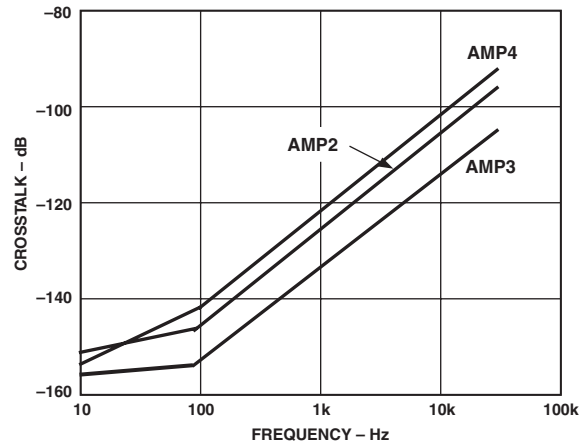


Figure 2b. Crosstalk vs. Frequency

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
AD704JN	0°C to 70°C	Plastic	N-14
AD704JR	0°C to 70°C	Small Outline (SOIC)	R-16
AD704JR-/REEL	0°C to 70°C		Tape and Reel
AD704KN*	0°C to 70°C	Plastic	N-14
AD704AN*	-40°C to +85°C	Plastic	N-14
AD704AR	-40°C to +85°C	Small Outline (SOIC)	R-16
AD704AR-/REEL	-40°C to +85°C		Tape and Reel
AD704SE/883B	-55°C to +125°C	Leadless Ceramic Chip Carrier	E-20A
AD704TQ/883B*	-55°C to +125°C	Cerdip	Q-14

Chips are also available.

*Not for new designs; obsolete April 2002.

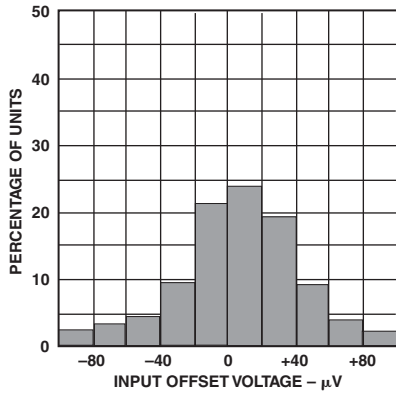
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD704 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

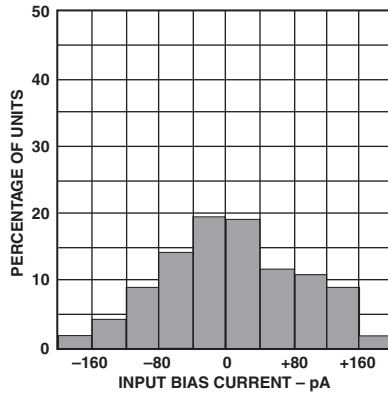


Typical Performance Characteristics—AD704

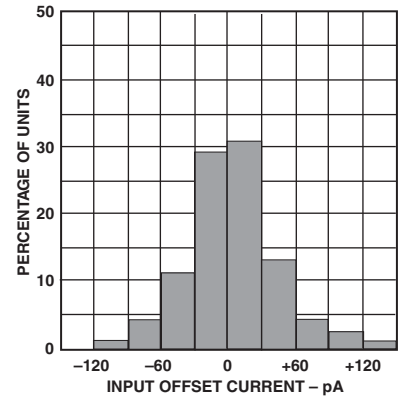
(@ 25°C, $V_S = \pm 15\text{ V}$ dc, unless otherwise noted.)



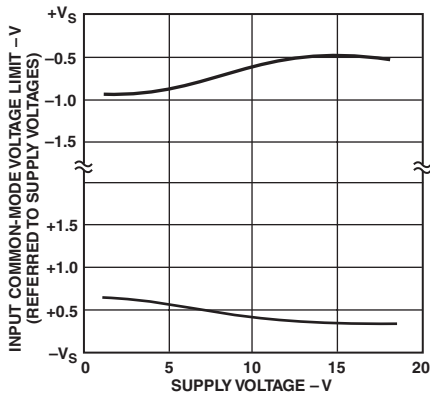
TPC 1. Typical Distribution of Input Offset Voltage



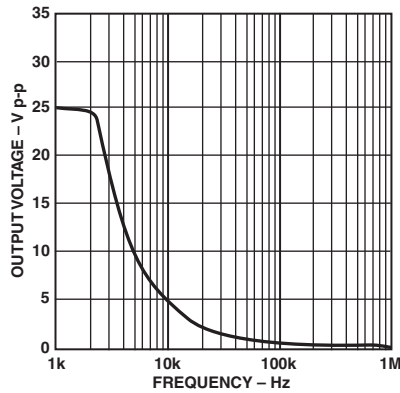
TPC 2. Typical Distribution of Input Bias Current



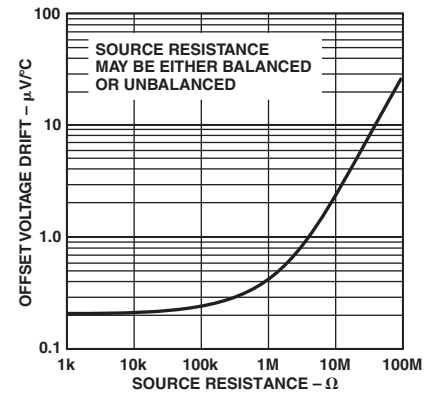
TPC 3. Typical Distribution of Input Offset Current



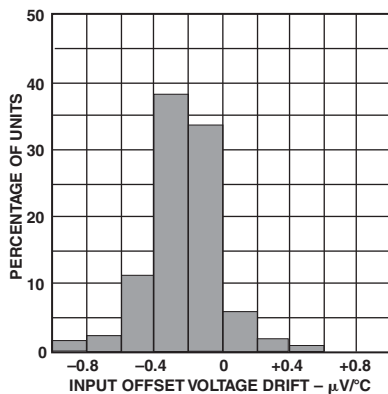
TPC 4. Input Common-Mode Voltage Range vs. Supply Voltage



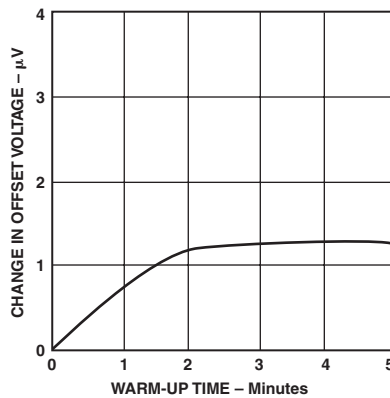
TPC 5. Large Signal Frequency Response



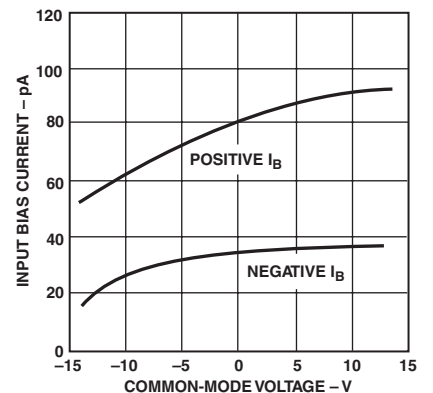
TPC 6. Offset Voltage Drift vs. Source Resistance



TPC 7. Typical Distribution of Offset Voltage Drift

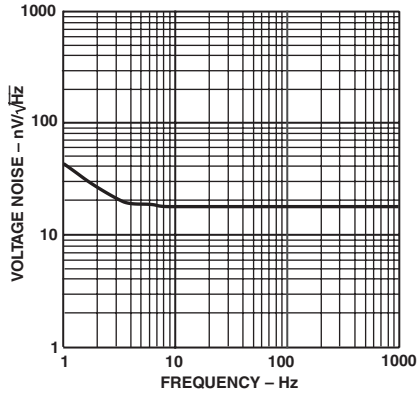


TPC 8. Change in Input Offset Voltage vs. Warm-Up Time

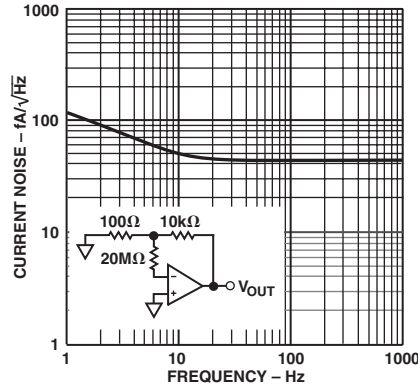


TPC 9. Input Bias Current vs. Common-Mode Voltage

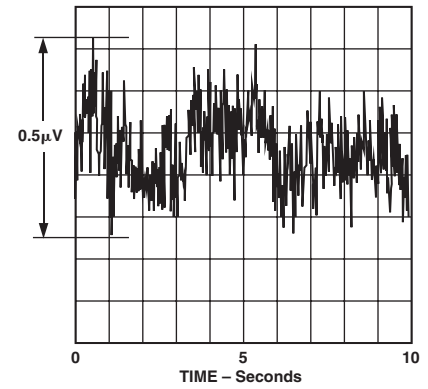
AD704



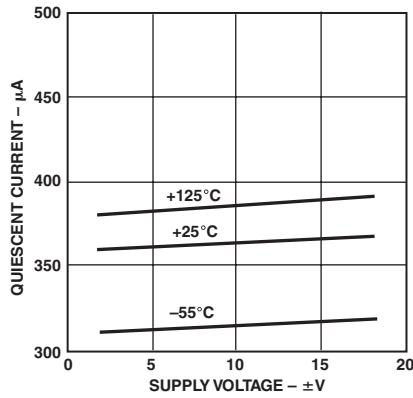
TPC 10. Input Noise Voltage Spectral Density



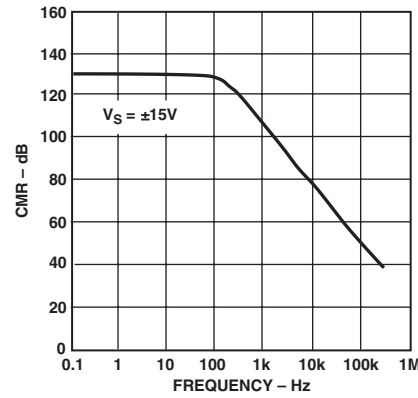
TPC 11. Input Noise Current Spectral Density



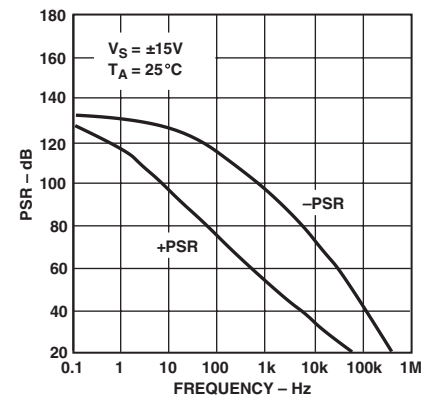
TPC 12. 0.1 Hz to 10 Hz Noise Voltage



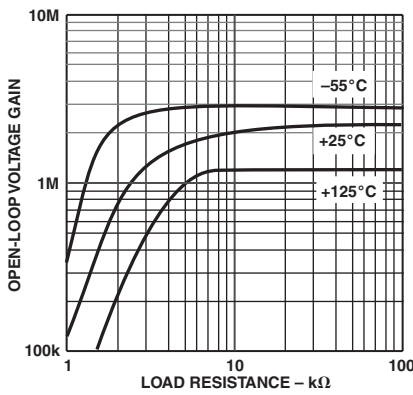
TPC 13. Quiescent Supply Current vs. Supply Voltage (per Amplifier)



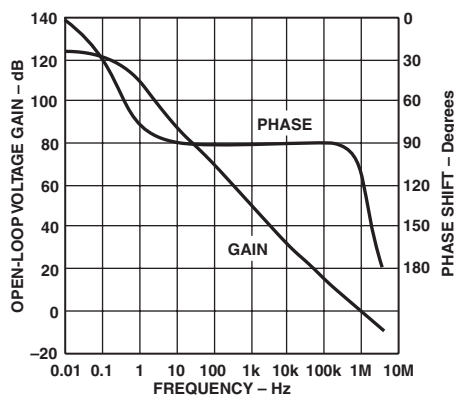
TPC 14. Common-Mode Rejection vs. Frequency



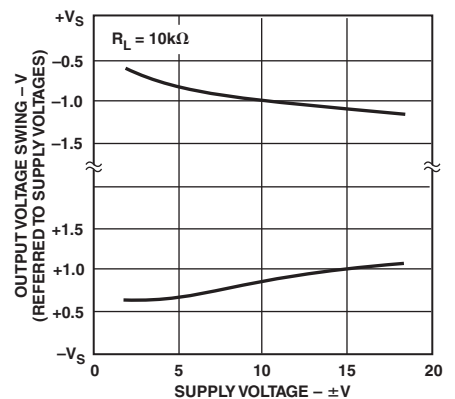
TPC 15. Power Supply Rejection vs. Frequency



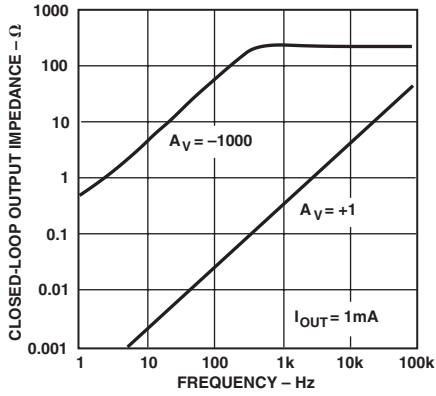
TPC 16. Open-Loop Gain vs. Load Resistance Over Temperature



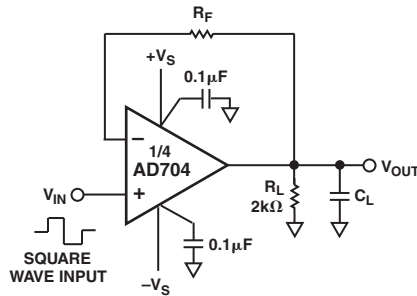
TPC 17. Open-Loop Gain and Phase vs. Frequency



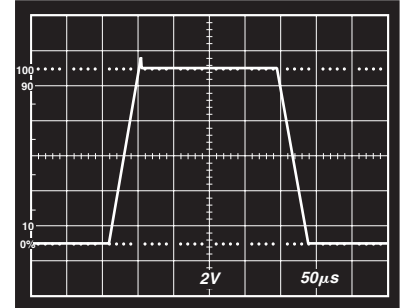
TPC 18. Output Voltage Swing vs. Supply Voltage



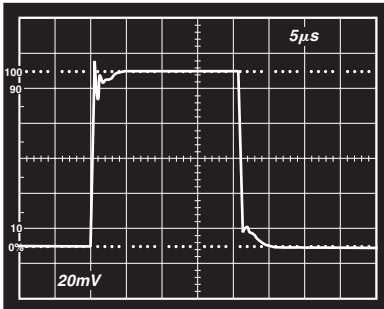
TPC 19. Closed-Loop Output Impedance vs. Frequency



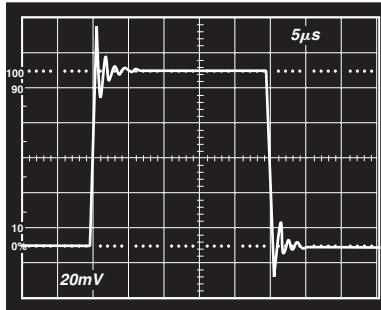
TPC 20a. Unity Gain Follower (For Large Signal Applications, Resistor R_F Limits the Current through the Input Protection Diodes)



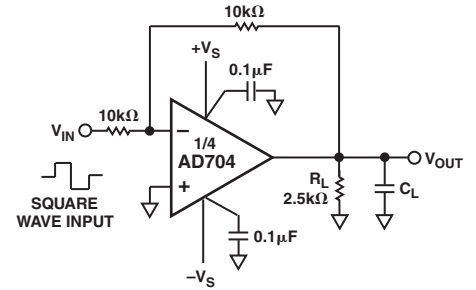
TPC 20b. Unity Gain Follower Large Signal Pulse Response $R_F = 10 \text{ k}\Omega$, $C_L = 1,000 \text{ pF}$



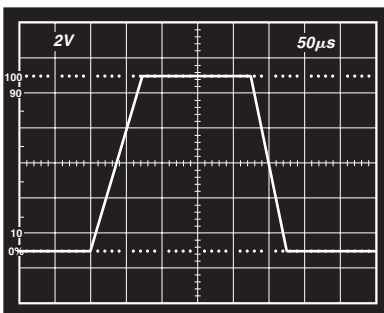
TPC 20c. Unity Gain Follower Small Signal Pulse Response $R_F = 0 \Omega$, $C_L = 100 \text{ pF}$



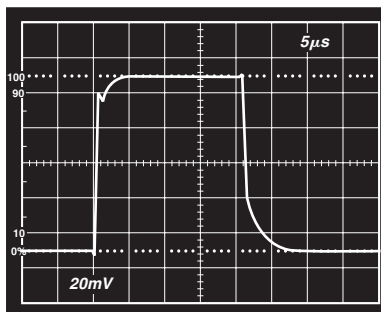
TPC 20d. Unity Gain Follower Small Signal Pulse Response $R_F = 0 \Omega$, $C_L = 1,000 \text{ pF}$



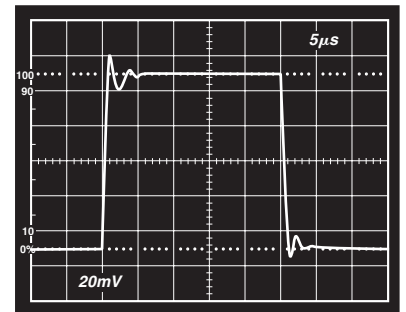
TPC 21a. Unity Gain Inverter Connection



TPC 21b. Unity Gain Inverter Large Signal Pulse Response, $C_L = 1,000 \text{ pF}$



TPC 21c. Unity Gain Inverter Small Signal Pulse Response, $C_L = 100 \text{ pF}$



TPC 21d. Unity Gain Inverter Small Signal Pulse Response, $C_L = 1,000 \text{ pF}$

AD704

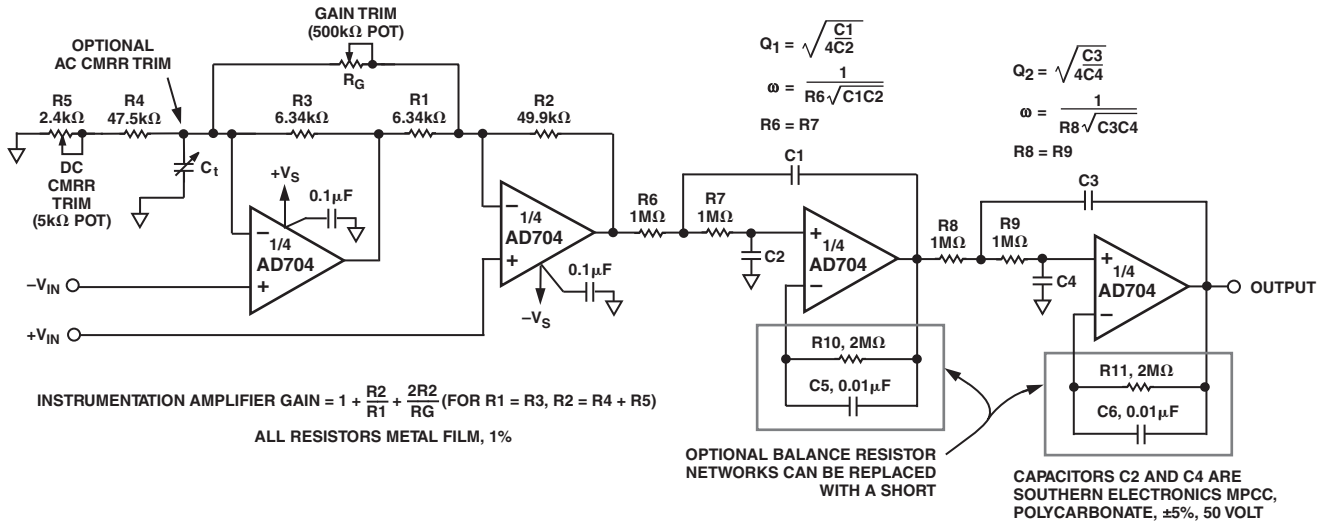


Figure 3. Gain of 10 Instrumentation Amplifier with Post Filtering

The instrumentation amplifier with post filtering (Figure 3) combines two applications which benefit greatly from the AD704. This circuit achieves low power and dc precision over temperature with a minimum of components.

The instrumentation amplifier circuit offers many performance benefits including BiFET level input bias currents, low input offset voltage drift and only 1.2 mA quiescent current. It will operate for gains $G \geq 2$, and at lower gains it will benefit from the fact that there is no output amplifier offset and noise contribution as encountered in a 3 op amp design. Good low frequency CMRR is achieved even without the optional ac CMRR trim (Figure 4). Table I provides resistance values for 3 common circuit gains. For other gains, use the following equations:

$$R_2 = R_4 + R_5 = 49.9 \text{ k}\Omega$$

$$R_1 = R_3 = \frac{49.9 \text{ k}\Omega}{0.9 G - 1}$$

$$\text{Max Value of } R_G = \frac{99.8 \text{ k}\Omega}{0.06 G}$$

$$C_t \approx \frac{1}{2 \pi (R_3) 5 \times 10^5}$$

Table I. Resistance Values for Various Gains

Circuit Gain (G)	R1 and R3	RG (Max Value of Trim Potentiometer)	Bandwidth (-3 dB), Hz
10	6.34 kΩ	166 kΩ	50k
100	526 Ω	16.6 kΩ	5k
1,000	56.2 Ω	1.66 kΩ	0.5k

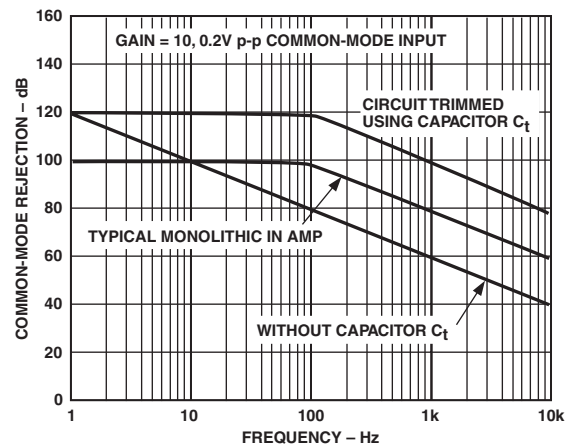


Figure 4. Common-Mode Rejection vs. Frequency with and without Capacitor C_t

The 1 Hz, 4-pole active filter offers dc precision with a minimum of components and cost. The low current noise, I_{OS} , and I_B allow the use of 1 M Ω resistors without sacrificing the 1 $\mu\text{V}/^\circ\text{C}$ drift of the AD704. This means lower capacitor values may be used, reducing cost and space. Furthermore, since the AD704's I_B is as low as its I_{OS} , over most of the MIL temperature range, most applications do not require the use of the normal balancing resistor (with its stability capacitor). Adding the optional balancing resistor enhances performance at high temperatures, as shown in Figure 5. Table II gives capacitor values for several common low pass responses.

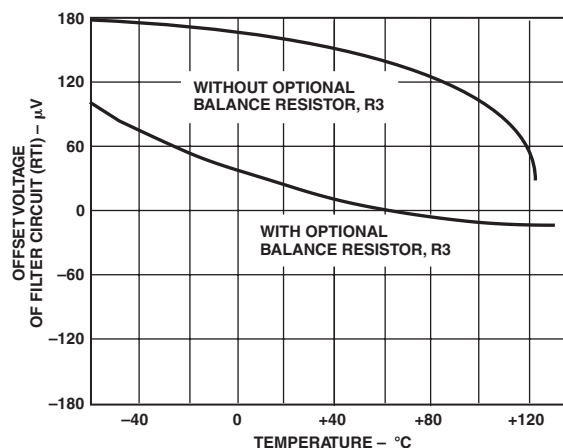


Figure 5. V_{OS} vs. Temperature Performance of the 1 Hz Filter Circuit

Table II. 1 Hz, 4-Pole Low-Pass Filter Recommended Component Values

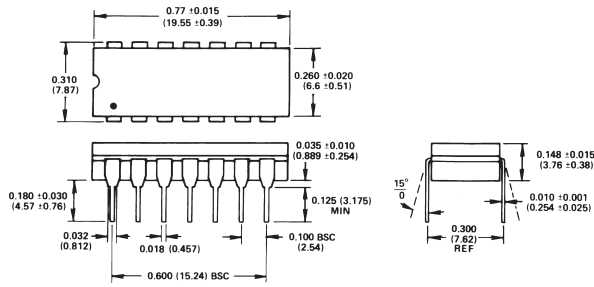
Desired Low Pass Response	Section 1 Frequency (Hz)	Q	Section 2 Frequency (Hz)	Q	C1 (μF)	C2 (μF)	C3 (μF)	C4 (μF)
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

Specified values are for a -3 dB point of 1.0 Hz. For other frequencies, simply scale capacitors C1 through C4 directly; i.e., for 3 Hz Bessel response, C1 = 0.0387 μF , C2 = 0.0357 μF , C3 = 0.0533 μF , C4 = 0.0205 μF .

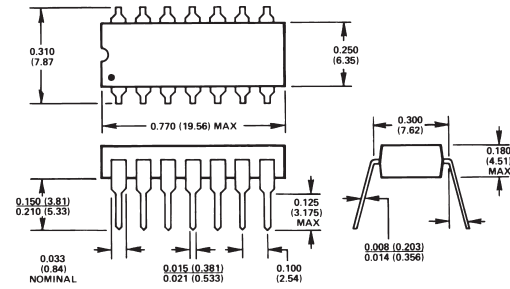
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

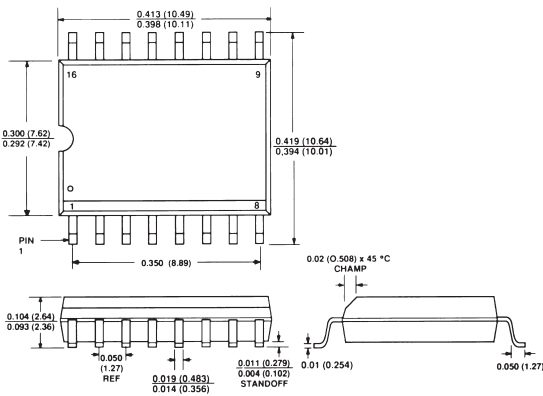
14-Lead Cerdip (Q) Package



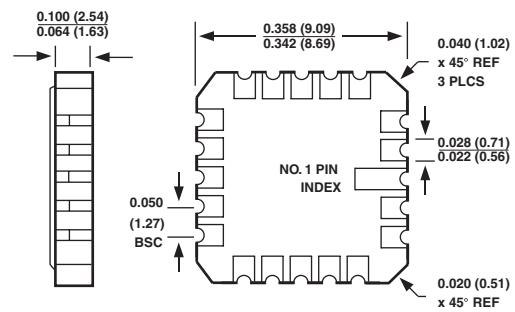
14-Lead Plastic DIP (N) Package



16-Lead Plastic SO (R) Package



20-Terminal LCC (E) Package



Revision History

Location	Page
11/01 Data Sheet changed from REV. B to REV. C.	
Edits to FEATURES	1
Edits to PRODUCT DESCRIPTION	1
Edits to ABSOLUTE MAXIMUM RATINGS	3
Deleted METALIZATION PHOTOGRAPH	3
Edits to ORDERING GUIDE	4

