



LC²MOS Quad SPST Switches

ADG441/ADG442/ADG444

FEATURES

- 44 V Supply Maximum Ratings
- V_{SS} to V_{DD} Analog Signal Range
- Low On Resistance (< 70 Ω)
- Low ΔR_{ON} (9 Ω max)
- Low R_{ON} Match (3 Ω max)
- Low Power Dissipation
- Fast Switching Times
 - t_{ON} < 110 ns
 - t_{OFF} < 60 ns
- Low Leakage Currents (3 nA max)
- Low Charge Injection (6 pC max)
- Break-Before-Make Switching Action
- Latch-Up Proof
- Plug-In Upgrade for
 - DG201A/ADG201A, DG202A/ADG202A,
 - DG211/ADG211A
- Plug in Replacement for DG441/DG442/DG444

APPLICATIONS

- Audio and Video Switching
- Automatic Test Equipment
- Precision Data Acquisition
- Battery Powered Systems
- Sample Hold Systems
- Communication Systems

GENERAL DESCRIPTION

The ADG441, ADG442 and ADG444 are monolithic CMOS devices comprising four independently selectable switches. They are designed on an enhanced LC²MOS process that provides low power dissipation yet gives high switching speed and low on resistance.

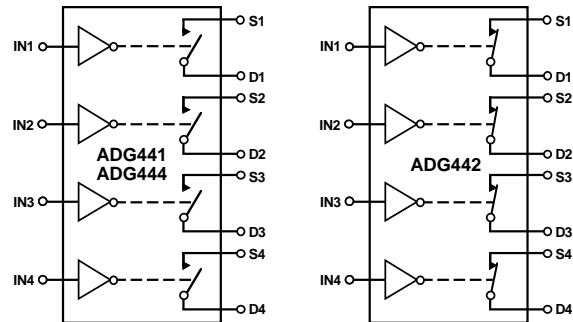
The on resistance profile is very flat over the full analog input range ensuring good linearity and low distortion when switching audio signals. High switching speed also makes the parts suitable for video signal switching. CMOS construction ensures ultralow power dissipation making the parts ideally suited for portable and battery powered instruments.

The ADG441, ADG442 and ADG444 contain four independent SPST switches. Each switch of the ADG441 and ADG444 turns on when a logic low is applied to the appropriate control input. The ADG442 switches are turned on with a logic high on the appropriate control input. The ADG441 and ADG444 switches differ in that the ADG444 requires a 5 V logic power supply which is applied to the V_L pin. The ADG441 and ADG442 do not have a V_L pin, the logic power supply being generated internally by an on-chip voltage generator.

REV. 0

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FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

Each switch conducts equally well in both directions when ON and has an input signal range that extends to the power supplies. In the OFF condition, signal levels up to the supplies are blocked. All switches exhibit break-before-make switching action for use in multiplexer applications. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

PRODUCT HIGHLIGHTS

1. Extended Signal Range
The ADG441/ADG442/ADG444 are fabricated on an enhanced LC²MOS, trench-isolated process, giving an increased signal range that extends to the supply rails.
2. Low Power Dissipation
3. Low R_{ON}
4. Trench Isolation Guards Against Latch Up
A dielectric trench separates the P and N channel transistors thereby preventing latch up even under severe overvoltage conditions.
5. Break-Before-Make Switching
This prevents channel shorting when the switches are configured as a multiplexer.
6. Single Supply Operation
For applications where the analog signal is unipolar, the ADG441/ADG442/ADG444 can be operated from a single rail power supply. The parts are fully specified with a single +12 V power supply.

ADG441/ADG442/ADG444—SPECIFICATIONS¹

Dual Supply ($V_{DD} = +15\text{ V} \pm 10\%$, $V_{SS} = -15\text{ V} \pm 10\%$, $V_L = +5\text{ V} \pm 10\%$ (ADG444), $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Version		T Version		Units	Test Conditions/Comments
	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
ANALOG SWITCH						
Analog Signal Range		V_{SS} to V_{DD}		V_{SS} to V_{DD}	V	
R_{ON}	40		40		Ω typ	$V_D = \pm 8.5\text{ V}$, $I_S = -10\text{ mA}$
	70		70	85	Ω max	$V_{DD} = +13.5\text{ V}$, $V_{SS} = -13.5\text{ V}$
ΔR_{ON}		4		4	Ω typ	$-8.5\text{ V} \leq V_D \leq +8.5\text{ V}$
		9		9	Ω max	
R_{ON} Match		1		1	Ω typ	$V_D = 0\text{ V}$, $I_S = -10\text{ mA}$
		3		3	Ω max	
LEAKAGE CURRENTS						
Source OFF Leakage I_S (OFF)	± 0.01		± 0.01		nA typ	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
	± 0.5	± 3	± 0.5	± 20	nA max	$V_D = \pm 15.5\text{ V}$, $V_S = \mp 15.5\text{ V}$;
Drain OFF Leakage I_D (OFF)	± 0.01		± 0.01		nA typ	Test Circuit 2
	± 0.5	± 3	± 0.5	± 20	nA max	$V_D = \pm 15.5\text{ V}$, $V_S = \mp 15.5\text{ V}$;
Channel ON Leakage I_D , I_S (ON)	± 0.08		± 0.08		nA typ	Test Circuit 2
	± 0.5	± 3	± 0.5	± 40	nA max	$V_S = V_D = \pm 15.5\text{ V}$;
						Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current					μA typ	$V_{IN} = V_{INL}$ or V_{INH}
I_{INL} or I_{INH}		± 0.00001		± 0.00001	μA max	
		± 0.5		± 0.5		
DYNAMIC CHARACTERISTICS²						
t_{ON}	85		85		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$;
	110	170	110	170	ns max	$V_S = \pm 10\text{ V}$; Test Circuit 4
t_{OFF}	45		45		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$;
	60	80	60	80	ns max	$V_S = \pm 10\text{ V}$; Test Circuit 4
t_{OPEN}	30		30		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$;
Charge Injection	1		1		pC typ	$V_S = 0\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$;
	6		6		pC max	$V_{DD} = +15\text{ V}$, $V_{SS} = -15\text{ V}$;
						Test Circuit 5
OFF Isolation	60		60		dB typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$;
						$f = 1\text{ MHz}$; Test Circuit 6
Channel-to-Channel Crosstalk	100		100		dB typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$;
						$f = 1\text{ MHz}$; Test Circuit 7
C_S (OFF)	4		4		pF typ	$f = 1\text{ MHz}$
C_D (OFF)	4		4		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	16		16		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS						
I_{DD}					μA max	$V_{DD} = +16.5\text{ V}$, $V_{SS} = -16.5\text{ V}$
ADG441/ADG442		80		80	μA typ	Digital Inputs = 0 V or 5 V
ADG444	0.001		0.001		μA max	
	1	2.5	1	2.5	μA max	
I_{SS}	0.0001		0.0001		μA typ	
	1	2.5	1	2.5	μA max	
I_L (ADG444 Only)	0.001		0.001		μA typ	$V_L = +5.5\text{ V}$
	1	2.5	1	2.5	μA max	

NOTES

¹Temperature ranges are as follows: B Versions: -40°C to +85°C; T Versions: -55°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG441/ADG442/ADG444

Single Supply ($V_{DD} = +12\text{ V} \pm 10\%$, $V_{SS} = 0\text{ V}$, $V_L = +5\text{ V} \pm 10\%$ (ADG444), $GND = 0\text{ V}$, unless otherwise noted)

Parameter	B Version -40°C to +85°C		T Version -55°C to +125°C		Units	Test Conditions/Comments
	+25°C		+25°C	+125°C		
ANALOG SWITCH						
Analog Signal Range		0 to V_{DD}		0 to V_{DD}	V	
R_{ON}	70		70		Ω typ	$V_D = +3\text{ V}$, $+8\text{ V}$, $I_S = -10\text{ mA}$;
	110	130	110	130	Ω max	$V_{DD} = +10.8\text{ V}$
ΔR_{ON}		4		4	Ω typ	$+3\text{ V} \leq V_D \leq +8\text{ V}$
		9		9	Ω max	
R_{ON} Match		1		1	Ω typ	$V_D = 6\text{ V}$, $I_S = -10\text{ mA}$
		3		3	Ω max	
LEAKAGE CURRENT						
Source OFF Leakage I_S (OFF)	± 0.01		± 0.01		nA typ	$V_{DD} = +13.2\text{ V}$
	± 0.5	± 3	± 0.5	± 20	nA max	$V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$;
Drain OFF Leakage I_D (OFF)	± 0.01		± 0.01		nA typ	$V_D = 12.2\text{ V}/1\text{ V}$, $V_S = 1\text{ V}/12.2\text{ V}$;
	± 0.5	± 3	± 0.5	± 20	nA max	Test Circuit 2
Channel ON Leakage I_D , I_S (ON)	± 0.08		± 0.08		nA typ	$V_S = V_D = 12.2\text{ V}/1\text{ V}$;
	± 0.5	± 3	± 0.5	± 40	nA max	Test Circuit 3
DIGITAL INPUTS						
Input High Voltage, V_{INH}		2.4		2.4	V min	
Input Low Voltage, V_{INL}		0.8		0.8	V max	
Input Current I_{INL} or I_{INH}		± 0.00001		± 0.00001	μA typ	$V_{IN} = V_{INL}$ or V_{INH}
		± 0.5		± 0.5	μA max	
DYNAMIC CHARACTERISTICS²						
t_{ON}	105		105		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$;
	150	220	150	220	ns max	$V_S = +8\text{ V}$; Test Circuit 4
t_{OFF}	40		40		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$;
	60	100	60	100	ns max	$V_S = +8\text{ V}$; Test Circuit 4
t_{OPEN}	50		50		ns typ	$R_L = 1\text{ k}\Omega$, $C_L = 35\text{ pF}$;
Charge Injection	2		2		pC typ	$V_S = 6\text{ V}$, $R_S = 0\text{ }\Omega$, $C_L = 1\text{ nF}$;
	6		6		pC max	$V_{DD} = +12\text{ V}$, $V_{SS} = 0\text{ V}$;
OFF Isolation	60		60		dB typ	Test Circuit 5
Channel-to-Channel Crosstalk	100		100		dB typ	$R_L = 50\text{ }\Omega$, $C_L = 5\text{ pF}$, $f = 1\text{ MHz}$;
						Test Circuit 6
C_S (OFF)	7		7		pF typ	$f = 1\text{ MHz}$
C_D (OFF)	10		10		pF typ	$f = 1\text{ MHz}$
C_D , C_S (ON)	16		16		pF typ	$f = 1\text{ MHz}$
POWER REQUIREMENTS						
I_{DD}						$V_{DD} = +13.2\text{ V}$
ADG441/ADG442		80		80	μA max	Digital Inputs = 0 V or 5 V
ADG444	0.001		0.001		μA typ	
	1	2.5	1	2.5	μA max	
I_L (ADG444 Only)	0.001		0.001		μA typ	$V_L = +5.5\text{ V}$
	1	2.5	1	2.5	μA max	

NOTES

¹Temperature ranges are as follows: B Versions: -40°C to +85°C; T Versions: -55°C to +125°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ORDERING GUIDE

Table I. Truth Table

ADG441/ADG444 IN	ADG442 IN	Switch Condition
0	1	ON
1	0	OFF

Model ¹	Temperature Range	Package Option ²
ADG441BN	-40°C to +85°C	N-16
ADG441BR	-40°C to +85°C	R-16A
ADG441TQ	-55°C to +125°C	Q-16
ADG442BN	-40°C to +85°C	N-16
ADG442BR	-40°C to +85°C	R-16A
ADG444BN	-40°C to +85°C	N-16
ADG444BR	-40°C to +85°C	R-16A

NOTES

¹To order MIL-STD-883, Class B processed parts, add /883B to T grade part numbers.

²N = Plastic DIP, R = 0.15" Small Outline IC (SOIC), Q = Cerdip.

ADG441/ADG442/ADG444

ABSOLUTE MAXIMUM RATINGS¹

(T_A = +25°C unless otherwise noted)

V _{DD} to V _{SS}	+44 V
V _{DD} to GND	-0.3 V to +25 V
V _{SS} to GND	+0.3 V to -25 V
V _L to GND	-0.3 V to V _{DD} + 0.3 V
Analog, Digital Inputs ²	V _{SS} - 2 V to V _{DD} + 2 V or 30 mA, Whichever Occurs First
Continuous Current, S or D	30 mA
Peak Current, S or D	100 mA
(Pulsed at 1 ms, 10% Duty Cycle Max)	
Operating Temperature Range	
Industrial (B Version)	-40°C to +85°C
Extended (T Version)	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Cerdip Package, Power Dissipation	900 mW
θ _{JA} , Thermal Impedance	76°C/W
Lead Temperature, Soldering (10 sec)	+300°C
Plastic Package, Power Dissipation	470 mW
θ _{JA} , Thermal Impedance	177°C/W
Lead Temperature, Soldering (10 sec)	+260°C
SOIC Package, Power Dissipation	600 mW
θ _{JA} , Thermal Impedance	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	+215°C
Infrared (15 sec)	+220°C

NOTES

¹Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

TERMINOLOGY

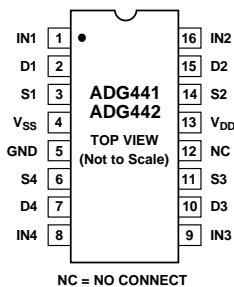
V _{DD}	Most Positive Power Supply Potential.
V _{SS}	Most Negative Power Supply Potential in dual supplies. In single supply applications, it may be connected to ground.
V _L	Logic Power Supply (+5 V).
GND	Ground (0 V) Reference.
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input.
R _{ON}	Ohmic resistance between D and S.
R _{ON Match}	Difference between the R _{ON} of any two channels.
I _S (OFF)	Source leakage current with the switch "OFF."
I _D (OFF)	Drain leakage current with the switch "OFF."
I _D , I _S (ON)	Channel leakage current with the switch "ON."
V _D (V _S)	Analog voltage on terminals D, S.
C _S (OFF)	"OFF" Switch Source Capacitance.
C _D (OFF)	"OFF" Switch Drain Capacitance.
C _D , C _S (ON)	"ON" Switch Capacitance.
t _{ON}	Delay between applying the digital control input and the output switching on.
t _{OFF}	Delay between applying the digital control input and the output switching off.
t _{OPEN}	Break-Before-Make Delay when switches are configured as a multiplexer.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.

CAUTION

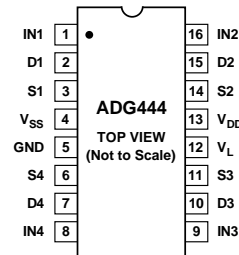
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although these devices feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADG441/ADG442 PIN CONFIGURATION (DIP/SOIC)



ADG444 PIN CONFIGURATION (DIP/SOIC)



ADG441/ADG442/ADG444

TRENCH ISOLATION

In the ADG441, ADG442 and ADG444, an insulating oxide layer (trench) is placed between the NMOS and the PMOS transistors of each CMOS switch. Parasitic junctions, which occur between the transistors in junction isolated switches, are eliminated, the result being a completely latch-up proof switch.

In junction isolation, the N and P wells of the PMOS and NMOS transistors form a diode that is reverse-biased under normal operation. However, during overvoltage conditions, this diode becomes forward biased. A silicon-controlled rectifier (SCR) type circuit is formed by the two transistors causing a significant amplification of the current which, in turn, leads to latch up. With trench isolation, this diode is removed, the result being a latch-up proof switch.

Trench isolation also leads to lower leakage currents. The ADG441, ADG442 and ADG444 have a leakage current of 0.5 nA as compared with a leakage current of several nanoamperes in non-trench isolated switches. Leakage current is an important parameter in sample-and-hold circuits, this current being responsible for the discharge of the holding capacitor with time causing droop. The ADG441/ADG442/ADG444's low leakage current, along with its fast switching speeds, make it suitable for fast and accurate sample-and-hold circuits.

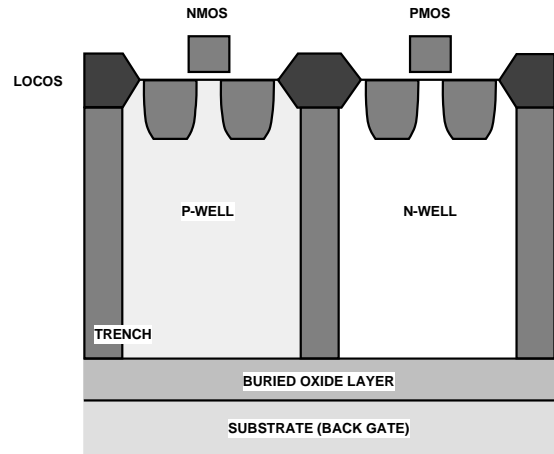


Figure 1. Trench Isolation

Typical Performance Characteristics

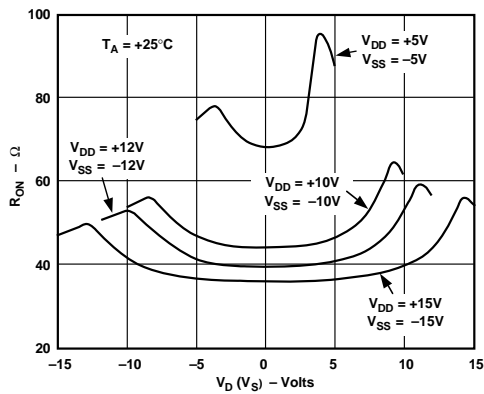


Figure 2. R_{ON} as a Function of V_D (V_S): Dual Supply

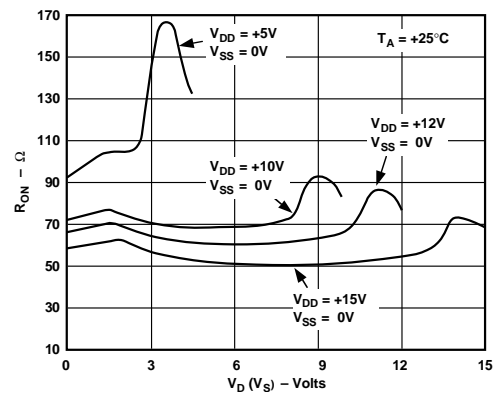


Figure 3. R_{ON} as a Function of V_D (V_S): Single Supply

ADG441/ADG442/ADG444

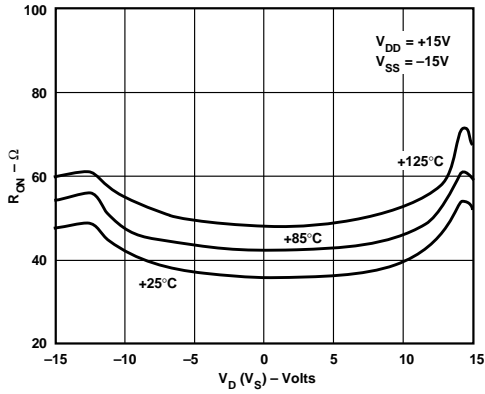


Figure 4. R_{ON} as a Function of V_D (V_S) for Different Temperatures

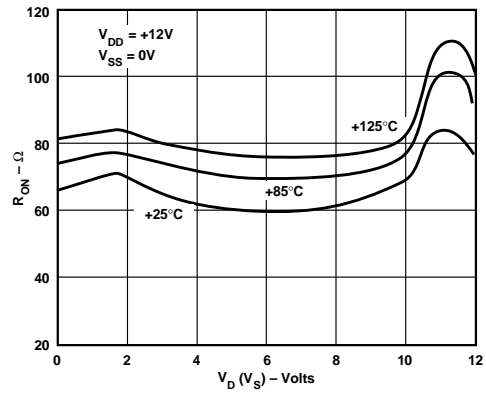


Figure 7. R_{ON} as a Function of V_D (V_S) for Different Temperatures

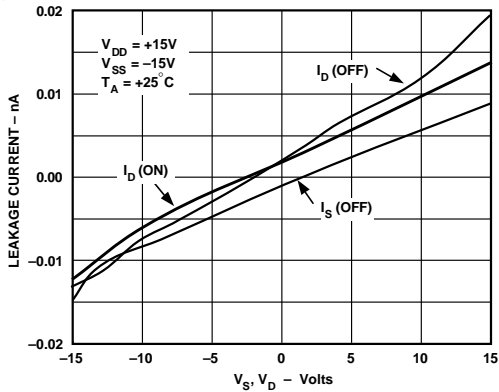


Figure 5. Leakage Currents as a Function of V_S (V_D)

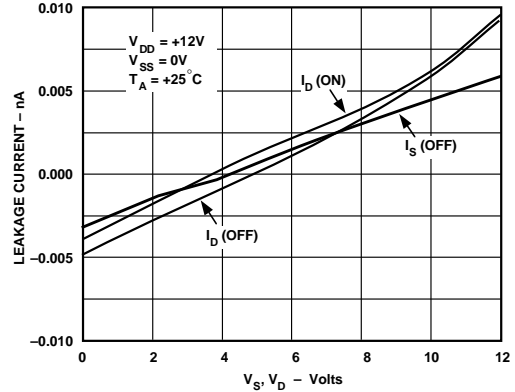


Figure 8. Leakage Currents as a Function of V_S (V_D)

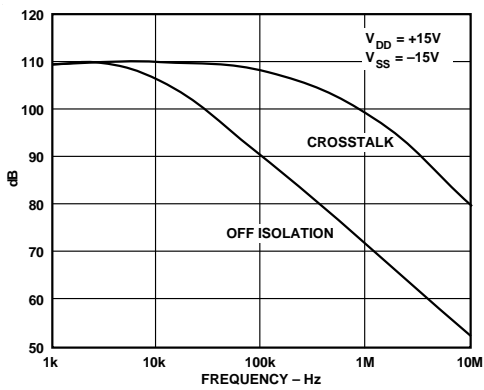


Figure 6. Crosstalk and Off Isolation vs. Frequency

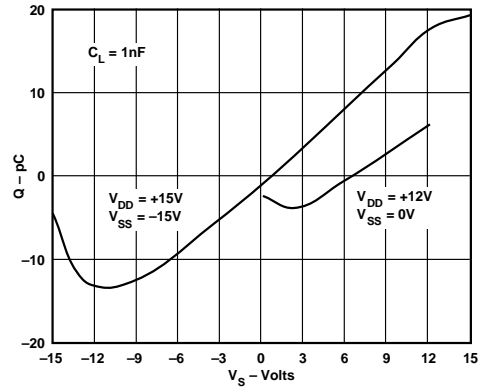


Figure 9. Charge Injection vs. Source Voltage

ADG441/ADG442/ADG444

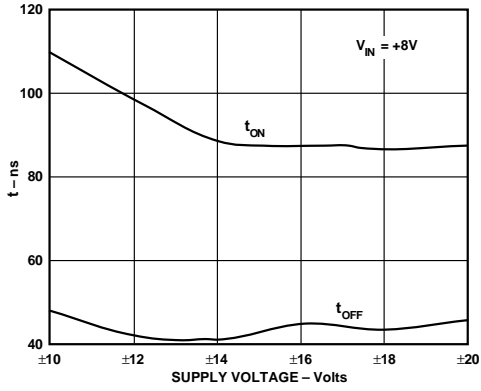


Figure 10. Switching Time vs. Bipolar Supply

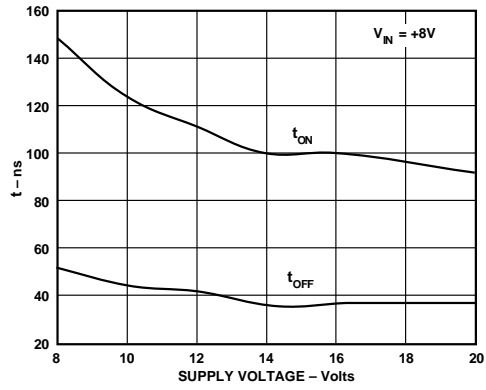
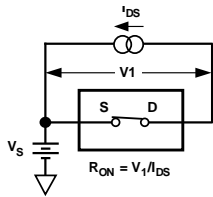
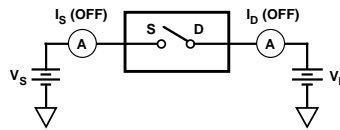


Figure 11. Switching Time vs. Single Supply

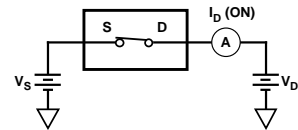
Test Circuits



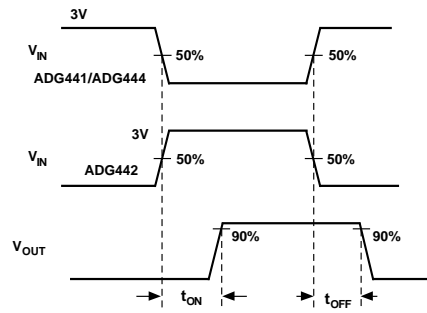
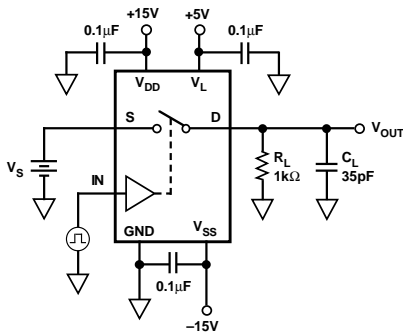
Test Circuit 1. On Resistance



Test Circuit 2. Off Leakage

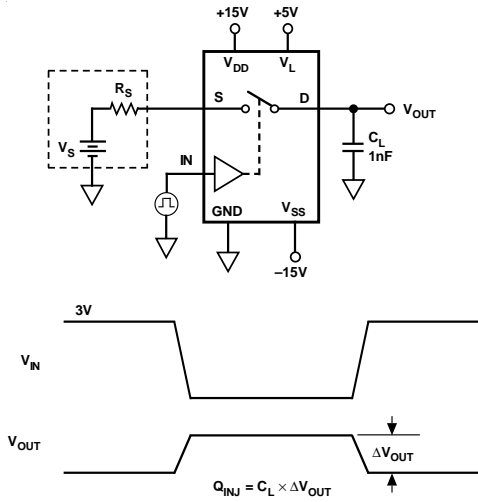


Test Circuit 3. On Leakage

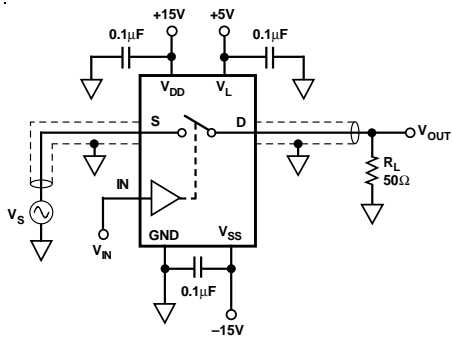


Test Circuit 4. Switching Times

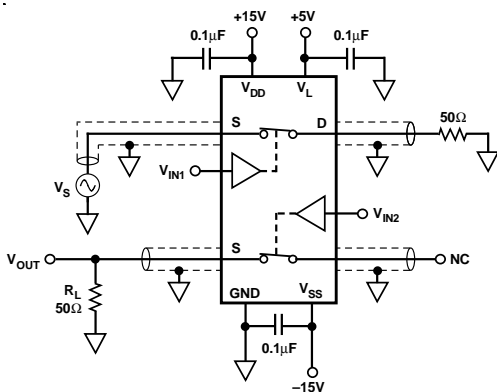
ADG441/ADG442/ADG444



Test Circuit 5. Charge Injection



Test Circuit 6. Off Isolation

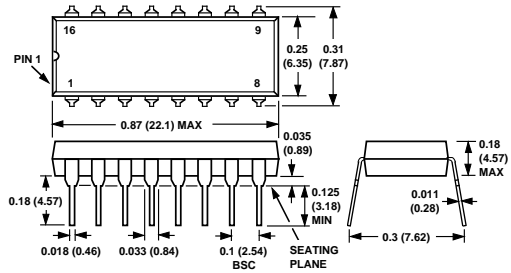


CHANNEL-TO-CHANNEL CROSSTALK = $20 \times \text{LOG} |V_S/V_{OUT}|$
Test Circuit 7. Channel-to-Channel Crosstalk

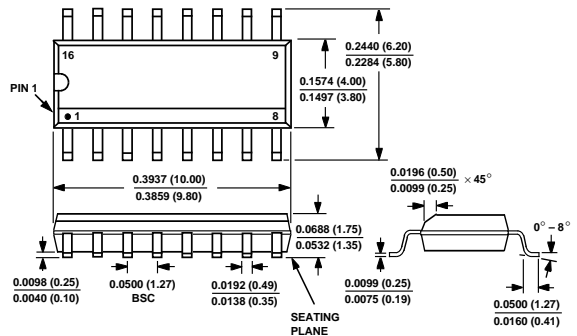
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

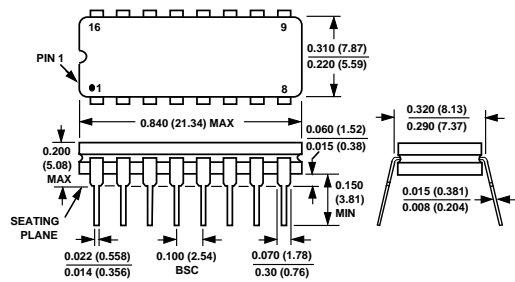
Plastic DIP (N-16)



Small Outline IC (R-16A)



Cerdip (Q-16)



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