# Octal, RS-232/RS-423 Line Receiver

# ADM5180

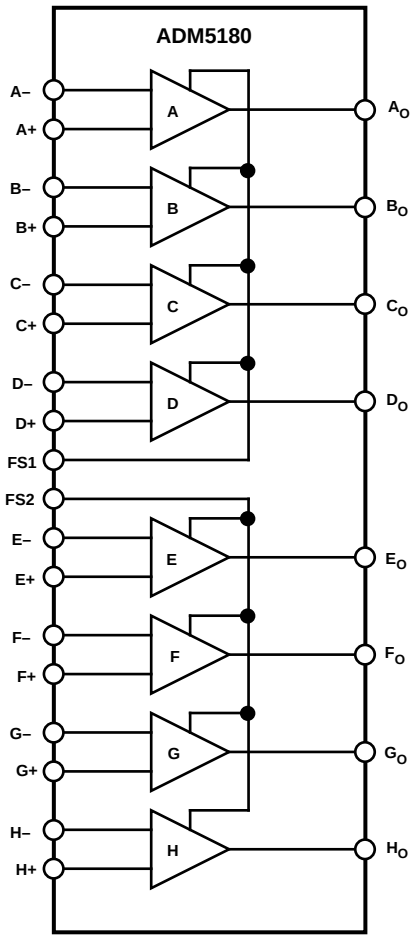
**FEATURES**

**Eight Differential Line Receivers in One Package**
**Meets EIA Standard EIA-232E, 423A, 422A and CCITT V.10, V.11, V.28**
**Single +5 V Supply**
**Differential Inputs Withstand ±25 V**
**Internal Hysteresis**
**Low Power CMOS –3.5 mA Supply Current**
**TTL/CMOS Compatible Outputs**
**Available in 28-Pin DIP and PLCC Packages**
**Low Power Replacement for UC5180C/NE5180**

**APPLICATIONS**

**High Speed Communication**
**Computer I-O Ports**
**Peripherals**
**High Speed Modems**
**Printers**
**Logic Level Translation**

**FUNCTIONAL BLOCK DIAGRAM**




**Truth Table**

| Differential Input (+) - (–) | Failsafe Input FS1, FS2 | Receiver Logic Output |
|---|---|---|
| >200 mV | X | H |
| <–200 mV | X | L |
| O/C | L | L |
| S/C | L | L |
| O/C | H | H |
| S/C | H | H |

## GENERAL DESCRIPTION

The ADM5180 is an octal differential line receiver suitable for a wide range of digital communication systems with data rates up to 200 kB/s. Input signals conforming to EIA Standards 232-E, 422A and CCITT V.10, V.11, V.28, X.26, and X.27 are accepted and translated into TTL /CMOS output signal levels.

The ADM5180 is a superior upgrade for the UC5180C and the NE5180. It is fabricated on an advanced BiCMOS process, allowing high speed bipolar circuitry to be combined with low power CMOS. This minimizes the power consumption to less than 25 mW.

A failsafe function ensures a known output state under a variety of input fault conditions as defined in RS-422A and RS-423A. The failsafe function is controlled by FS1 and FS2. Each controls four receivers. With FS = Low and a fault condition the output is forced low while if FS = High, the output is forced high.

The device is available in both 28-pin DIP and 28-lead PLCC packages.

REV. 0



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# ADM5180–SPECIFICATIONS ($V_{DD}$ = +5 V ± 5%, Input Common-Mode Range = ±7 V. All Specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted.)

| Parameter | Min | Typ | Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|
| POWER REQUIREMENTS | | | | | |
| $V_{DD}$ | 4.75 | | 5.25 | V | |
| $I_{DD}$ | | 3.5 | 5 | mA | |
| INPUTS | | | | | |
| Input Resistance, $R_{IN}$ | 3 | | 7 | kΩ | 3 V ≤ \|$V_{IN}$\| ≤ 25 V |
| Differential Input High Threshold, $V_{TH}$ | 50 | | 200 | mV | $R_S$ = 0 Ω, $V_{OUT}$ = 2.7 V, $I_{OUT}$ = –440 µA, See Figure 1 |
| | | | 400 | mV | $R_S$ = 500 Ω, $V_{OUT}$ = 2.7 V, $I_{OUT}$ = –440 µA, See Figure 1 |
| Differential Input Low Threshold, $V_{TL}$ | –200 | | –50 | mV | $R_S$ = 0 Ω, $V_{OUT}$ = 0.45 V, $I_{OUT}$ = 8 mA, See Figure 1 |
| | –400 | | | mV | $R_S$ = 500 Ω, $V_{OUT}$ = 0.45 V, $I_{OUT}$ = 8 mA, See Figure 1 |
| Hysteresis, $V_H$ | 50 | | 140 | mV | FS1, FS2 = 0 V or $V_{DD}$, See Figure 1 |
| Open Circuit Input Voltage, $V_{IOC}$ | | | 60 | mV | |
| Input Capacitance | | | 20 | pF | |
| Input Current, $I_{IN}$ | | | 3.25 | mA | $V_{IN}$ = +10 V |
| | –3.25 | | | mA | $V_{IN}$ = –10 V |
| OUTPUTS | | | | | |
| High Level Output Voltage,$V_{OH}$ | 2.7 | | | V | $V_{ID}$ = 1.0 V, $I_{OUT}$ = –440 µA |
| Low Level Output Voltage ,$V_{OL}$ | | | 0.4 | V | $V_{ID}$ = –1.0 V, $I_{OUT}$ = 4 mA |
| | | | 0.45 | V | $V_{ID}$ = –1.0 V, $I_{OUT}$ = 8 mA, $T_A$ = 0°C to +70°C |
| Short Circuit O/P Current, $I_{OS}$ | | | 100 | mA | Note 1 |
| FAILSAFE FUNCTION | | | | | |
| Failsafe Output Voltage, $V_{OFS}$ | | | | | Inputs Open or Shorted Together or One Input Open and One Grounded |
| | | | 0.40 | V | 0 ≤ $I_{OUT}$ ≤ 4 mA; FS1, FS2 = 0 V |
| | | | 0.45 | V | 0 ≤ $I_{OUT}$ ≤ 8 mA, $T_A$ = 0°C to +70°C; FS1, FS2 = 0 V |
| | 2.7 | | | V | 0 ≥ $I_{OUT}$ ≥ –400 µA; FS1, FS2 = $V_{DD}$ |
| FS1, FS2 Input Current | –10 | | +10 | µA | |

NOTE
[1]Only one output may be shorted at any time.

Specifications subject to change without notice.

# TIMING CHARACTERISTICS ($V_{DD}$ = +5 V ± 5%. All Specifications $T_{MIN}$ to $T_{MAX}$ unless otherwise noted)

| Parameter | Min | Typ | Max | Units | Test Conditions/Comments |
|---|---|---|---|---|---|
| Propagation Delay–Low to High | | | 550 | ns | $C_L$ = 50 pF, $V_{IN}$ = ±500 mV |
| Propagation Delay–High to Low | | | 550 | ns | $C_L$ = 50 pF, $V_{IN}$ = ±500 mV |
| Acceptable Input Frequency | | | 0.1 | MHz | Unused Input Grounded, $V_{IN}$ = ±200 mV |
| Rejectable Input Frequency | 5.5 | | | MHz | Unused Input Grounded, $V_{IN}$ = ±500 mW |

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS**[1]

($T_A$ = 25°C unless otherwise noted)

$V_{DD}$ ..... +7 V
Common-Mode Input Voltage ..... +15 V
Differential Input Voltage ..... +25 V
Failsafe Voltage ..... –0.3 V to $V_{CC}$
Output Short Circuit Duration ..... Continuous[2]
Power Dissipation Plastic DIP ..... 1250 mW
(Derate at 12.5 mW/°C Above +50°C)
$\theta_{JA}$, Thermal Impedance ..... 75°C/W
Power Dissipation PLCC ..... 1000 mW
(Derate at 12.5 mW/°C Above +50°C)
$\theta_{JA}$, Thermal Impedance ..... +80°C/W
Operating Temperature Range
Commercial ( J Version) ..... 0°C to +70°C
Industrial (A Version) ..... –40°C to +80°C
Lead Temperature (Soldering 10 sec) ..... +300°C
Vapour Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

NOTES
[1]This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.
[2]Only one output should be shorted at any time.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM5180 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

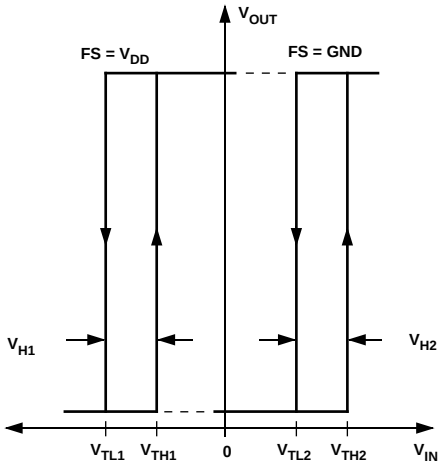




*Figure 1. $V_{TL}$, $V_{TH}$, $V_H$ Definition*

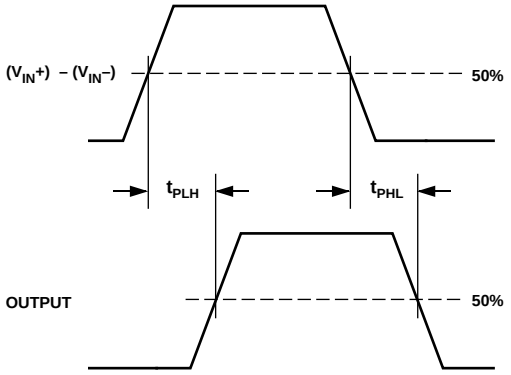



*Figure 3. Timing Waveform*

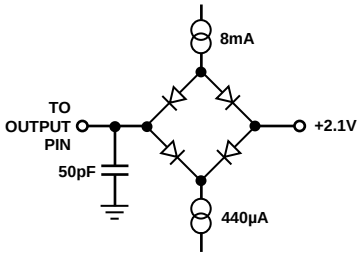


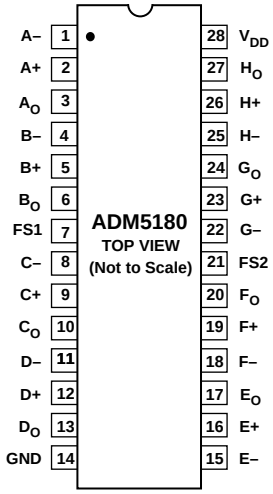

*Figure 2. Timing Test Load*

**ORDERING GUIDE**

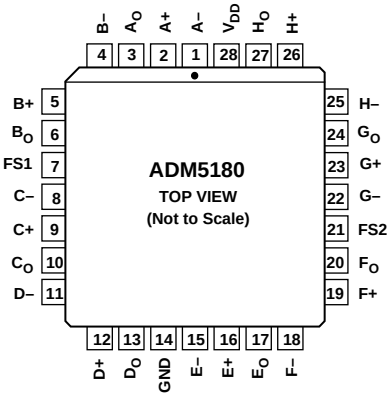
| Model | Temperature Range | Package Option |
|---|---|---|
| ADM5180JN | 0°C to +70°C | N-28 |
| ADM5180AN | –40°C to +85°C | N-28 |
| ADM5180JP | 0°C to +70°C | P-28A |
| ADM5180AP | –40°C to +85°C | P-28A |

## PIN CONFIGURATIONS

### DIP




### PLCC




## PIN DESCRIPTION

| Mnemonic | Function |
|---|---|
| $V_{DD}$ | Power Supply Input, 5 V ± 5%. |
| GND | Ground Pin. Must be connected to 0 V. |
| A+ . . . H+ | Noninverting Input to Differential Receivers A to H. |
| A– . . . H– | Inverting Input to Differential Receivers A to H. |
| $A_O$ . . . $H_O$ | Receiver Outputs A to H. |
| FS1, FS2 | A through D and FS2 controls receivers E through H.<br>Failsafe Control Inputs. FS1 controls receivers A through D and FS2 control Receiver E through H. |

## APPLICATIONS INFORMATION

### FAILSAFE OPERATION

The ADM5180 provides a failsafe operating mode to guard against input fault conditions as defined in RS-422A and RS-423A standards. The fault conditions are (1) Driver in power-off condition, (2) Receiver not interconnected with Driver, (3) Open-circuited interconnecting cable, and (4) Short-circuited interconnecting cable. If any of these four fault conditions occurs at the inputs of a receiver, then the output of that receiver is driven to a known logic level. The failsafe level is programmed using the failsafe (FS) input. There are two failsafe inputs, FS1 and FS2 which each control four receivers. FSI controls receivers A . . . D and FS2 controls receivers E . . . H. A connection to $V_{DD}$ on the failsafe input sets the output high under fault conditions while a connection to GND sets the output low.

| FS1, FS2 | Output During Fault Condition |
|---|---|
| $V_{DD}$ | High |
| GND | Low |

### Input Filtering

The ADM5180 contains internal low pass filtering for additional noise rejection. Frequencies above the passband will be rejected. For the specified input (5.5 MHz at ±500 mV) the input stage attenuates the signal such that the threshold levels are not reached and therefore no change of state occurs on the output. The filtering is a function of both amplitude and and frequency. As the signal amplitude decreases then the rejected frequency will decrease.

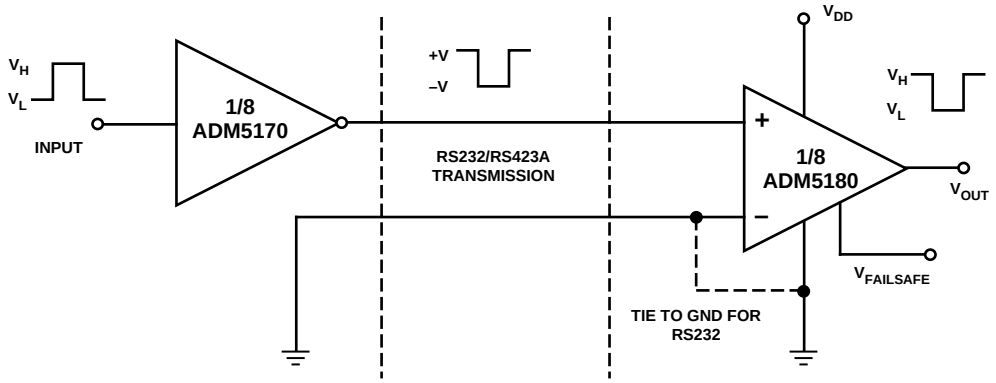



*Figure 4. EIA-232/V.28 Data Transmission*

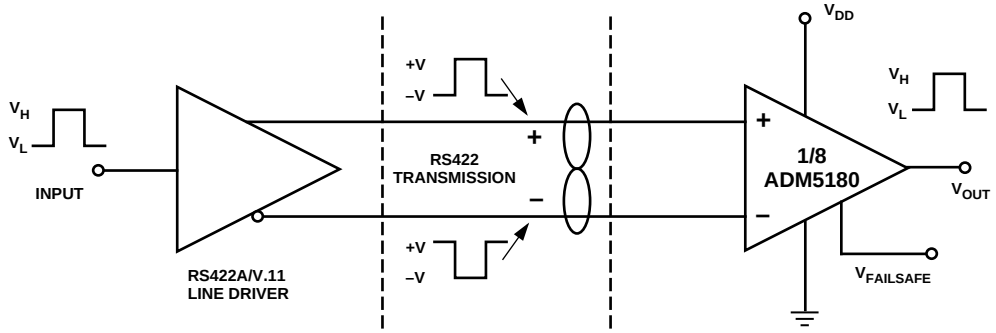



*Figure 5. RS-422A/V.11 Data Transmission*

# Typical Performance Characteristics

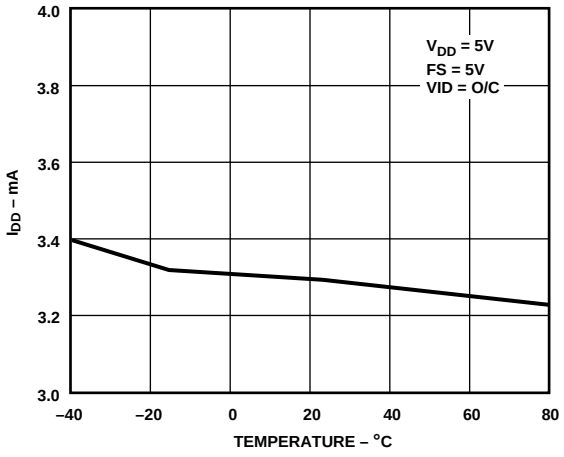



*Figure 6. Supply Current vs. Temperature*

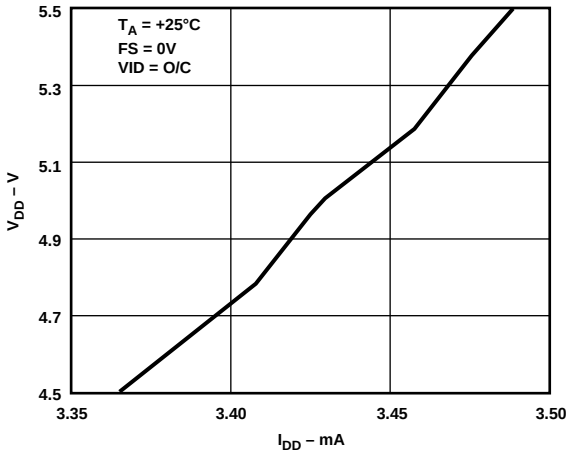



*Figure 7. Supply Current vs. Supply Voltage*

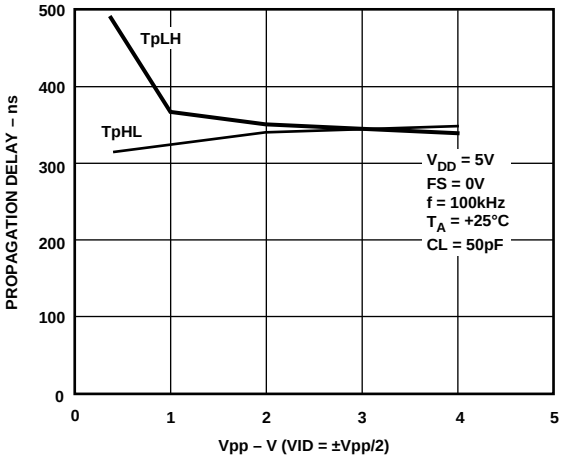



*Figure 8. Propagation Delay vs. Amplitude*

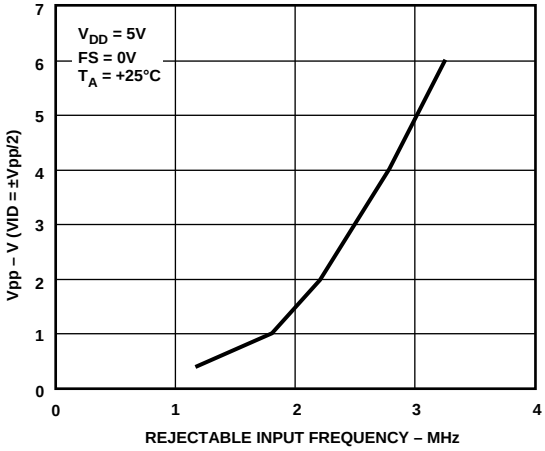



*Figure 10. Rejectable Input Frequency vs. Amplitude*

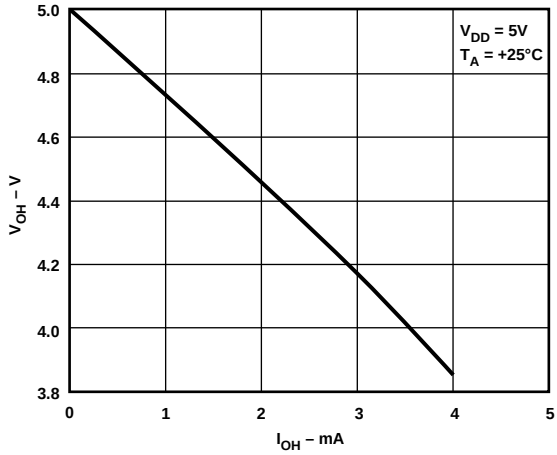



*Figure 9. High Level Output Voltage vs. Output Source Current*

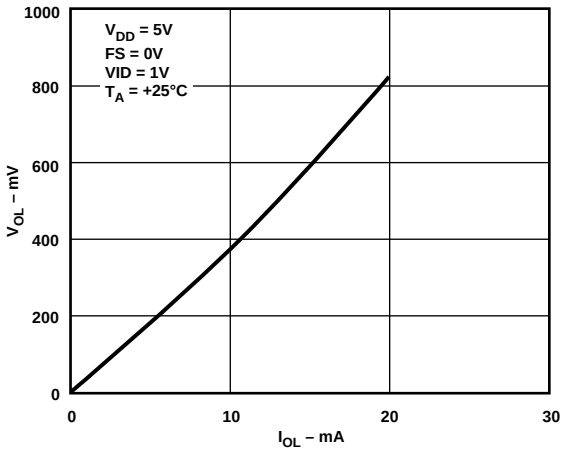


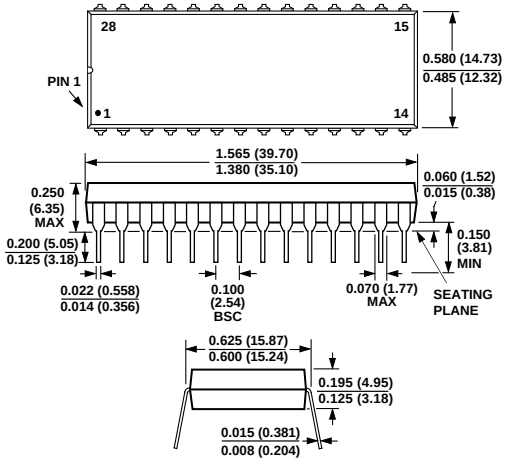

*Figure 11. Low Level Output Voltage vs. Output Sink Current*

C1854–7.5–10/93

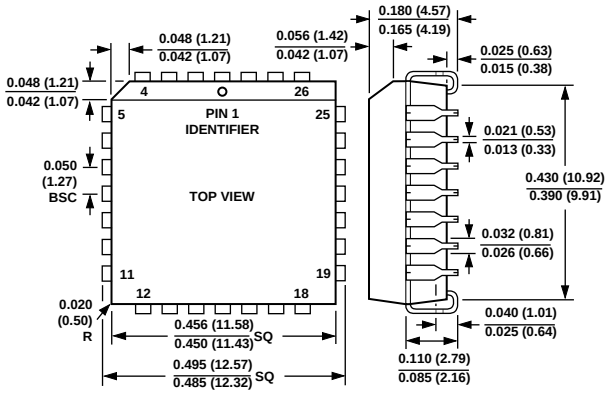
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**28-Lead Plastic DIP**
**(N Suffix)**




**28-Lead Plastic Leaded Chip Carrier (PLCC)**
**(P Suffix)**

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