ANALOG DEVICES

192-Bit, 360 MHz True-Color Video DAC with Onboard PLL

ADV7129

FEATURES

192-Bit Pixel Port Allows 2048 × 2048 × 24 Screen Resolution
360 MHz, 24-Bit True-Color Operation
Triple 8-Bit D/A Converters
8:1 Multiplexing
Onboard PLL
RS-343A/RS-170 Compatible Analog Outputs
TTL Compatible Digital Inputs
Internal Voltage Reference
Standard 8-Bit MPU I/O Interface
DAC-DAC Matching: Typ 2%, Adjustable to 0.02%
+5 V CMOS Monolithic Construction
304-Pin PQFP Package

APPLICATIONS

Ultrahigh Resolution Color Graphics
Image Processing
Drives 24-Bit Color 2K × 2K Monitors

GENERAL DESCRIPTION

The ADV7129 is a complete analog output, video DAC on a single CMOS (ADV®) monolithic chip. The part is specifically designed for use in the highest resolution graphics and imaging systems. The ultimate level of integration, comprised of 360 MHz triple 8-bit DACs, a programmable pixel port, an internal voltage reference and an onboard PLL, makes the ADV7129 the only choice for the very highest level of performance and functionality.

The device consists of three high speed, 8-bit, video D/A converters (RGB). An onboard phase locked loop clock generator is provided to provide high speed operation without requiring high speed external crystal or clock circuitry.

The part is fully controlled through the MPU port by the onboard command registers. This MPU port may be updated at any time without causing sparkle effects on the screen.

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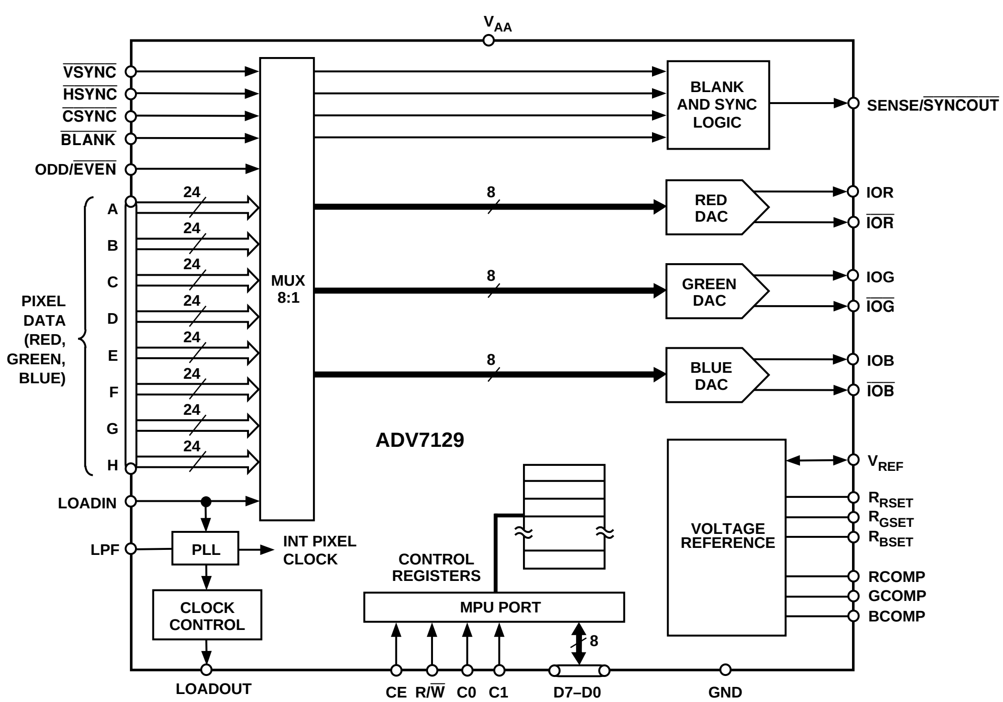
(continued on page 10)

FUNCTIONAL BLOCK DIAGRAM



REV. 0

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ADV7129–SPECIFICATIONS (V_{AA}[1] = +5 V, V_{REF} = +1.235 V, R_{RSET}, R_{GSET}, R_{BSET} = 280 Ω, R_L = 25 Ω, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

All Versions	Conditions[1]	Min	Typ	Max	Units
STATIC PERFORMANCE[3]					
Resolution (Each DAC)				8	Bits
Accuracy (Each DAC)					
Integral Nonlinearity				±1	LSB
Differential Nonlinearity	Guaranteed Monotonic			±1	LSB
Gray Scale Error				±5	% Gray Scale
					Binary Coding
DIGITAL INPUTS					
Input High Voltage, V_{INH}		2.0		V_{AA} + 0.5	V
Input Low Voltage, V_{INL}		GND – 0.5		0.8	V
Input Current, I_{IN}	V_{IN} = 0.4 V or 2.4 V			±10	μA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS					
Output High Voltage, V_{OH}	I_{OH} = –400 μA	2.4			V
Output Low Voltage, V_{OL}	I_{OL} = 3.2 mA			0.4	V
Floating-State Leakage Current				±10	μA
Floating-State Output Capacitance			10		pF
ANALOG OUTPUTS					
Gray Scale Current Range		10		60	mA
Output Current					
White Level Relative to Black		50.16	52.80	55.44	mA
Black Level Relative to Blank		4.1	4.32	4.54	mA
Blank Level, Sync Disabled		0	5	50	μA
LSB Size			223		μA
DAC to DAC Matching			2	5	%
Output Compliance, V_{OC}		0		1.4	V
Output Impedance, R_{OUT}			10		kΩ
Output Capacitance, C_{OUT}			20		pF
VOLTAGE REFERENCE					
Voltage Reference Range, V_{REF}	V_{REF} = 1.234 V for Specified	1.14	1.235	1.30	V
Input Current, I_{VREF}	Performance		5		μA
POWER REQUIREMENTS					
V_{AA}			5		V
I_{AA}[4]	Analog Current		160	200	mA
I_{AA}[4]	Digital Current @ 360 MHz		360	400	mA
Power Supply Rejection Ratio			0.12		%/%
DYNAMIC PERFORMANCE					
Clock and Data Feedthrough[5]			–30		dB
Glitch Impulse			50		pV secs
DAC to DAC Crosstalk[6]			–23		dB

NOTES
[1]±5% for all versions.
[2]Temperature range (T_{MIN} to T_{MAX}), 0°C to +70°C, TJ (Silicon Junction Temperature) ≤100°C.
[3]Static performance is measured with the Gain Error Registers set to 00H (disabled).
[4]I_{AA} is measured with a typical dynamic pattern, satisfying the absolute maximum current spec for the DACs.
[5]Clock and Data Feedthrough is a function of the amount of overshoot and undershoot on the digital inputs. Glitch impulse includes clock and data feedthrough. TTL input values are 0 V to 3 V, with input rise/fall times ≥3 ns, measured at the 10% and 90% points. Timing reference points are at 50% for inputs and outputs.
[6]DAC to DAC crosstalk is measured by holding one DAC high while the other two DACs are making low to high and high to low transitions.
Specifications subject to change without notice.

TIMING SPECIFICATIONS

(V_{AA}[2] = +5 V, V_{REF} = +1.235 V, R_{RSET}, R_{GSET}, R_{BSET} = 280 Ω, R_L = 25 Ω for IOG, IOR, IOB, C_L = 10 pF. All specifications T_{MIN} to T_{MAX}[3] unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Units
CLOCK CONTROL & PIXEL PORT[4]					
LOADIN Clocking Rate, f_{LCLK}		10		45	MHz
LOADIN Cycle Time, t_1		16.67			ns
LOADIN Low Time, t_2		6.67			ns
LOADIN High Time, t_3		6.67			ns
LOADIN to LOADOUT Delay, t_4			5		ns
Pixel Setup Time, t_5		1	0		ns
Pixel Hold Time, t_6		4	2		ns
MPU PORT					
R/$\overline{W}$, C0, C1 Setup Time, t_7		10	2.5		ns
R/$\overline{W}$, C0, C1 Hold Time, t_8		10	0.5		ns
$\overline{CE}$ Low Time, t_9		25			ns
$\overline{CE}$ High Time, t_{10}		25			ns
$\overline{CE}$ Asserted to Data-Bus Driven, t_{11}		2	5		ns
$\overline{CE}$ Asserted to Data-Bus Valid, t_{12}				20	ns
$\overline{CE}$ Negated to Data-Bus Invalid, t_{13}		1			ns
$\overline{CE}$ Negated to Data-Bus Three Stated, t_{14}				15	ns
Write Data (D7–D0) Setup Time, t_{15}		10			ns
Write Data (D7–D0) Hold Time, t_{16}		10			ns
ANALOG OUTPUTS[5]					
Analog Output Delay, t_{17}	@ 360 MHz		5		ns
Analog Output Rise/Fall Time, t_{18}			0.8		ns
Analog Output Transition Time, t_{19}			25		ns
RGB Analog Output Skew, t_{SK}				1.5	ns
Pipeline Delay, t_{PD}			19		PCLKs
PLL PERFORMANCE[6]					
Jitter (1σ)	(LOADIN = 45 MHz)		55		ps rms

NOTES

[1]TTL inputs values are 0 V to 3 V with input rise/fall times ≥3 ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. Analog output load ≤10 pF. Databus (D7–D0) loaded as shown in Figure 1. Digital output load for SENSE ≤30 pF.

[2]±5% for all versions.

[3]Temperature range (T_{MIN} to T_{MAX}), 0°C to +70°C.

[4]Pixel Port consists of the following inputs: Pixel Inputs: RED [A-H], BLUE [A-H], GREEN [A-H].

[5]Output Delay is measured from the 50% rising edge of LOADIN to the 50% point of full-scale transition on the A pixel. t_{17} includes the analog delay due to DACs and internal gate transitions plus the pipeline stages delay. The output delay for pixels B-H will be the output delay to the A pixel (t_{17}) plus the appropriate number of clock cycles. Output rise/fall time is measured between the 10% and 90% points of full-scale transition. Settling time is measured from the 50% point of full-scale transition to the output remaining within 1%. (Settling Time does not include clock and data feedthrough.)

[6]Jitter is measured by triggering on the output clock, delayed by 15 µs and then measuring the time period from the trigger edge to the next edge of the output clock after the delay. This measurement is repeated multiple times and the rms value is determined.

Specifications subject to change without notice.

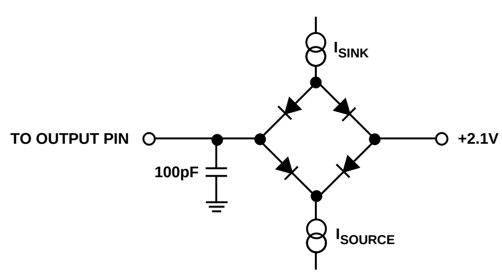


Figure 1. LOADIN vs. Pixel Input Data

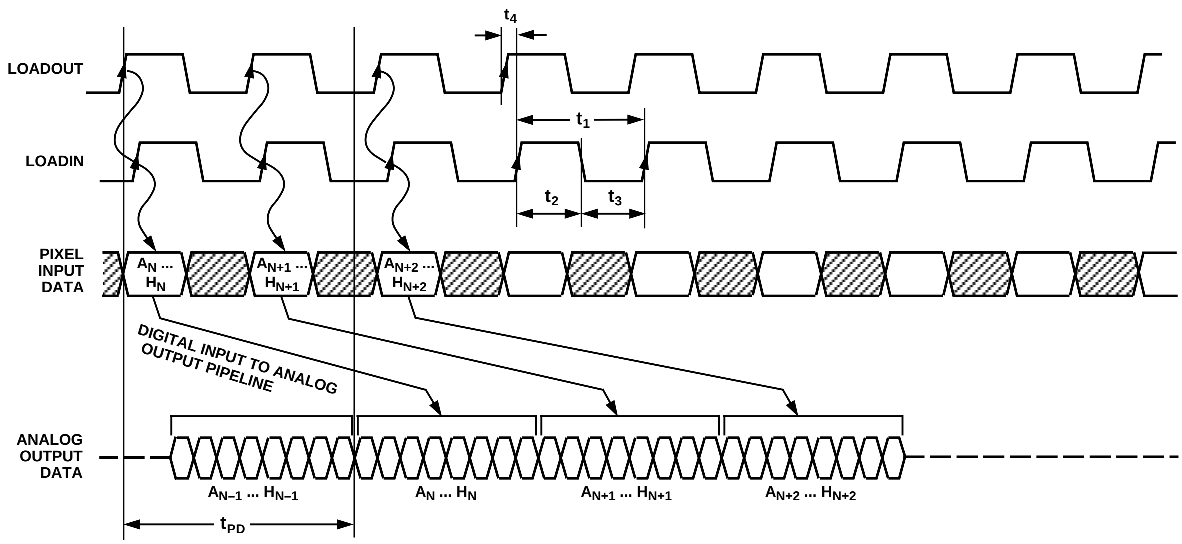


Figure 2. LOADIN vs. Pixel Input Data

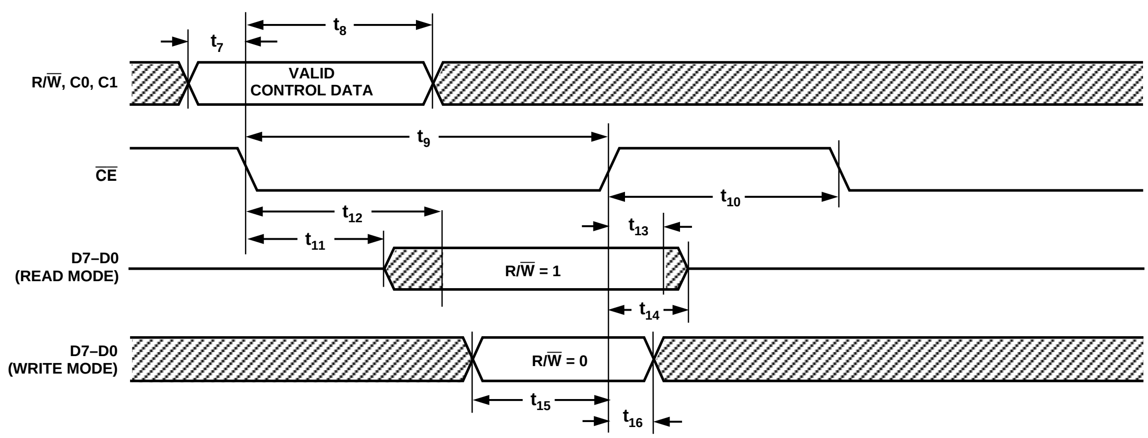
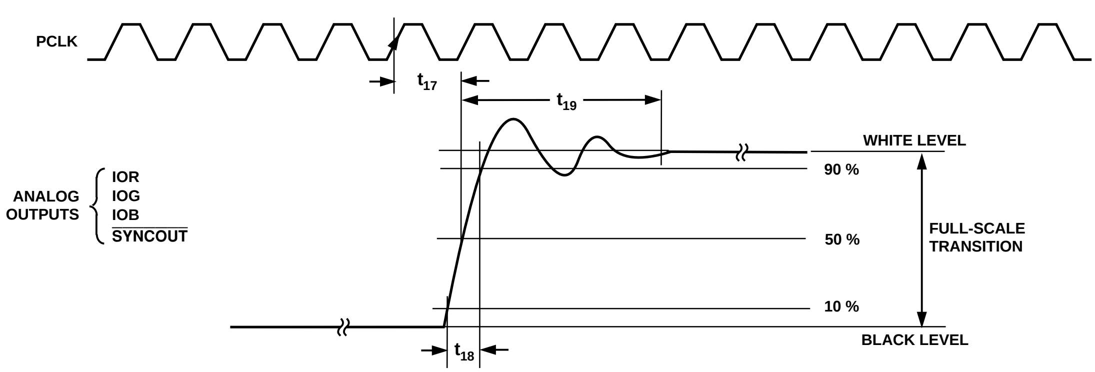


Figure 3. Microprocessor Port (MPU) Interface Timing



NOTE:
THIS DIAGRAM IS NOT TO SCALE.
FOR THE PURPOSES OF CLARITY, THE ANALOG OUTPUT WAVEFORM IS MAGNIFIED IN TIME AND AMPLITUDE W.R.T THE CLOCK WAVEFORM.
$\overline{\text{SYNCOUT}}$ IS A DIGITAL VIDEO OUTPUT SIGNAL.
t_{17} IS THE ONLY RELEVENT TIMING SPECIFICATION FOR $\overline{\text{SYNCOUT}}$.

Figure 4. Analog Output Response vs. LOADIN

ABSOLUTE MAXIMUM RATINGS[1]

V_{AA} to GND . . . . 7 V
Voltage on Any Digital Pin . . . . GND – 0.5 V to V_{AA} + 0.5 V
Ambient Operating Temperature (T_A) . . . . 0°C to +70°C
Storage Temperature (T_S) . . . . –65°C to +150°C
Junction Temperature (T_J) . . . . +150°C
Lead Temperature (Soldering, 10 sec) . . . . +260°C
Vapor Phase Soldering (1 minute) . . . . +220°C
Analog Outputs to GND[2] . . . . GND – 0.5 V to V_{AA}
Current on Any DAC Output . . . . 60 mA

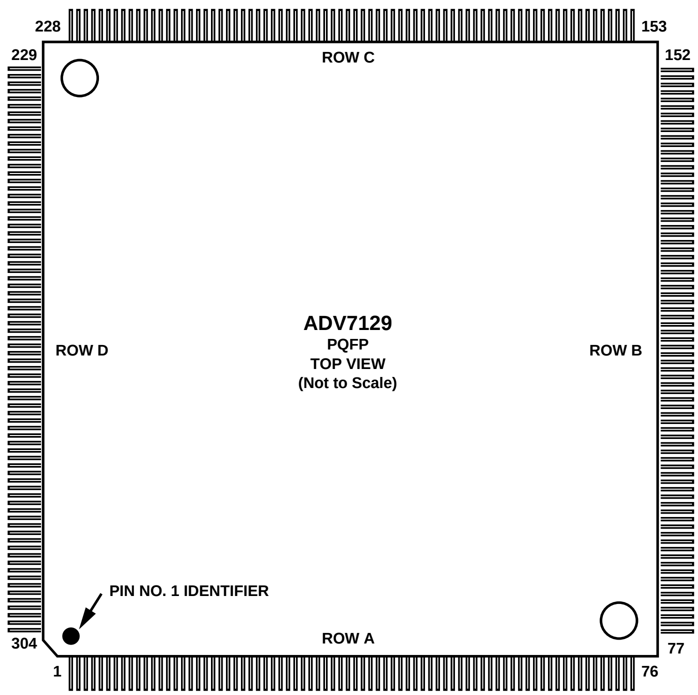
NOTES
[1]Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

ORDERING GUIDE*

Model	Temperature Range	Package Option
ADV7129KS	0°C to +70°C	S-304

*Due to the specialized nature and application of this part, it is not automatically available to order. Please contact your local sales office for details.

304-LEAD PQFP PIN CONFIGURATION



CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7129 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN ASSIGNMENTS

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
1	GND	41	$G4_C$	81	GND	121	$B4_E$
2	GND	42	$G4_B$	82	GND	122	$B4_D$
3	GND	43	$G4_A$	83	$G1_A$	123	$B4_C$
4	GND	44	V_{AA}	84	$G0_H$	124	$B4_B$
5	GND	45	GND	85	$G0_G$	125	$B4_A$
6	GND	46	V_{AA}	86	$G0_F$	126	$B3_H$
7	$R0_E$	47	GND	87	$G0_E$	127	$B3_G$
8	$R0_D$	48	$G3_H$	88	$G0_D$	128	$B3_F$
9	$R0_C$	49	$G3_G$	89	$G0_C$	129	$B3_E$
10	$R0_B$	50	$G3_F$	90	$G0_B$	130	$B3_D$
11	$R0_A$	51	$G3_E$	91	$G0_A$	131	$B3_C$
12	$G7_H$	52	$G3_D$	92	$B7_H$	132	$B3_B$
13	$G7_G$	53	$G3_C$	93	$B7_G$	133	$B3_A$
14	$G7_F$	54	$G3_B$	94	$B7_F$	134	$B2_H$
15	$G7_E$	55	$G3_A$	95	$B7_E$	135	$B2_G$
16	$G7_D$	56	$G2_H$	96	$B7_D$	136	$B2_F$
17	$G7_C$	57	$G2_G$	97	$B7_C$	137	$B2_E$
18	$G7_B$	58	$G2_F$	98	$B7_B$	138	$B2_D$
19	$G7_A$	59	$G2_E$	99	$B7_A$	139	$B2_C$
20	$G6_H$	60	$G2_D$	100	$B6_H$	140	$B2_B$
21	$G6_G$	61	$G2_C$	101	$B6_G$	141	$B2_A$
22	$G6_F$	62	$G2_B$	102	$B6_F$	142	$B1_H$
23	$G6_E$	63	$G2_A$	103	$B6_E$	143	$B1_G$
24	$G6_D$	64	$G1_H$	104	$B6_D$	144	$B1_F$
25	$G6_C$	65	$G1_G$	105	$B6_C$	145	$B1_E$
26	$G6_B$	66	$G1_F$	106	$B6_B$	146	$B1_D$
27	$G6_A$	67	$G1_E$	107	$B6_A$	147	GND
28	$G5_H$	68	$G1_D$	108	$B5_H$	148	GND
29	$G5_G$	69	$G1_C$	109	$B5_G$	149	GND
30	$G5_F$	70	$G1_B$	110	$B5_F$	150	GND
31	$G5_E$	71	GND	111	$B5_E$	151	GND
32	$G5_D$	72	GND	112	$B5_D$	152	GND
33	$G5_C$	73	GND	113	$B5_C$	153	GND
34	$G5_B$	74	GND	114	$B5_B$	154	GND
35	$G5_A$	75	GND	115	$B5_A$	155	GND
36	$G4_H$	76	GND	116	V_{AA}	156	GND
37	$G4_G$	77	GND	117	GND	157	GND
38	$G4_F$	78	GND	118	$B4_H$	158	GND
39	$G4_E$	79	GND	119	$B4_G$	159	$B1_C$
40	$G4_D$	80	GND	120	$B4_F$	160	$B1_B$

*No Connect.

Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic	Pin No.	Mnemonic
161	$B1_A$	197	R_{BIAS}	233	GND	269	LOADOUT
162	$B0_H$	198	SENSE/$\overline{\text{SYNCOUT}}$	234	GND	270	$R4_B$
163	$B0_G$	199	V_{REF}	235	$R6_H$	271	$R4_A$
164	$B0_F$	200	GND	236	$R6_G$	272	$R3_H$
165	$B0_E$	201	D0	237	$R6_F$	273	$R3_G$
166	$B0_D$	202	D1	238	$R6_E$	274	$R3_F$
167	$B0_C$	203	D2	239	$R6_D$	275	$R3_E$
168	$B0_B$	204	D3	240	$R6_C$	276	$R3_D$
169	$B0_A$	205	GND	241	$R6_B$	277	$R3_C$
170	$\overline{\text{BLANK}}$	206	V_{AA}	242	$R6_A$	278	$R3_B$
171	$\overline{\text{HSYNC}}$	207	D4	243	$R5_H$	279	$R3_A$
172	$\overline{\text{VSYNC}}$	208	D5	244	$R5_G$	280	$R2_H$
173	ODD/$\overline{\text{EVEN}}$	209	D6	245	$R5_F$	281	$R2_G$
174	NC*	210	D7	246	V_{AA}	282	$R2_F$
175	GND	211	$\overline{\text{CE}}$	247	GND	283	$R2_E$
176	GND	212	R/$\overline{\text{W}}$	248	V_{AA}	284	$R2_D$
177	$\overline{\text{IOB}}$	213	C0	249	GND	285	$R2_C$
178	IOB	214	C1	250	$R5_E$	286	$R2_B$
179	R_{BSET}	215	$R7_H$	251	$R5_D$	287	$R2_A$
180	B_{COMP}	216	$R7_G$	252	$R5_C$	288	$R1_H$
181	V_{AA}	217	$R7_F$	253	$R5_B$	289	$R1_G$
182	V_{AA}	218	$R7_E$	254	$R5_A$	290	$R1_F$
183	B_{BIAS}	219	$R7_D$	255	$R4_H$	291	$R1_E$
184	$\overline{\text{IOG}}$	220	$R7_C$	256	$R4_G$	292	$R1_D$
185	IOG	221	$R7_B$	257	$R4_F$	293	$R1_C$
186	R_{GSET}	222	$R7_A$	258	$R4_E$	294	$R1_B$
187	G_{COMP}	223	GND	259	$R4_D$	295	$R1_A$
188	V_{AA}	224	GND	260	$R4_C$	296	$R0_H$
189	V_{AA}	225	GND	261	GND	297	$R0_G$
190	G_{BIAS}	226	GND	262	GND	298	$R0_F$
191	$\overline{\text{IOR}}$	227	GND	263	V_{AA}	299	GND
192	IOR	228	GND	264	LPF	300	GND
193	R_{RSET}	229	GND	265	GND	301	GND
194	R_{COMP}	230	GND	266	LOADIN	302	GND
195	V_{AA}	231	GND	267	GND	303	GND
196	V_{AA}	232	GND	268	$\overline{\text{CSYNC}}$	304	GND

*No Connect.

PIN DESCRIPTION

Mnemonic	Function
R7–R0[A . . . H]	Red Pixel Port Inputs (TTL Compatible Inputs). Eight sets of eight bits latched on the rising edge of LOADIN.
G7–G0[A . . . H]	Green Pixel Port Inputs (TTL Compatible Inputs). Eight sets of eight bits latched on the rising edge of LOADIN.
B7–B0[A . . . H]	Blue Pixel Port Inputs (TTL Compatible Inputs). Eight sets of eight bits latched on the rising edge of LOADIN.
$\overline{\text{BLANK}}$	Composite Blank (TTL Compatible Input). This video control signal drives the analog outputs to the blanking level. When $\overline{\text{BLANK}}$ is at logic "0," the pixel inputs are ignored. Pedestal selection is controlled by Bit CR15 of Command Register 1. $\overline{\text{BLANK}}$ is latched on the rising edge of LOADIN.
ODD/$\overline{\text{EVEN}}$	Odd/Even Field Input (TTL Compatible Input). This input indicates which field of the frame is being displayed. An even field is selected by setting ODD/$\overline{\text{EVEN}}$ to logical "0." An odd field is selected by setting ODD/$\overline{\text{EVEN}}$ to logical "1." ODD/$\overline{\text{EVEN}}$ should be changed only during vertical blank.
$\overline{\text{HSYNC}}$	Horizontal-Sync Input (TTL Compatible Input). This control signal is latched on the rising edge of LOADIN.
$\overline{\text{VSYNC}}$	Vertical-Sync Input (TTL Compatible Input). This control signal is latched on the rising edge of LOADIN.
$\overline{\text{CSYNC}}$	Composite-Sync Input (TTL Compatible Input). This video control signal drives the analog outputs to the $\overline{\text{SYNC}}$ level. It is only asserted during the blanking period and does not override any other control or data input. CR14, CR13 or CR12 of Command Register 1 must be set together with CR11 or Command Register 1 to decode $\overline{\text{SYNC}}$ onto the IOR/$\overline{\text{IOR}}$, IOG/$\overline{\text{IOG}}$ or IOB/$\overline{\text{IOB}}$ analog outputs, otherwise the $\overline{\text{SYNC}}$ input is ignored.
$\overline{\text{CE}}$	Chip Enable Input (TTL Compatible Input). This input must be set to logic "0" when writing or reading over the data bus (D7–D0). Internally, data is latched on the rising edge of $\overline{\text{CE}}$.
R/$\overline{\text{W}}$	Read/Write pin (TTL Compatible Input). This signal is latched on the falling edge of $\overline{\text{CE}}$. A high level indicates a read operation and a low level indicates a write operation.
C0, C1	Register select pins (TTL Compatible Inputs). These inputs select which MPU port register is selected for writing or reading. Data is latched on the falling edge of $\overline{\text{CE}}$.
D7–D0	Data Bus (TTL Compatible Input/Output Bus). Data, including color palette values and device control information is written to and read from the device over this 8-bit, bidirectional databus. Any unused bits of the data bus should be terminated through a resistor to either the digital power plane (V_{CC}) or GND.
LOADIN	Pixel Data Load Input (TTL Compatible Input). This input latches the multiplexed pixel data, including $\overline{\text{BLANK}}$, $\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{CSYNC}}$, and ODD/$\overline{\text{EVEN}}$ into the device. This rising edge of this signal is used to latch in the video signal inputs. It is also used as a reference frequency to generate an 8 × multiple pixel clock using the fixed reference onboard PLL.
LOADOUT	Pixel Data Load Output (TTL Compatible Output). This digital output is PCLK/8. If the onboard phase lock loop is used, it has the same phase as LOADIN.
LPF	Low-Pass Filter Pin. This pin stabilizes the internal PLL. The following network is recommended.

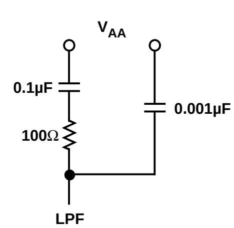


Figure 5.

Mnemonic	Function
IOR, IOG, IOB	Red, Green & Blue Current Outputs (High Impedance Current Sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into doubly terminated 50 Ω or 75 Ω loads.
$\overline{IOR}$, $\overline{IOG}$, $\overline{IOB}$	Differential Red, Green & Blue Current Outputs (High Impedance Current Sources). These RGB video outputs are specified to directly drive RS-343A and RS-170 video levels into doubly terminated 50 Ω or 75 Ω loads. If the complementary outputs are not required, then these outputs should be tied to GND.
R_{COMP}	Red Compensation pin. This pin should be bypassed to V_{AA} with 0.01 μF capacitor.
G_{COMP}	Green Compensation pin. This pin should be bypassed to V_{AA} with 0.01 μF capacitor.
B_{COMP}	Blue Compensation pin. This pin should be bypassed to V_{AA} with 0.01 μF capacitor.
R_{RSET}, R_{GSET}, R_{BSET}	DAC Output Full-Scale Adjust Control (Analog Input): A resistor from this pin to ground sets the current in the DACs. The current in the DACs is set according to the equations: $I_{OUT} = 12{,}950 \times V_{REF}/R_{SET}$ (*$\overline{SYNC}$ not encoded on the DAC Output*) $I_{OUT} = 18{,}137 \times V_{REF}/R_{SET}$ (*$\overline{SYNC}$ encoded on the DAC Output*) To generate RS 343-A video levels on the DAC outputs, a resistor value of 280 Ω is recommended for doubly terminated 50 Ω lines. Any combination of R_{SET} value, DAC termination resistor and programming of $\overline{SYNC}$ and pedestal are possible provided that the maximum DAC current and the DAC output compliance specifications are adhered to. For example, in a doubly terminated 50 Ω system with no $\overline{SYNC}$ or pedestal encoded on the DAC outputs, an R_{SET} value of 280 Ω gives a DAC full-scale output of 52.8 mA, i.e., a white-to-black value of 1.4 V. This example would give a 6 dB reduction in noise and feedthrough on the DAC outputs (compared to a 0.7 V full-scale value), but may require a 0.5X splitter at the monitor.
R_{BIAS}	Red Bias node. This node should be decoupled to V_{AA} with a 0.01 μF capacitor.
G_{BIAS}	Green Bias node. This node should be decoupled to V_{AA} with a 0.01 μF capacitor.
B_{BIAS}	Blue Bias node. This node should be decoupled to V_{AA} with a 0.01 μF capacitor.
SENSE/$\overline{SYNCOUT}$	Comparator Sense Output (TTL Compatible Output). This output will be logic "1" if one or more of the analog outputs exceeds the internal voltage of the SENSE comparator circuit. It can be used to determine the absence of a CRT monitor. The value of the SENSE Output corresponds to the current pixel at the outputs. The output can drive one CMOS load. This pin can alternately be programmed to be a TTL sync output which is a delayed version of $\overline{CSYNC}$.
V_{REF}	Voltage Reference (Analog Input/Output): This should always have a 0.1 μF decoupling capacitor attached between V_{REF} and V_{AA}. If nothing else is connected then the DACs are driven by the internal voltage reference. If it is required to use a more accurate reference, then this pin acts as an overdrive input. An external 1.235 V voltage reference such as the AD1580 or equivalent is recommended to drive this input. (Note: It is not recommended to use a resistor network to generate the voltage reference.)
V_{AA}	Power Supply (+5 V ± 5%). The part contains multiple power supply pins, all should be connected together to one common +5 V filtered analog power supply.
GND	Analog Ground. The part contains multiple ground pins, all should be connected together to the system's ground plane.

(continued from page 1)

The ADV7129 supports 24-bit true-color formats where screen resolution is the primary design goal. The individual Red, Green and Blue pixel input ports allow true-color image rendition at resolutions of 2048 × 2048 × 24 bit.

The ADV7129 is capable of generating RGB video output signals that are compatible with RS-343A and RS-170 video standards, without requiring external buffering.

An internal voltage reference is also provided to simplify system design.

The ADV7129 is fabricated in a +5 V CMOS process.

The ADV7129 is packaged in a 304-pin PQFP package.

CIRCUIT DETAILS AND OPERATION

Digital video or pixel data is latched into the ADV7129 over the pixel port. The data is multiplexed and latched into the three 8-bit digital-to-analog converters (DACs) and output as an RGB video signal.

The ADV7129 can be broken into three sections for purposes of clarity of explanation:

1. Pixel port and clock control circuit.
2. MPU port, registers and cursor.
3. Digital-to-analog converters and video outputs.

Pixel Port and Clock Circuits

The pixel port of the ADV7129 is directly interfaced to the video/graphics pipeline of a computer graphics subsystem. It is connected directly through a gate array to the video RAM of the system's frame buffer. The pixel port of the ADV7129 consists of:

Color Data:	RED, GREEN, BLUE
Pixel Controls:	$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{CSYNC}}$, $\overline{\text{BLANK}}$

The associated clocking signals for the pixel port include:

Clock Input	LOADIN
Clock Output	LOADOUT

Pixel Port (Color Data)

The ADV7129 has 192 color data inputs. This supports 24-bit true color with 8:1 multiplexing.

Color data is always latched on the rising edge of LOADIN. LOADOUT is generated internally by the ADV7129. The frequency of LOADOUT is the internal clock frequency (PCLK) divided by 8.

Other pixel data signals latched into the part by LOADIN include $\overline{\text{HSYNC}}$, $\overline{\text{BLANK}}$, $\overline{\text{VSYNC}}$ and $\overline{\text{CSYNC}}$.

$\overline{\text{HSYNC}}$, $\overline{\text{VSYNC}}$, $\overline{\text{CSYNC}}$, $\overline{\text{BLANK}}$

The $\overline{\text{BLANK}}$ and SYNC video control signals drive the analog outputs to the blanking and sync levels respectively. These are latched on the rising edge of LOADIN. The SYNC information can be encoded onto any of the IOG, IOR or IOB analog outputs by setting Bits CR12, CR13 or CR14 of Command Register 1 to logic "1."

The SYNC information is ignored if Bits CR12, CR13 and CR14 of Command Register 1 are set to logic "0."

The SYNC and BLANK information can be decoded onto the inverted outputs by setting CR10 and CR11 of Command Register 1 to logic level "1."

SENSE

If any one or more of the analog outputs, IOG, IOR and IOB, exceed the internal voltage reference level (due to absence of CRT), SENSE is set to logic "1." The SENSE output can drive one CMOS load and can be used to determine the absence of a CRT monitor.

CLOCK CONTROL CIRCUIT

The ADV7129 has an integrated clock control circuit. This circuit is capable of generating the internal clocking signals.

A lower frequency external clock generator is used by enabling the onboard PLL. This fixed multiple PLL is used to speed up LOADIN by a factor of 8. This onboard 8 × clock multiplier is activated by setting Bit CR20 of Command Register 2 from logic "0" to logic "1." It must be set up after power-up.

MICROPROCESSOR (MPU) PORT

The ADV7129 supports a standard MPU interface. All the functions of the part are controlled via this MPU port. Direct access is gained to the address register and all the control registers as well as the cursor palette. The following sections describe the setup for reading and writing to all of the devices' registers.

MPU Interface

The MPU interface consists of a bidirectional, 8-bit wide databus and interface control signals R/$\overline{\text{W}}$, $\overline{\text{CE}}$, C1, C0. Two write operations are required to set up the lower 8 bits and higher 2 bits of the Address Register.

Register Mapping

The ADV7129 contains a number of onboard registers including the Address Register, Command Registers and Gain Error Registers. Control Lines C1-C0 determine whether the Address Register is being pointed to (upper or lower bytes) or whether the other registers are being accessed.

The R/$\overline{\text{W}}$ and $\overline{\text{CE}}$ control inputs allow read and write access. All registers can to read and written to.

Power-On Reset

After power-up, the ADV7129 must be set to perform a reset operation. This is achieved by resetting the PLL (a low to high transition on Bit CR20 of Command Register 2). This initializes the pixel port such that the pixel sequence ABCDEFGH starts at A. This reset can be performed as the registers are being initialized. The Command Registers power up in an indeterminate state and must be set up for the required operation. The power-on is activated when V_{AA} goes from 0 V to 5 V. This is active for 1 µs. The ADV7129 should not be accessed during this period.

Register Accesses

The MPU can write to or read from all of the ADV7129s' registers. Figure 6 shows the Control Registers and C1-C0 Control Input Truth Table. The read/write timing is controlled by the $\overline{\text{CE}}$ and R/$\overline{\text{W}}$ inputs. The Address Register determines which Control Register is being accessed.

The registers can be addressed directly by two write cycles to set up the high and low bytes of Address Register and then by a read or write cycle of the MPU.

REGISTER PROGRAMMING

The following section describes each register, including Address Register and each of the Control Registers in terms of its configuration.

Address Register (A10–A0)

As illustrated previously, the C1–C0 inputs, in conjunction with the Address Register specify which control register, or palette RAM location is accessed by the MPU port. The Address Register is 16 bits wide and can be read from as well as written to.

CONTROL REGISTERS

A large bank of registers can be accessed using the Address register and C1–C0. Access is made first by writing the Address Register with the appropriate address to point to the particular Control Register, and then performing an MPU access to the Control Register.

ADDRESS REGISTER (A10–A0)

C1	C0	$R/\overline{W}$	
0	0	0	WRITE TO ADDRESS REGISTER (LOWER BYTE)
0	1	0	WRITE TO ADDRESS REGISTER (UPPER BYTE)
1	0	0	WRITE TO REGISTERS
0	0	1	READ FROM ADDRESS REGISTER (LOWER BYTE)
0	1	1	READ FROM ADDRESS REGISTER (UPPER BYTE)
1	0	1	READ FROM REGISTERS
1	1	X	RESERVED

(A10–A0)	REGISTER ACCESS
4FF–412	RESERVED
411	COMMAND REGISTER 2
410	RESERVED
40F	RESERVED
40E	RESERVED
40D	RESERVED
40C	RESERVED
40B	RESERVED
40A	RESERVED
409	RESERVED
408	RESERVED
407	BLUE DAC GAIN ERROR REGISTER
406	GREEN DAC GAIN ERROR REGISTER
405	RED DAC GAIN ERROR REGISTER
004	RESERVED
403	RESERVED
402	RESERVED
401	RESERVED
400	COMMAND REGISTER 1
000–3FF	RESERVED

Figure 6. Control Registers

COMMAND REGISTER 1 (CR1)

(Address Register (A10–A0) = 400H)

This register contains a number of control bits as shown in the diagram. CR1 is an 8-bit wide register.

Figure 7 shows the various operations under the control of CR1. This register can be read from as well as written to. Bit CR16 is reserved and should be set to logic "1."

COMMAND REGISTER 1-BIT DESCRIPTION

$\overline{\text{BLANK}}$ Control on Inverted Outputs (CR10):

This bit specifies whether the video $\overline{\text{BLANK}}$ is to be decoded onto the inverted analog outputs or ignored.

$\overline{\text{SYNC}}$ Control on Inverted Outputs (CR11)

This bit specifies whether the video $\overline{\text{SYNC}}$ is to be decoded onto the inverted analog outputs or ignored.

$\overline{\text{SYNC}}$ Recognition on Blue (CR12)

This bit specifies whether the video $\overline{\text{SYNC}}$ input is to be decoded onto the IOB analog output or ignored.

$\overline{\text{SYNC}}$ Recognition on Green (CR13)

This bit specifies whether the video $\overline{\text{SYNC}}$ input is to be decoded onto the IOG analog output or ignored.

$\overline{\text{SYNC}}$ Recognition on Red (CR14)

This bit specifies whether the video $\overline{\text{SYNC}}$ input is to be decoded onto the IOR analog output or ignored.

Pedestal Enable Control (CR15)

This bit specifies whether a 0 IRE or a 7.5 IRE blanking pedestal is to be generated on the video outputs.

Display Mode Control (CR17)

This bit controls whether the display is interlaced or noninterlaced.

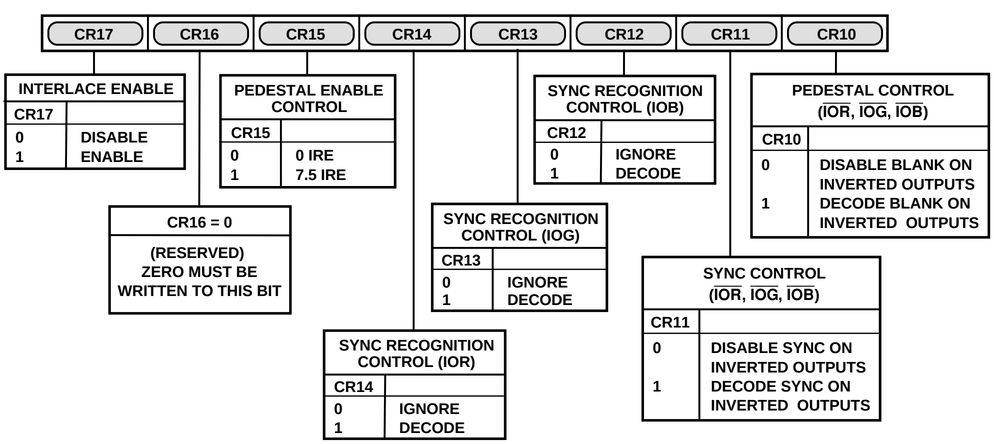


Figure 7. Command Register 1

COMMAND REGISTER 2 (CR2)
(Address Register (A10–A0) = 411H)

This register contains a number of control bits as shown in the diagram. CR2 is an 8-bit wide register. CR27, CR24, CR22 and CR21 are reserved and should be set to logic "0." Figure 8 shows the various operations under the control of CR2. This register can be read from as well as written to.

COMMAND REGISTER 2-BIT DESCRIPTION

PLL Control (CR20)

This bit resets the PLL divider when set to logic "0" and releases it when set to logic "1."

$\overline{\text{SYNCOUT}}$ Control (CR23)

This bit is an enable for SYNCOUT. If this bit is set to logic "1," the SENSE output becomes a pipelined version of $\overline{\text{CSYNC}}$. Otherwise the SENSE output remains unaffected.

SENSE Bit (CR25)

This output bit is used to determine the absence of a CRT monitor. When CR25 is set to logic "1," a CRT is not present. With some diagnostic code, the presence of loading on the individual RGB lines can be determined. The reference is generated by a voltage divider from the external voltage reference on the V_{REF} pin. For the proper operation, the following levels should be applied to the comparator by the IOR, IOG and IOB outputs:

DAC Low Voltage ≤ 250 mV.

DAC High Voltage ≥ 450 mV.

VCO Override Bit (CR26)

This bit is used to override the VCO and set the PLL to the lowest frequency possible. If the external LOADIN source takes some time before it reaches its required frequency, the internal PLL can become unstable as it tries to track to a varying LOADIN signal. The VCO override bit can be set to logic level "0" and then released (set to logic level "1") to allow the VCO to track to the input after it has stabilized. It is required to allow 200 µs before the VCO override bit is released.

GAIN ERROR REGISTERS
(Address Register (A10–A0) = 405H–407H)

The Red, Green and Blue Gain Error Registers allow the user to compensate for any channel-to-channel variations in the video output system. They control internal resistors from each of the three DAC outputs to GND, i.e., they appear in parallel with the external termination resistor across the DAC outputs. This allows the RGB output voltages to be adjusted as the value of R_{INT} is varied. A logic "1" on any of the control bits GR06 to GR00 switches in the appropriate resistor. A logic "0" disables or open circuits the resistor. Bit GR07 of the Gain Error Register enables or disables the Gain Error Adjust. Figure 9 shows the typical resistor values for these internal resistances versus R_{SET}.

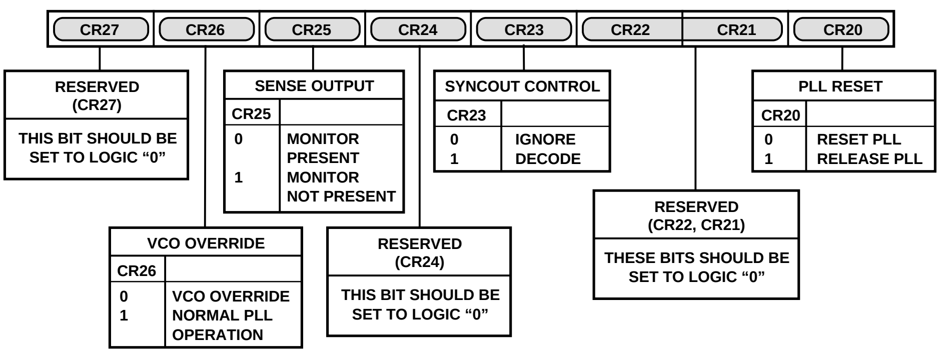
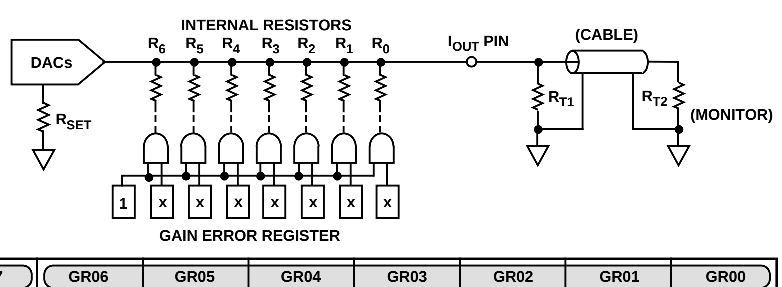


Figure 8. Command Register 2



GAIN ERROR CONTROL	
GR07	
0	DISABLE GAIN ERROR ADJ
1	ENABLE GAIN ERROR ADJ

REGISTER	(RESET = 280Ω)
GR06 R6	47Ω
GR05 R5	923Ω
GR04 R4	1926Ω
GR03 R3	3476Ω
GR02 R2	6979Ω
GR01 R1	16610Ω
GR00 R0	27037Ω

Figure 9. Gain Error Register

DIGITAL-TO-ANALOG CONVERTERS (DACS) AND VIDEO OUTPUTS

The ADV7129 contains three high speed video DACs. The DAC outputs are represented as the three primary analog color signals IOR (red video), IOG (green video) and IOB (blue video).

DACs and Analog Outputs

The part contains three matched 8-bit digital-to-analog converters. The DACs are designed using an advanced, high speed, segmented architecture. The bit currents corresponding to each digital input are routed to either IOR, IOG, IOB (bit = "1") or $\overline{IOR}$, $\overline{IOG}$, $\overline{IOB}$ (bit = "0"). Normally $\overline{IOR}$, $\overline{IOG}$, & $\overline{IOB}$ are connected to GND.

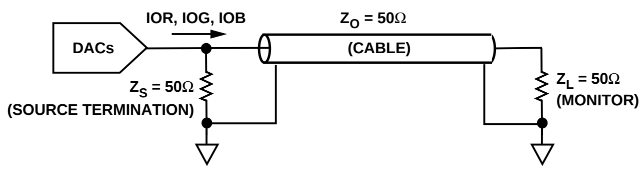


Figure 10. DAC Output Termination (Doubly Terminated 50 Ω Load)

The analog video outputs are high impedance current sources. Each of the these three RGB current outputs are specified to directly drive a 25 Ω load (doubly-terminated 50 Ω).

Reference Input and R_{SET}

An external 1.235 V voltage reference is preferred to set up the analog outputs of the ADV7129. The reference voltage is connected to the V_{REF} input. In the absence of an external reference, the on-chip voltage reference is internally connected to the V_{REF} pin. The internal reference will set up the DAC currents, although with slightly less accuracy.

A resistor R_{SET} is connected between the R_{SET} (R_{RSET}, R_{GSET}, R_{BSET}) input of the part and ground. An R_{SET} value of 280 Ω corresponds to the generation of two times RS-343A video levels into a doubly-terminated 50 Ω load. Figure 11 illustrates the resulting video waveform and the Video Output Truth Table illustrates the corresponding control input stimuli. On the ADV7129 $\overline{SYNC}$ can be encoded on any of the analog signals, however in practice, $\overline{SYNC}$ is generally encoded on either the IOG output or on all of the video outputs.

Any combination of R_{SET}, DAC termination resistors and programming of $\overline{SYNC}$ and pedestal are possible provided that the maximum DAC current of 60 mA and the DAC output compliance specifications are adhered to. The following tables show the current levels for different values of R_{SET} resistors and R_{LOAD} termination.

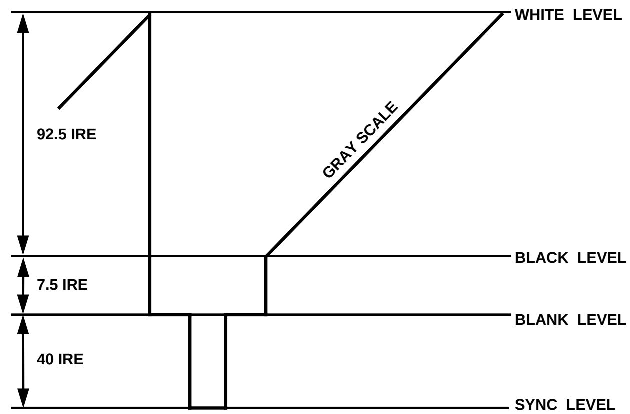


Figure 11. Composite Video Waveform SYNC Decoded; Pedestal = 7.5 IRE

Table I. Video Output Truth Table (R_{SET} = 398 Ω, R_{LOAD} = 37.5 Ω)

Description	O/P with Sync Enabled (mA)	O/P with Sync Disabled (mA)	SYNC	BLANK	DAC Input Data
WHITE LEVEL	26.67	19.05	1	1	FFH
VIDEO	Video + 9.05	Video + 1.44	1	1	Data
VIDEO to BLANK	Video + 1.44	Video + 1.44	0	1	Data
BLACK LEVEL	9.05	1.44	1	1	00H
BLACK to BLANK	1.44	1.44	0	1	00H
BLANK LEVEL	7.62	0	1	0	xxH
$\overline{\text{SYNC}}$ LEVEL	0	0	0	0	xxH

Table II. Video Output Truth Table (R_{SET} = 560 Ω, R_{LOAD} = 25 Ω)

Description	O/P with Sync Enabled (mA)	O/P with Sync Disabled (mA)	SYNC	BLANK	DAC Input Data
WHITE LEVEL	40	28.57	1	1	FFH
VIDEO	Video + 13.6	Video + 2.14	1	1	Data
VIDEO to BLANK	Video + 2.16	Video + 2.14	0	1	Data
BLACK LEVEL	13.6	2.14	1	1	00H
BLACK to BLANK	2.14	2.14	0	1	00H
BLANK LEVEL	11.44	0	1	0	xxH
$\overline{\text{SYNC}}$ LEVEL	0	0	0	0	xxH

Table III. Video Output Truth Table (R_{SET} = 280 Ω, R_{LOAD} = 25 Ω)

Description	O/P with Sync Disabled (mA)	SYNC	BLANK	DAC Input Data
WHITE LEVEL	52.8	0	0	FFH
VIDEO	Video + 0	0	0	Data
VIDEO to BLACK	Video + 0	0	0	Data
BLACK LEVEL	0	0	0	xxH

APPENDIX I
BOARD DESIGN AND LAYOUT CONSIDERATIONS

The ADV7129 is a highly integrated circuit containing both precision analog and high speed digital circuitry. It has been designed to minimize interference effects on the integrity of the analog circuitry by the high speed digital circuitry. It is imperative that these same design and layout techniques be applied to the system level design such that high speed, accurate performance is achieved. The "Recommended Analog Circuit Layout" (see Figure 12) shows the analog interface between the device and monitor.

The layout should be optimized for lowest noise on the ADV7129 power and ground lines by shielding the digital inputs and providing good decoupling. The lead length between groups of V_{AA} and GND pins should by minimized so as to minimize inductive ringing.

Ground Planes

The ground plane should encompass all ADV7129 ground pins, voltage reference circuitry, power supply bypass circuitry for the ADV7129, the analog output traces, and all the digital signal traces leading up to the ADV7129. The analog ground plane should be separated from the system ground plane by a ferrite bead.

Power Planes

The ADV7129 and any associated analog circuitry should have its own power plane, referred to as the analog power plane (V_{AA}). This power plane should be connected to the regular PCB power plane (V_{CC}) at a single point through a ferrite bead. This bead should be located within three inches of the ADV7129.

The PCB power plane should provide power to all digital logic on the PC board, and the analog power plane should provide power to all ADV7129 power pins and voltage reference circuitry.

Plane-to-plane noise coupling can be reduced by ensuring that portions of the regular PCB power and ground planes do not overlay portions of the analog power plane, unless they can be arranged such that the plane-to-plane noise is common mode.

Supply Decoupling

For optimum performance, bypass capacitors should be installed using the shortest leads possible, consistent with reliable operation, to reduce the lead inductance. Best performance is obtained with 0.1 µF ceramic capacitor decoupling. Each group of V_{AA} pins on the ADV7129 must have at least one 0.1 µF decoupling capacitor to GND. These capacitors should be placed as close as possible to the device.

It is important to note that while the ADV7129 contains circuitry to reject power supply noise, this rejection decreases with frequency. If a high frequency switching power supply is used, the designer should pay close attention to reducing power supply noise and consider using a three terminal voltage regulator for supplying power to the analog power plane.

Digital Signal Interconnect

The digital inputs to the ADV7129 should be isolated as much as possible from the analog outputs and other analog circuitry. Also, these input signals should not overlay the analog power plane.

Due to the high clock rates involved, long clock lines to the ADV7129 should be avoided to reduce noise pickup.

Any active termination resistors for the digital inputs should be connected to the regular PCB power plane (V_{CC}), and not the analog power plane.

Analog Signal Interconnect

The ADV7129 should be located as close as possible to the output connectors to minimize noise pickup and reflections due to impedance mismatch.

The video output signals should overlay the ground plane, and not the analog power plane, to maximize the high frequency power supply rejection.

Digital Inputs, especially Pixel Data Inputs and clocking signals (LOADOUT, LOADIN, etc.) should never overlay any of the analog signal circuitry and should be kept as far away as possible.

For best performance, the analog outputs should each have a 50 Ω load resistor connected to GND. These resistors should be placed as close as possible to the ADV7129 so as to minimize reflections.

There are a number of precautions that the user can take to minimize the effects of data feedthrough.

a. Apply external filtering to the DAC outputs.

b. Reduce input voltage risetime. From experiments, it has been seen that a reduction from 2 ns to 4 ns gives significant improvement.

c. Reduce input voltage swing. A reduction from 5 V to 3 V gives significant improvement.

d. Use series resistors on the pixel inputs (e.g., 100 Ω).

e. The part can be run at 2× DAC current levels as shown in the DAC output. The differential outputs can then be connected through a differential to single balun transformer to eliminate common-mode noise. A phase splitter should be used to reduce the 2× levels to 1× at the monitor end.

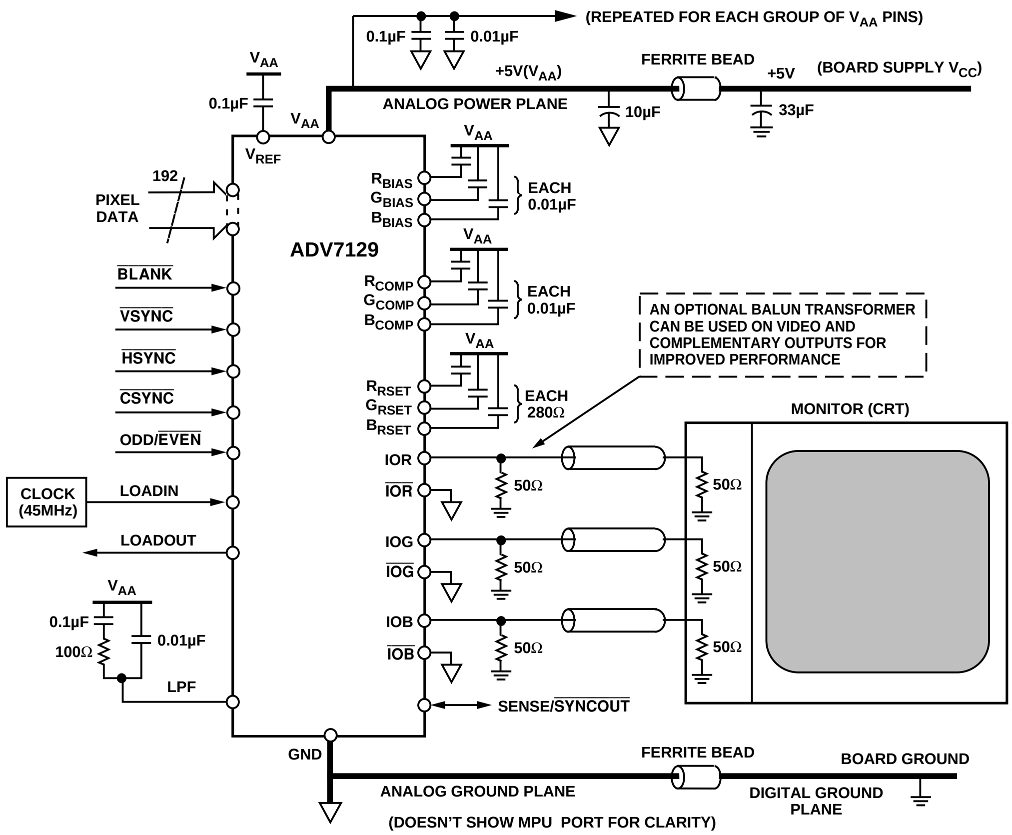


Figure 12. Typical Connection Diagram

APPENDIX II
THERMAL AND ENVIRONMENTAL CONSIDERATIONS

The ADV7129 is a very highly integrated monolithic silicon device. This high level of integration inevitably leads to consideration of thermal and environmental conditions which the ADV7129 must operate in. Reliability of the device is enhanced by keeping it as cool as possible. In order to avoid destructive damage to the device, the absolute maximum junction temperature must never be exceeded. Certain applications, depending on ambient temperature and pixel data rates may require forced air cooling or external heatsinks. The following data is intended as a guide in evaluating the operating conditions of a particular application so that optimum device and system performance is achieved.

It should be noted that information on package characteristics published herein may not be the most up to date at the time of reading this. Advances in package compounds and manufacture will inevitably lead to improvements in the thermal data. Please contact your local sales office for the most up-to-date information.

Package Characteristics
Junction-to-Case (θ_{JC}) Thermal Resistance for this particular part is:

$$\theta_{JC} = 8.9°C/W$$

(Note: θ_{JC} is independent of airflow.)

The maximum silicon junction temperature should be limited to 100°C. Temperatures greater than this will reduce long-term device reliability. To ensure that the silicon junction temperature stays within prescribed limits, the addition of an external heatsink can be used if the junction temperature is brought beyond the maximum limit.

Junction-to-Ambient (θ_{JA}) Thermal Resistance for this particular part is:

θ_{JA} = 25.9°C/W (Still Air)
θ_{JA} = will significantly decrease in air flow.

Thermal Model
The junction temperature of the device in a specific application is given by:

$$T_J = T_A + P_D\,(\theta_{JC} + \theta_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D\,(\theta_{JA}) \quad (2)$$

where:

T_J = Junction Temperature of Silicon (°C)
T_A = Ambient Temperature (°C)
P_D = Power Dissipation (W)
θ_{JC} = Junction to Case Thermal Resistance (°C/W)
θ_{CA} = Case to Ambient Thermal Resistance (°C/W)
θ_{JA} = Junction to Ambient Thermal Resistance (°C/W)

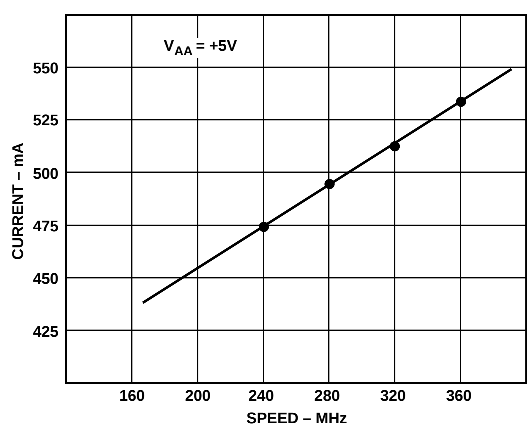
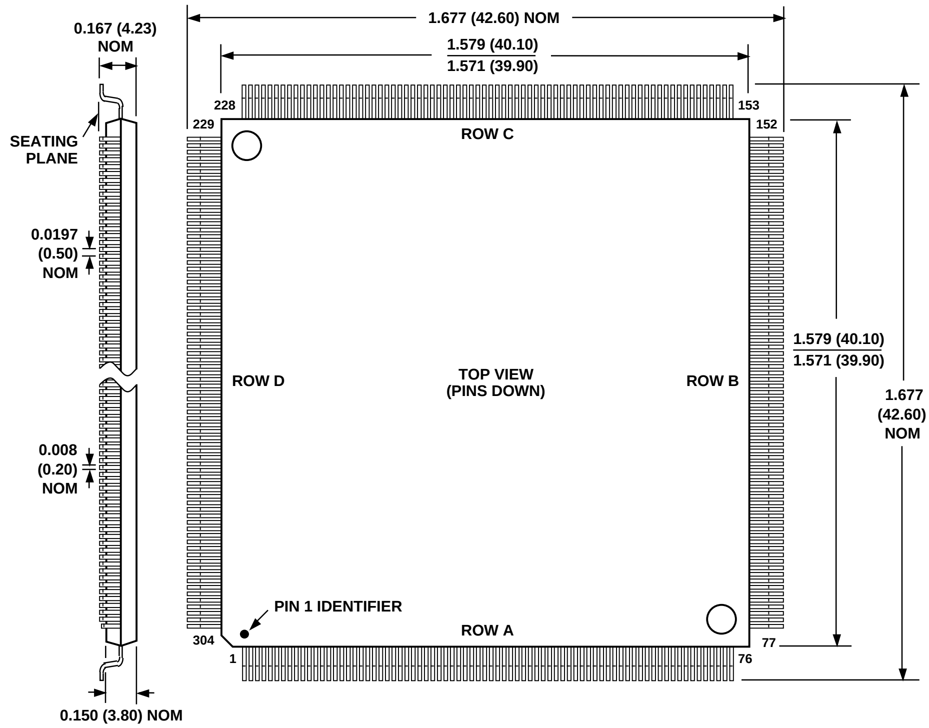


Figure 13. Supply Current vs. Frequency

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

304-Lead Plastic Quad Flatpack (S-304)



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