

## ADG608/ADG609

### FEATURES

- +3 V, +5 V,  $\pm 5$  V Power Supplies
- $V_{SS}$  to  $V_{DD}$  Analog Signal Range
- Low On Resistance (30  $\Omega$  max)
- Fast Switching Times
  - $t_{ON}$  75 ns max
  - $t_{OFF}$  45 ns max
- Low Power Dissipation (1.5  $\mu$ W max)
- Break-Before-Make Construction
- ESD > 5000 V as per Military Standard 3015.7
- TTL and CMOS Compatible Inputs

### APPLICATIONS

- Automatic Test Equipment
- Data Acquisition Systems
- Communication Systems
- Avionics and Military Systems
- Microprocessor Controlled Analog Systems
- Medical Instrumentation
- Battery Powered Instruments
- Remote Powered Equipment
- Compatible with  $\pm 5$  V DACs and ADCs such as AD7840/8, AD7870/1/2/4/5/6/8

### GENERAL DESCRIPTION

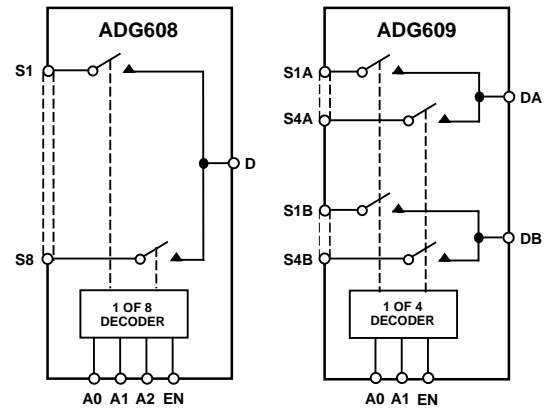
The ADG608 and ADG609 are monolithic CMOS analog multiplexers comprising eight single channels and four differential channels respectively, fully specified for  $\pm 5$  V, +5 V and +3 V power supplies. The ADG608 switches one of eight inputs to a common output as determined by the 3-bit binary address lines A0, A1 and A2. The ADG609 switches one of four differential inputs to a common differential output as determined by the 2-bit binary address lines A0 and A1. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF. All the address and enable inputs are TTL compatible over the full specified operating temperature range, making the parts suitable for bus-controlled systems such as data acquisition systems, process controls, avionics and ATEs since the TTL compatible address inputs simplify the digital interface design and reduce the board space requirements.

The ADG608/ADG609 are designed on an enhanced LC<sup>2</sup>MOS process that provides low power dissipation yet gives high switching speed and low on resistance. Each channel conducts equally well in both directions when ON and has an input signal range which extends to the supplies. In the OFF condition, signal levels up to the supplies are blocked. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. Inherent in the design is low charge injection for minimum transients when switching the digital inputs.

### REV. A

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### FUNCTIONAL BLOCK DIAGRAMS



The ability to operate from single +3 V, +5 V or  $\pm 5$  V bipolar supplies makes the ADG608 and ADG609 perfect for use in battery operated instruments and with the new generation of DACs and ADCs from Analog Devices. The use of 5 V supplies and reduced operating currents gives much lower power dissipation than devices operating from  $\pm 15$  V supplies.

### PRODUCT HIGHLIGHTS

1. Extended Signal Range  
The ADG608/ADG609 are fabricated on an enhanced LC<sup>2</sup>MOS process giving an increased signal range which extends to the supplies.
2. Low Power Dissipation
3. Low  $R_{ON}$
4. Fast Switching Times
5. Break-Before-Make Switching  
Switches are guaranteed break-before-make so that input signals are protected against momentary shorting.
6. Single/Dual Supply Operation

### ORDERING GUIDE

Model	Temperature Range	Package Option*
ADG608BN	-40°C to +85°C	N-16
ADG608BR	-40°C to +85°C	R-16A
ADG608BRU	-40°C to +85°C	RU-16
ADG608TRU	-55°C to +125°C	RU-16
ADG609BN	-40°C to +85°C	N-16
ADG609BR	-40°C to +85°C	R-16A
ADG609BRU	-40°C to +85°C	RU-16

\*N = Plastic DIP; RU = Thin Shrink Small Outline Package (TSSOP); R = 0.15" Small Outline IC (SOIC).

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# ADG608/ADG609–SPECIFICATIONS

DUAL SUPPLY<sup>1</sup> ( $V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = -5\text{ V} \pm 10\%$ ,  $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	B Version		T Version		Units	Test Conditions/ Comments
	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
<b>ANALOG SWITCH</b>						
Analog Signal Range		$V_{SS}$ to $V_{DD}$		$V_{SS}$ to $V_{DD}$	V	
$R_{ON}$	22 30		22 30	40	$\Omega$ typ $\Omega$ max	$-3.5\text{ V} \leq V_S \leq +3.5\text{ V}$ , $I_S = -1\text{ mA}$ ; $V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$ ; Test Circuit 1
$\Delta R_{ON}$	5	6	5	6	$\Omega$ max	$-3\text{ V} \leq V_S \leq +3\text{ V}$ , $I_{DS} = -1\text{ mA}$ ; $V_{DD} = +5\text{ V}$ , $V_{SS} = -5\text{ V}$
$R_{ON}$ Match	2	3	2	3	$\Omega$ max	$V_S = 0\text{ V}$ , $I_{DS} = -1\text{ mA}$ ; $V_{DD} = +5\text{ V}$ , $V_{SS} = -5\text{ V}$
<b>LEAKAGE CURRENTS</b>						
Source OFF Leakage $I_S$ (OFF)	$\pm 0.05$ $\pm 0.5$	$\pm 2$	$\pm 0.05$ $\pm 0.5$	$\pm 10$	nA typ nA max	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ $V_D = \pm 4.5\text{ V}$ , $V_S = \mp 4.5\text{ V}$ ; Test Circuit 2
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.05$ $\pm 0.5$	$\pm 2$ $\pm 1$	$\pm 0.05$ $\pm 0.5$	$\pm 10$ $\pm 5$	nA typ nA max nA max	$V_D = \pm 4.5\text{ V}$ , $V_S = \mp 4.5\text{ V}$ ; Test Circuit 3
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.05$ $\pm 0.5$	$\pm 3$	$\pm 0.05$ $\pm 0.5$	$\pm 20$	nA typ nA max	$V_S = V_D = \pm 4.5\text{ V}$ ; Test Circuit 4
ADG608	$\pm 0.5$	$\pm 1.5$	$\pm 0.5$	$\pm 10$	nA max	
ADG609	$\pm 0.5$	$\pm 1.5$	$\pm 0.5$	$\pm 10$	nA max	
<b>DIGITAL INPUTS</b>						
Input High Voltage, $V_{INH}$		2.4		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8		0.8	V max	
Input Current		$\pm 1$		$\pm 1$	$\mu\text{A}$ max	$V_{IN} = 0$ or $V_{DD}$
$I_{INL}$ or $I_{INH}$		$\pm 1$		$\pm 1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	5		5		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>						
$t_{TRANSITION}$	50 75	90	50 75	100	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = \pm 3.5\text{ V}$ , $V_{S8} = \mp 3.5\text{ V}$ ; Test Circuit 5
$t_{OPEN}$	10		10		ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +3.5\text{ V}$ ; Test Circuit 6
$t_{ON}$ (EN)	50 75	90	50 75	100	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +3.5\text{ V}$ ; Test Circuit 7
$t_{OFF}$ (EN)	30 45	60	30 45	75	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +3.5\text{ V}$ ; Test Circuit 7
Charge Injection	6		6		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 8
OFF Isolation	85		85		dB typ	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $f = 100\text{ kHz}$ ; $V_S = 3\text{ V rms}$ ; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $f = 100\text{ kHz}$ ; Test Circuit 10
$C_S$ (OFF)	9		9		pF typ	
$C_D$ (OFF)						
ADG608	40		40		pF typ	
ADG609	20		20		pF typ	
$C_D$ (ON)						
ADG608	54		54		pF typ	
ADG609	34		34		pF typ	
<b>POWER REQUIREMENTS</b>						
$I_{DD}$	0.05 0.2	0.2 2	0.05 0.2	0.2 2	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = 0\text{ V}$ or $V_{DD}$
$I_{SS}$	0.01 0.1	0.1 1	0.01 0.1	0.1 1	$\mu\text{A}$ typ $\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; T Version:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**SINGLE SUPPLY<sup>1</sup>** ( $V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	B Version		T Version		Units	Test Conditions/ Comments
	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
<b>ANALOG SWITCH</b>						
Analog Signal Range		0 to $V_{DD}$		0 to $V_{DD}$	V	
$R_{ON}$	40		40		$\Omega$ typ	$V_S = +3.5\text{ V}$ , $I_S = -1\text{ mA}$ ;
	50	60	50	70	$\Omega$ max	$V_{DD} = +4.5\text{ V}$ ;
$\Delta R_{ON}$	5	6	5	6	$\Omega$ max	Test Circuit 1
$R_{ON}$ Match	2	3	2	3	$\Omega$ max	+1 V $\leq V_S \leq$ +3 V, $I_{DS} = -1\text{ mA}$ ;
						$V_{DD} = +5\text{ V}$
						$V_S = 0\text{ V}$ , $I_{DS} = -1\text{ mA}$ ;
						$V_{DD} = +5\text{ V}$
<b>LEAKAGE CURRENTS</b>						
Source OFF Leakage $I_S$ (OFF)	$\pm 0.05$		$\pm 0.05$		nA typ	$V_{DD} = +5.5\text{ V}$
	$\pm 0.5$	$\pm 2$	$\pm 0.5$	$\pm 10$	nA max	$V_D = 4.5\text{ V}/0.1\text{ V}$ , $V_S = 0.1\text{ V}/4.5\text{ V}$ ;
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.05$		$\pm 0.05$		nA typ	Test Circuit 2
ADG608	$\pm 0.5$	$\pm 2$	$\pm 0.5$	$\pm 10$	nA max	$V_D = 4.5\text{ V}/0.1\text{ V}$ , $V_S = 0.1\text{ V}/4.5\text{ V}$ ;
ADG609	$\pm 0.5$	$\pm 1$	$\pm 0.5$	$\pm 5$	nA max	Test Circuit 3
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.05$		$\pm 0.05$		nA typ	$V_S = V_D = 4.5\text{ V}/0.1\text{ V}$ ;
ADG608	$\pm 0.5$	$\pm 3$	$\pm 0.5$	$\pm 20$	nA max	Test Circuit 4
ADG609	$\pm 0.5$	$\pm 1.5$	$\pm 0.5$	$\pm 10$	nA max	
<b>DIGITAL INPUTS</b>						
Input High Voltage, $V_{INH}$		2.4		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8		0.8	V max	
Input Current						
$I_{INL}$ or $I_{INH}$		$\pm 1$		$\pm 1$	$\mu\text{A}$ max	$V_{IN} = 0$ or $V_{DD}$
$C_{IN}$ , Digital Input Capacitance	5		5		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>						
$t_{TRANSITION}$	80		80		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ;
	100	130	100	150	ns max	$V_{S1} = 3.5\text{ V}/0\text{ V}$ , $V_{S8} = 0\text{ V}/3.5\text{ V}$ ;
						Test Circuit 5
$t_{OPEN}$	10		10		ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ;
						$V_S = +3.5\text{ V}$ ; Test Circuit 6
$t_{ON}$ (EN)	80		80		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ;
	100	130	100	150	ns max	$V_S = +3.5\text{ V}$ ; Test Circuit 7
$t_{OFF}$ (EN)	40		40		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ;
	50	60	50	75	ns max	$V_S = +3.5\text{ V}$ ; Test Circuit 7
Charge Injection	0.5		0.5		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ;
	3		3		pC max	Test Circuit 8
OFF Isolation	85		85		dB typ	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $f = 100\text{ kHz}$ ;
						$V_S = 1.5\text{ V rms}$ ; Test Circuit 9
Channel-to-Channel Crosstalk	85		85		dB typ	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $f = 100\text{ kHz}$ ;
						Test Circuit 10
$C_S$ (OFF)	9		9		pF typ	
$C_D$ (OFF)						
ADG608	40		40		pF typ	
ADG609	20		20		pF typ	
$C_D$ (ON)						
ADG608	54		54		pF typ	
ADG609	34		34		pF typ	
<b>POWER REQUIREMENTS</b>						
$I_{DD}$	0.05	0.2	0.05	0.2	$\mu\text{A}$ typ	$V_{IN} = 0\text{ V}$ or $V_{DD}$
	0.2	2	0.2	2	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature ranges are as follows: B Version: -40°C to +85°C; T Version: -55°C to +125°C.

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG608/ADG609–SPECIFICATIONS

## SINGLE SUPPLY<sup>1</sup> ( $V_{DD} = +3.3\text{ V} \pm 10\%$ , $V_{SS} = 0\text{ V}$ , $GND = 0\text{ V}$ , unless otherwise noted)

Parameter	B Version		T Version		Units	Test Conditions/ Comments
	+25°C	-40°C to +85°C	+25°C	-55°C to +125°C		
<b>ANALOG SWITCH</b>						
Analogue Signal Range		0 to $V_{DD}$		0 to $V_{DD}$	V	
$R_{ON}$	60		60		$\Omega$ typ	$V_S = +1.5\text{ V}$ , $I_S = -1\text{ mA}$ ; $V_{DD} = +3\text{ V}$ ; Test Circuit 1 $V_S = 0\text{ V}$ , $I_{DS} = -1\text{ mA}$ , $V_{DD} = +3.3\text{ V}$
	90	100	90	120	$\Omega$ max	
$R_{ON}$ Match	3	3	3	3	$\Omega$ max	
<b>LEAKAGE CURRENTS</b>						
Source OFF Leakage $I_S$ (OFF)	$\pm 0.05$		$\pm 0.05$		nA typ	$V_{DD} = +3.6\text{ V}$ $V_D = 2.6\text{ V}/0.1\text{ V}$ , $V_S = 0.1\text{ V}/2.6\text{ V}$ ; Test Circuit 2
	$\pm 0.5$	$\pm 2$	$\pm 0.5$	$\pm 10$	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.05$		$\pm 0.05$		nA typ	$V_D = 2.6\text{ V}/0.1\text{ V}$ , $V_S = 0.1\text{ V}/2.6\text{ V}$ ; Test Circuit 3
ADG608	$\pm 0.5$	$\pm 2$	$\pm 0.5$	$\pm 10$	nA max	
ADG609	$\pm 0.5$	$\pm 1$	$\pm 0.5$	$\pm 5$	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.05$		$\pm 0.05$		nA typ	$V_S = V_D = 2.6\text{ V}/0.1\text{ V}$ ; Test Circuit 4
ADG608	$\pm 0.5$	$\pm 3$	$\pm 0.5$	$\pm 20$	nA max	
ADG609	$\pm 0.5$	$\pm 1.5$	$\pm 0.5$	$\pm 10$	nA max	
<b>DIGITAL INPUTS</b>						
Input High Voltage, $V_{INH}$		2.4		2.4	V min	$V_{IN} = 0$ or $V_{DD}$
Input Low Voltage, $V_{INL}$		0.8		0.8	V max	
Input Current					$\mu\text{A}$ max	
$I_{INL}$ or $I_{INH}$		$\pm 1$		$\pm 1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	5		5		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>						
$t_{TRANSITION}$	120		120		ns typ	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_{S1} = 1.5\text{ V}/0\text{ V}$ , $V_{S8} = 0\text{ V}/1.5\text{ V}$ ; Test Circuit 5
	170	225	170	250	ns max	
$t_{OPEN}$	10		10		ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +1.5\text{ V}$ ; Test Circuit 6
$t_{ON}$ (EN)	120		120		ns typ	
	170	225	170	250	ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +1.5\text{ V}$ ; Test Circuit 7
$t_{OFF}$ (EN)	40		40		ns typ	
	60	75	60	90	ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ ; $V_S = +1.5\text{ V}$ ; Test Circuit 7
Charge Injection	0.5		0.5		pC typ	
	3		3		pC max	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ ; Test Circuit 8
OFF Isolation	85		85		dB typ	
Channel-to-Channel Crosstalk	85		85		dB typ	$R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $f = 100\text{ kHz}$ ; $V_S = 1\text{ V rms}$ ; Test Circuit 9 $R_L = 1\text{ k}\Omega$ , $C_L = 15\text{ pF}$ , $f = 100\text{ kHz}$ ; Test Circuit 10
$C_S$ (OFF)	9		9		pF typ	
$C_D$ (OFF)						pF typ
ADG608	40		40		pF typ	
ADG609	20		20		pF typ	
$C_D$ (ON)						pF typ
ADG608	54		54		pF typ	
ADG609	34		34		pF typ	
<b>POWER REQUIREMENTS</b>						
$I_{DD}$	0.05	0.2	0.05	0.2	$\mu\text{A}$ typ	$V_{IN} = 0\text{ V}$ or $V_{DD}$
	0.2	2	0.2	2	$\mu\text{A}$ max	

### NOTES

<sup>1</sup>Temperature ranges are as follows: B Version:  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ; T Version:  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> .....	+13 V
V <sub>DD</sub> to GND .....	-0.3 V to +6.5 V
V <sub>SS</sub> to GND .....	+0.3 V to -6.5 V
Analog, Digital Inputs <sup>2</sup> .....	-0.3 V to V <sub>DD</sub> + 2 V
or 20 mA, Whichever Occurs First	
Continuous Current, S or D .....	20 mA
Peak Current, S or D .....	20 mA
(Pulsed at 1 ms, 10% Duty Cycle Max) .....	
Operating Temperature Range	
Industrial (B Version) .....	-40°C to +85°C
Extended (T Version) .....	-55°C to +125°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	+150°C
Plastic DIP Package	
θ <sub>JA</sub> , Thermal Impedance .....	117°C/W
Lead Temperature, Soldering (10 sec) .....	+260°C

## SOIC Package

θ <sub>JA</sub> , Thermal Impedance .....	77°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec) .....	+215°C
Infrared (15 sec) .....	+220°C

## TSSOP Package

θ <sub>JA</sub> , Thermal Impedance .....	158°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec) .....	+215°C
Infrared (15 sec) .....	+220°C

ESD Rating .....

## NOTES

<sup>1</sup>Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overtages at A, S, D or EN will be clamped by internal diodes. Current should be limited to the maximum ratings given.

**Table I. ADG608 Truth Table**

A2	A1	A0	EN	ON SWITCH
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

X = Don't Care

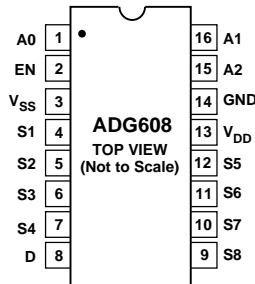
**Table II. ADG609 Truth Table**

A1	A0	EN	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

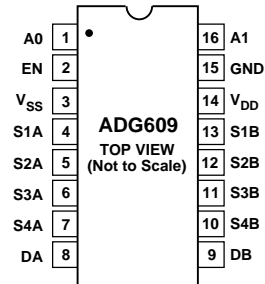
X = Don't Care

## PIN CONFIGURATIONS

### DIP/SOIC/TSSOP



### DIP/SOIC/TSSOP



# ADG608/ADG609—Typical Performance Characteristics



Figure 1.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Dual Supply Voltage



Figure 4.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ): Single Supply Voltage



Figure 2.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures



Figure 5.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures



Figure 3.  $R_{ON}$  as a Function of  $V_D$  ( $V_S$ ) for Different Temperatures



Figure 6. Leakage Currents as a Function of  $V_D$  ( $V_S$ )

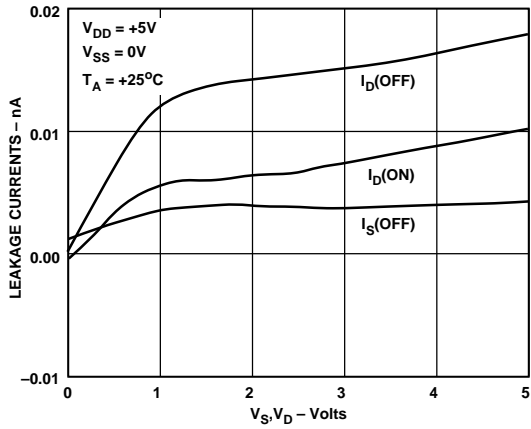


Figure 7. Leakage Currents as a Function of  $V_D$  ( $V_S$ )

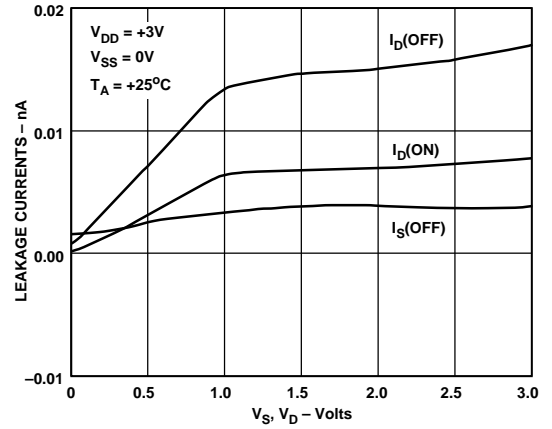


Figure 10. Leakage Currents as a Function of  $V_D$  ( $V_S$ )

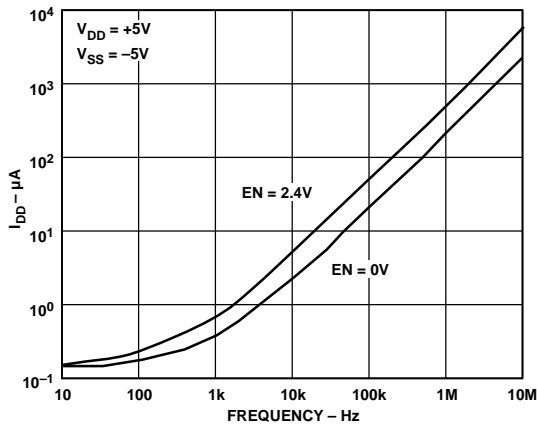


Figure 8. Positive Supply Current vs. Switching Frequency

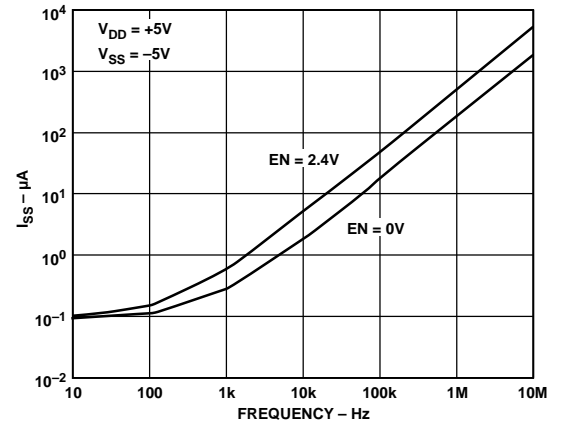


Figure 11. Negative Supply Current vs. Switching Frequency

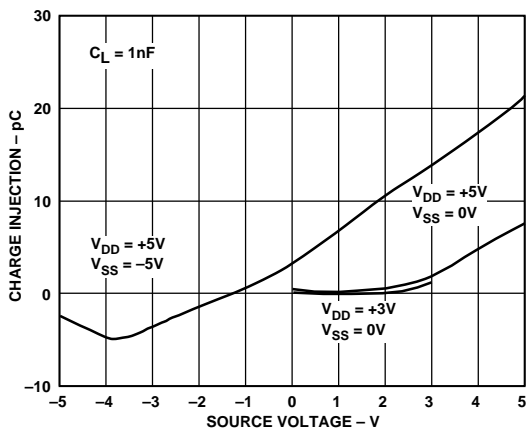


Figure 9. Charge Injection vs. Analog Voltage  $V_S$

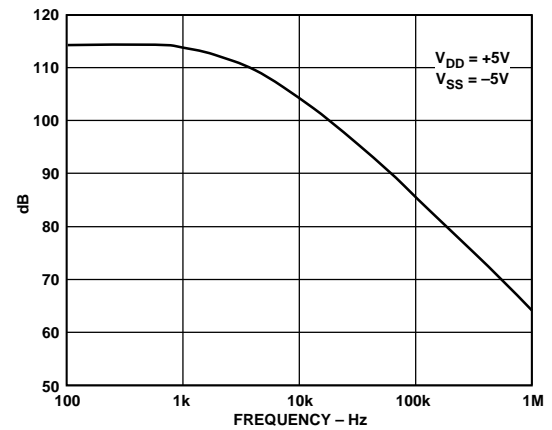
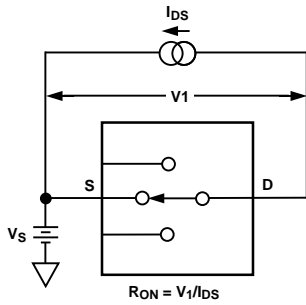


Figure 12. Crosstalk and Off Isolation vs. Frequency

# ADG608/ADG609

## Test Circuits



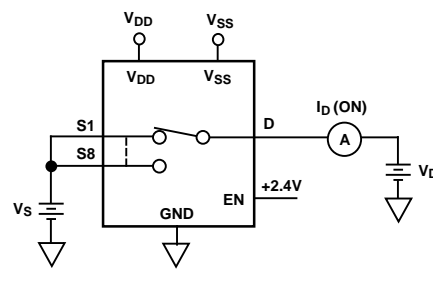
Test Circuit 1. On Resistance



Test Circuit 3.  $I_D$  (OFF)



Test Circuit 2.  $I_S$  (OFF)



Test Circuit 4.  $I_D$  (ON)

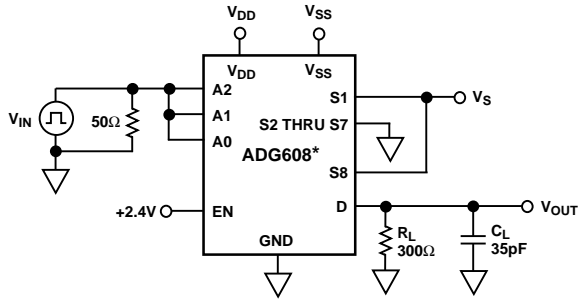


\* SIMILAR CONNECTION FOR ADG609



Test Circuit 5. Switching Time of Multiplexer,  $t_{TRANSITION}$





\* SIMILAR CONNECTION FOR ADG609



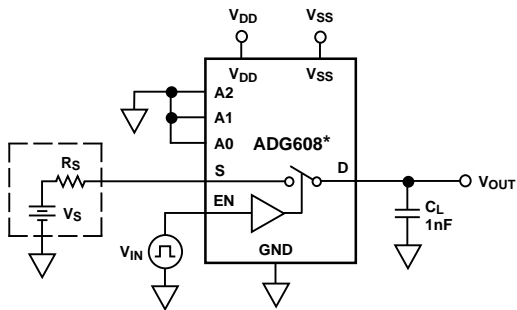
Test Circuit 6. Break-Before-Make Delay,  $t_{OPEN}$



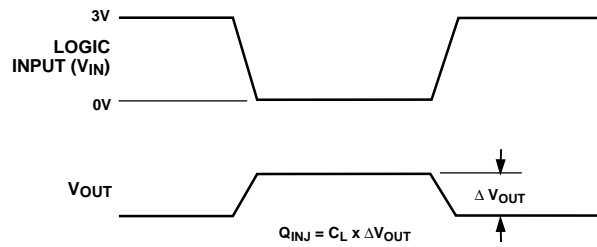
\* SIMILAR CONNECTION FOR ADG609



Test Circuit 7. Enable Delay,  $t_{ON}(EN)$ ,  $t_{OFF}(EN)$



\* SIMILAR CONNECTION FOR ADG609

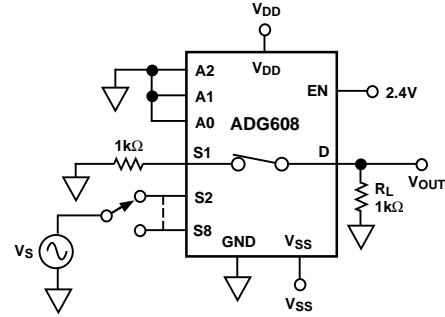


Test Circuit 8. Charge Injection

# ADG608/ADG609



Test Circuit 9. OFF Isolation



Test Circuit 10. Channel-to-Channel Crosstalk

## TERMINOLOGY

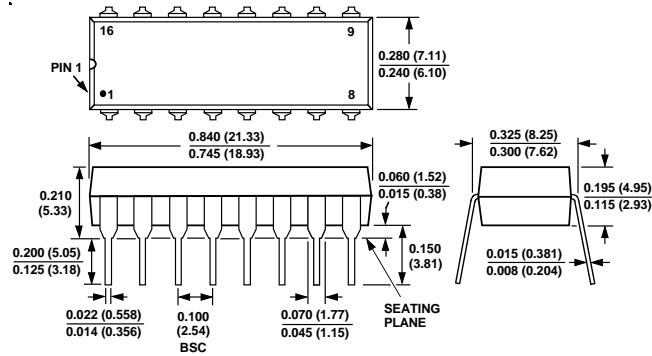
$V_{DD}$	Most positive power supply potential.
$V_{SS}$	Most negative power supply potential in dual supplies. In single supply applications, it may be connected to ground.
GND	Ground (0 V) reference.
$R_{ON}$	Ohmic resistance between D and S.
$\Delta R_{ON}$	$R_{ON}$ variation due to a change in the analog input voltage with a constant load current.
$R_{ON}$ Match	Difference between the $R_{ON}$ of any two channels.
$I_S$ (OFF)	Source leakage current when the switch is off.
$I_D$ (OFF)	Drain leakage current when the switch is off.
$I_D, I_S$ (ON)	Channel leakage current when the switch is on.
$V_D, V_S$	Analog voltage on terminals D, S.
$C_S$ (OFF)	Channel input capacitance for "OFF" condition.
$C_D$ (OFF)	Channel output capacitance for "OFF" condition.
$C_D, C_S$ (ON)	"ON" switch capacitance.
$C_{IN}$	Digital input capacitance.
$t_{ON}$ (EN)	Delay time between the 50% and 90% points of the digital input and switch "ON" condition.

$t_{OFF}$ (EN)	Delay time between the 50% and 90% points of the digital input and switch "OFF" condition.
$t_{TRANSITION}$	Delay time between the 50% and 90% points of the digital inputs and the switch "ON" condition when switching from one address state to another.
$t_{OPEN}$	"OFF" time measured between the 80% points of both switches when switching from one address state to another.
$V_{INL}$	Maximum input voltage for logic "0."
$V_{INH}$	Minimum input voltage for logic "1."
$I_{INL}$ ( $I_{INH}$ )	Input current of the digital input.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" channel.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
$I_{DD}$	Positive supply current.
$I_{SS}$	Negative supply current.

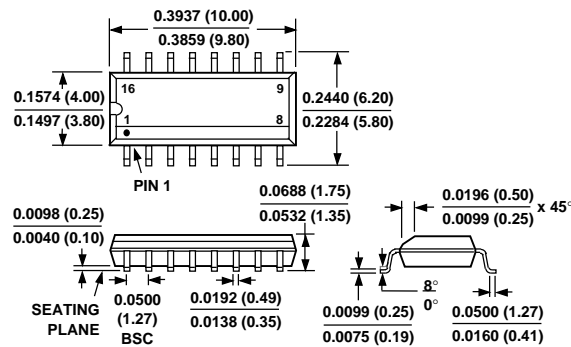
**OUTLINE DIMENSIONS**

Dimensions shown in inches and (mm).

**16-Pin Plastic (N-16)**



**16-Pin SOIC (R-16A)**



**16-Pin TSSOP (RU-16)**

