270 MHz, 400 μA Current Feedback Amplifier

AD8005

FEATURES

Ultralow Power
- 400 μA Power Supply Current (4 mW on ±5 V_S)
- Specified for Single Supply Operation

High Speed
- 270 MHz, –3 dB Bandwidth (G = +1)
- 170 MHz, –3 dB Bandwidth (G = +2)
- 280 V/μs Slew Rate (G = +2)
- 28 ns Settling Time to 0.1%, 2 V Step (G = +2)

Low Distortion/Noise
- –63 dBc @ 1 MHz, V_O = 2 V p-p
- –50 dBc @ 10 MHz, V_O = 2 V p-p
- 4.0 nV/$\sqrt{Hz}$ Input Voltage Noise @ 10 MHz

Good Video Specifications (R_L = 1 kΩ, G = +2)
- Gain Flatness 0.1 dB to 30 MHz
- 0.11% Differential Gain Error
- 0.4° Differential Phase Error

APPLICATIONS

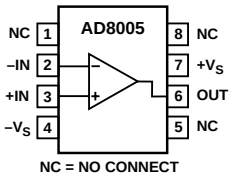
Signal Conditioning
A/D Buffer
Power-Sensitive, High-Speed Systems
- Battery Powered Equipment
- Loop/Remote Power Systems
- Communication or Video Test Systems
- Portable Medical Instruments

PRODUCT DESCRIPTION

The AD8005 is an ultralow power, high-speed amplifier with a wide signal bandwidth of 170 MHz and slew rate of 280 V/μs. This performance is achieved while consuming only 400 μA of quiescent supply current. These features increase the operating time of high-speed battery-powered systems without reducing dynamic performance.

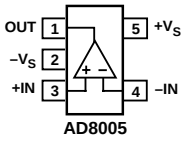
FUNCTIONAL BLOCK DIAGRAM

8-Lead Plastic DIP and SOIC



NC = NO CONNECT

5-Lead SOT-23



The current feedback design results in gain flatness of 0.1 dB to 30 MHz while offering differential gain and phase errors of 0.11% and 0.4°. Harmonic distortion is low over a wide bandwidth with THDs of –63 dBc at 1 MHz and –50 dBc at 10 MHz. Ideal features for a signal conditioning amplifier or buffer to a high-speed A-to-D converter in portable video, medical or communication systems.

The AD8005 is characterized for +5 V and ±5 V supplies and will operate over the industrial temperature range of –40°C to +85°C. The amplifier is supplied in 8-lead plastic DIP, 8-lead SOIC and 5-lead SOT-23 packages.

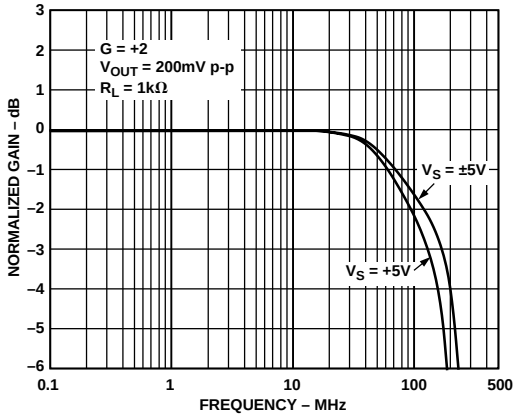


Figure 1. Frequency Response; G = +2, V_S = +5 V or ±5 V

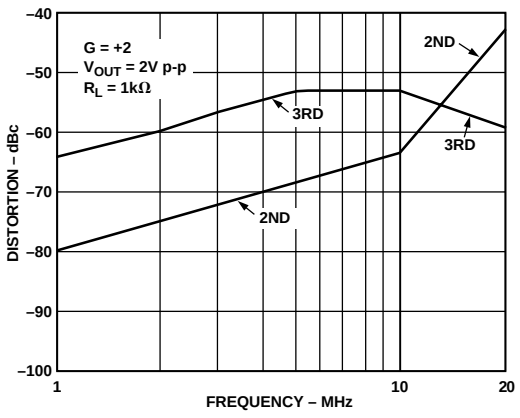


Figure 2. Distortion vs. Frequency; V_S = ±5 V

REV. A

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AD8005–SPECIFICATIONS

±5 V SUPPLIES (@ T_A = +25°C, V_S = ±5 V, R_L = 1 kΩ unless otherwise noted)

Parameter	Conditions	AD8005A Min	Typ	Max	Units
DYNAMIC PERFORMANCE	R_F = 3.01 kΩ for "N" Package or R_F = 2.49 kΩ for "R" Package or R_F = 2.10 kΩ for "RT" Package				
–3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	225	270		MHz
	G = +2, V_O = 0.2 V p-p	140	170		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p	10	30		MHz
Large Signal Bandwidth	G = +10, V_O = 4 V p-p, R_F = 499 Ω		40		MHz
Slew Rate (Rising Edge)	G = +2, V_O = 4 V Step		280		V/µs
	G = –1, V_O = 4 V Step, R_F = 1.5 kΩ		1500		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		28		ns
DISTORTION/NOISE PERFORMANCE	R_F = 3.01 kΩ for "N" Package or R_F = 2.49 kΩ for "R" Package or R_F = 2.10 kΩ for "RT" Package				
Total Harmonic Distortion	f_C = 1 MHz, V_O = 2 V p-p, G = +2		–63		dBc
	f_C = 10 MHz, V_O = 2 V p-p, G = +2		–50		dBc
Differential Gain	NTSC, G = +2		0.11		%
Differential Phase	NTSC, G = +2		0.4		Degrees
Input Voltage Noise	f = 10 MHz		4.0		nV/√Hz
Input Current Noise	f = 10 MHz, $+I_{IN}$		1.1		pA/√Hz
	$–I_{IN}$		9.1		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			5	30	±mV
	T_{MIN} to T_{MAX}			50	±mV
Offset Drift			40		µV/°C
+Input Bias Current			0.5	1	±µA
	T_{MIN} to T_{MAX}			2	±µA
–Input Bias Current			5	10	±µA
	T_{MIN} to T_{MAX}			12	±µA
Input Bias Current Drift (±)			6		nA/°C
Open-Loop Transimpedance		400	1000		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		90		MΩ
	–Input		260		Ω
Input Capacitance	+Input		1.6		pF
Input Common-Mode Voltage Range			3.8		±V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	46	54		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Positive	+3.7	+3.90		V
	Negative		–3.90	–3.7	V
Output Current	R_L = 50 Ω		10		mA
Short Circuit Current			60		mA
POWER SUPPLY					
Quiescent Current			400	475	µA
	T_{MIN} to T_{MAX}			560	µA
Power Supply Rejection Ratio	V_S = ±4 V to ±6 V	56	66		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

+5 V SUPPLY (@ T_A = +25°C, V_S = +5 V, R_L = 1 kΩ to 2.5 V unless otherwise noted)

Parameter	Conditions	AD8005A Min	AD8005A Typ	AD8005A Max	Units
DYNAMIC PERFORMANCE	R_F = 3.01 kΩ for "N" Package or R_F = 2.49 kΩ for "R" Package or R_F = 2.10 kΩ for "RT" Package				
–3 dB Small Signal Bandwidth	G = +1, V_O = 0.2 V p-p	190	225		MHz
	G = +2, V_O = 0.2 V p-p	110	130		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p	10	30		MHz
Large Signal Bandwidth	G = +10, V_O = 2 V p-p, R_F = 499 Ω		45		MHz
Slew Rate (Rising Edge)	G = +2, V_O = 2 V Step		260		V/µs
	G = –1, V_O = 2 V Step, R_F = 1.5 kΩ		775		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		30		ns
DISTORTION/NOISE PERFORMANCE	R_F = 3.01 kΩ for "N" Package or R_F = 2.49 kΩ for "R" Package or R_F = 2.10 kΩ for "RT" Package				
Total Harmonic Distortion	f_C = 1 MHz, V_O = 2 V p-p, G = +2		–60		dBc
	f_C = 10 MHz, V_O = 2 V p-p, G = +2		–50		dBc
Differential Gain	NTSC, G = +2, R_L to 1.5 V		0.14		%
Differential Phase	NTSC, G = +2, R_L to 1.5 V		0.70		Degrees
Input Voltage Noise	f = 10 MHz		4.0		nV/√Hz
Input Current Noise	f = 10 MHz, $+I_{IN}$		1.1		pA/√Hz
	$-I_{IN}$		9.1		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage			5	35	±mV
	T_{MIN} to T_{MAX}			50	±mV
Offset Drift			40		µV/°C
+Input Bias Current			0.5	1	±µA
	T_{MIN} to T_{MAX}			2	±µA
–Input Bias Current			5	10	±µA
	T_{MIN} to T_{MAX}			11	±µA
Input Bias Current Drift (±)			8		nA/°C
Open-Loop Transimpedance		50	500		kΩ
INPUT CHARACTERISTICS					
Input Resistance	+Input		120		MΩ
	–Input		300		Ω
Input Capacitance	+Input		1.6		pF
Input Common-Mode Voltage Range			1.5 to 3.5		V
Common-Mode Rejection Ratio	V_{CM} = 1.5 V to 3.5 V	48	54		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing		1.1 to 3.9	0.95 to 4.05		V
Output Current	R_L = 50 Ω		10		mA
Short Circuit Current			30		mA
POWER SUPPLY					
Quiescent Current			350	425	µA
	T_{MIN} to T_{MAX}			475	µA
Power Supply Rejection Ratio	V_S = +4 V to +6 V	56	66		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage . . . . . 12.6 V
Internal Power Dissipation[2]
Plastic DIP Package (N) . . . . . 1.3 Watts
Small Outline Package (R) . . . . . 0.75 Watts
SOT-23-5 Package (RT) . . . . . 0.5 Watts
Input Voltage (Common Mode) . . . . . $\pm V_S \pm 1$ V
Differential Input Voltage . . . . . ±3.5 V
Output Short Circuit Duration
. . . . . Observe Power Derating Curves
Storage Temperature Range
N, R & RT Package . . . . . –65°C to +125°C
Operating Temperature Range (A Grade) . . . –40°C to +85°C
Lead Temperature Range (Soldering 10 sec) . . . . . +300°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Specification is for device in free air:
8-Lead Plastic DIP Package: θ_{JA} = 90°C/W
8-Lead SOIC Package: θ_{JA} = 155°C/W
5-Lead SOT-23 Package: θ_{JA} = 240°C/W

MAXIMUM POWER DISSIPATION

The maximum power that can be safely dissipated by the AD8005 is limited by the associated rise in junction temperature. The maximum safe junction temperature for plastic encapsulated devices is determined by the glass transition temperature of the plastic, approximately +150°C. Exceeding this limit temporarily may cause a shift in parametric performance due to a change in the stresses exerted on the die by the package. Exceeding a junction temperature of +175°C for an extended period can result in device failure.

While the AD8005 is internally short circuit protected, this may not be sufficient to guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. To ensure proper operation, it is necessary to observe the maximum power derating curves shown in Figure 3.

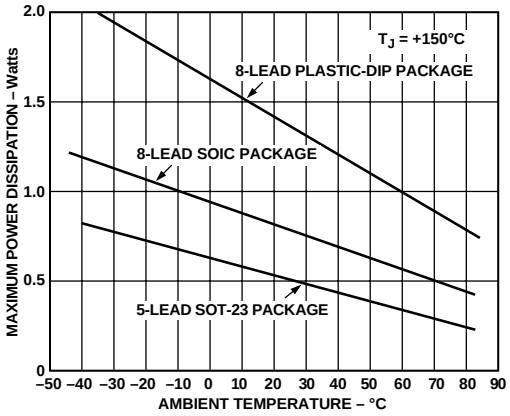


Figure 3. Maximum Power Dissipation vs. Temperature

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Brand Code
AD8005AN	–40°C to +85°C	8-Lead Plastic DIP	N-8	
AD8005AR	–40°C to +85°C	8-Lead Plastic SOIC	SO-8	
AD8005AR-REEL	–40°C to +85°C	13" Tape and Reel	SO-8	
AD8005ART-REEL	–40°C to +85°C	13" Tape and Reel	RT-5	H1A
AD8005AR-REEL7	–40°C to +85°C	7" Tape and Reel	SO-8	
AD8005ART-REEL7	–40°C to +85°C	7" Tape and Reel	RT-5	H1A

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8005 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

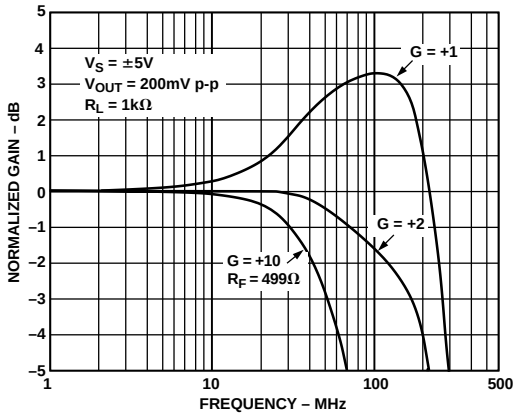


Figure 4. Frequency Response; G = +1, +2, +10; V_S = ±5 V

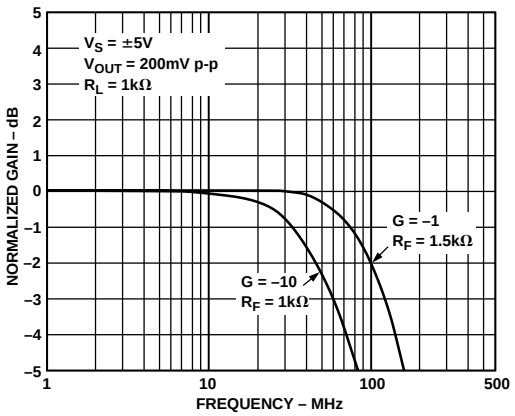


Figure 7. Frequency Response; G = –1, –10; V_S = ±5 V

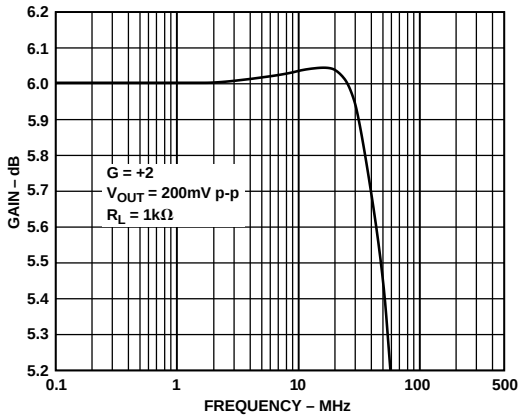


Figure 5. Gain Flatness; G = +2; V_S = ±5 V or +5 V

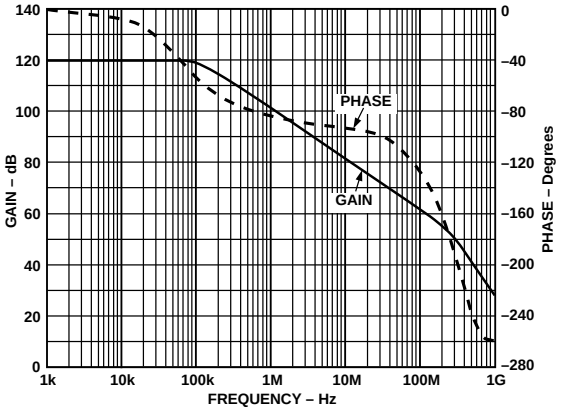


Figure 8. Transimpedance Gain and Phase vs. Frequency

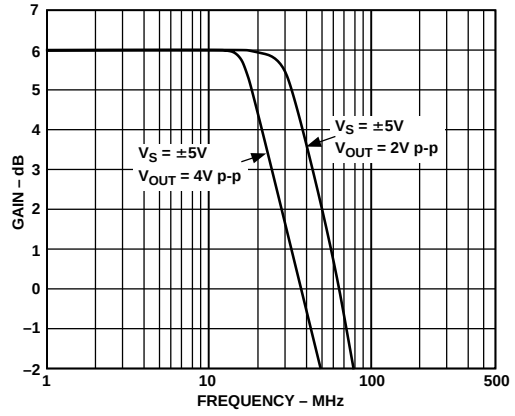


Figure 6. Large Signal Frequency Response; G = +2, R_L = 1 kΩ

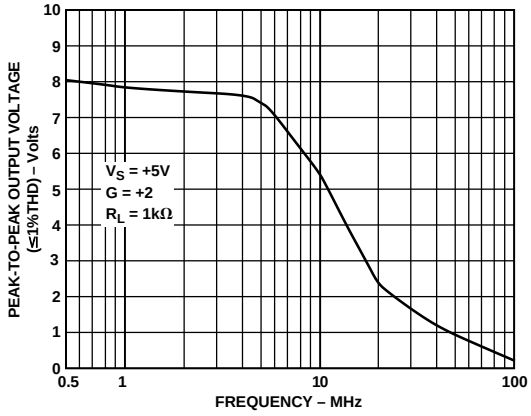


Figure 9. Output Swing vs. Frequency; V_S = ±5 V

AD8005–Typical Characteristics

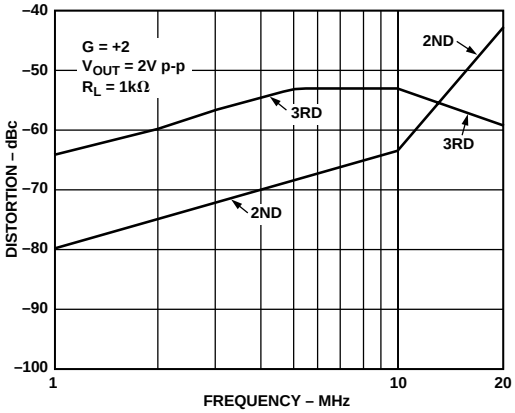


Figure 10. Distortion vs. Frequency; V_S = ±5 V

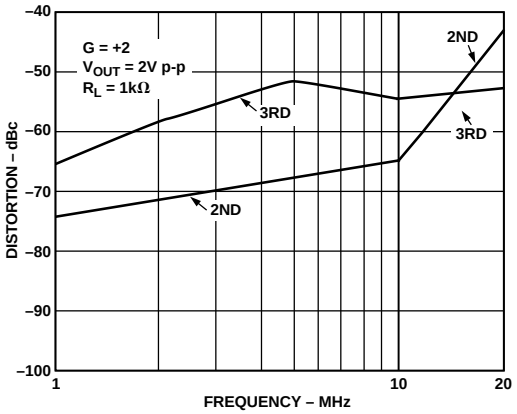


Figure 13. Distortion vs. Frequency V_S = +5 V

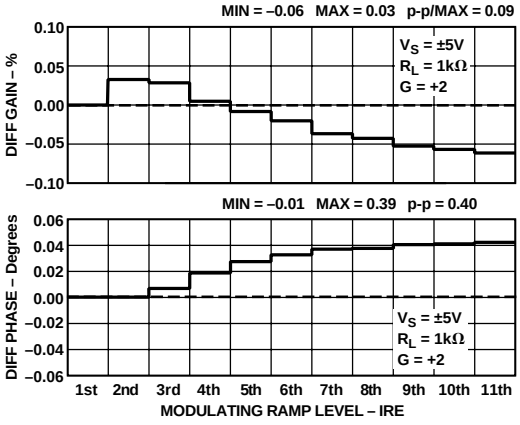


Figure 11. Differential Gain and Phase, V_S = ±5 V

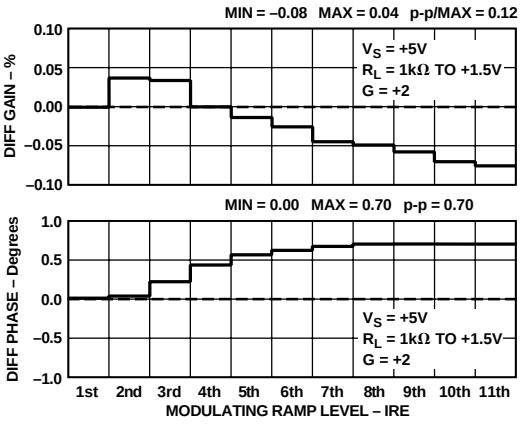


Figure 14. Differential Gain and Phase, V_S = +5 V

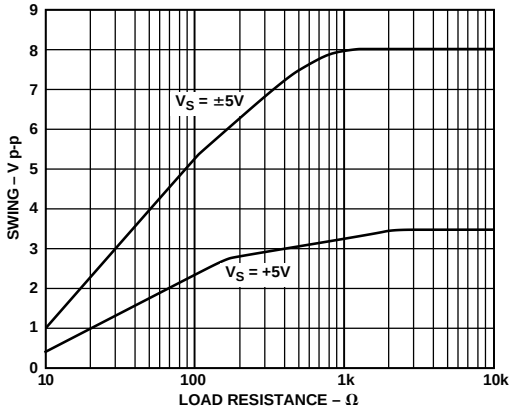


Figure 12. Output Voltage Swing vs. Load

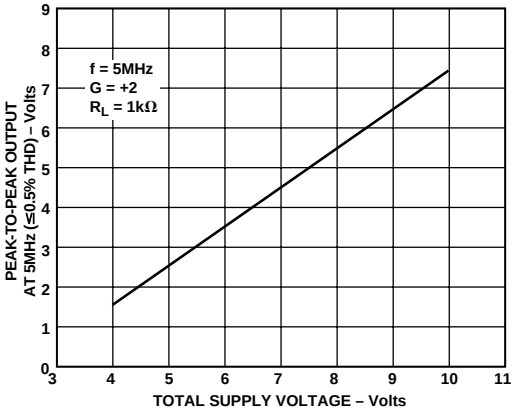


Figure 15. Output Swing vs. Supply

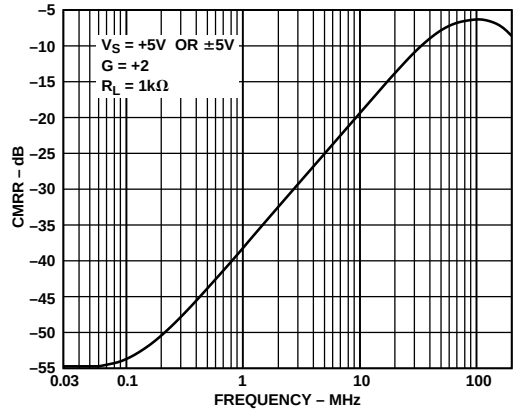


Figure 16. CMRR vs. Frequency; V_S = +5 V or ±5 V

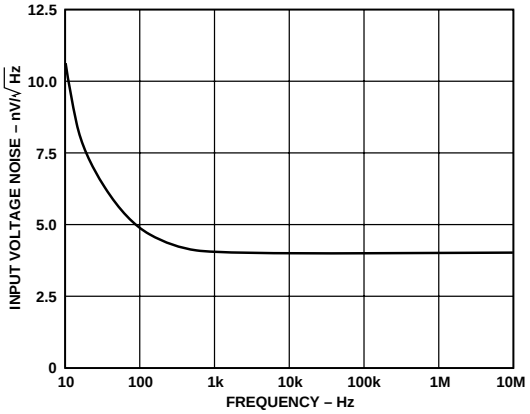


Figure 19. Noise vs. Frequency; V_S = +5 V or ±5 V

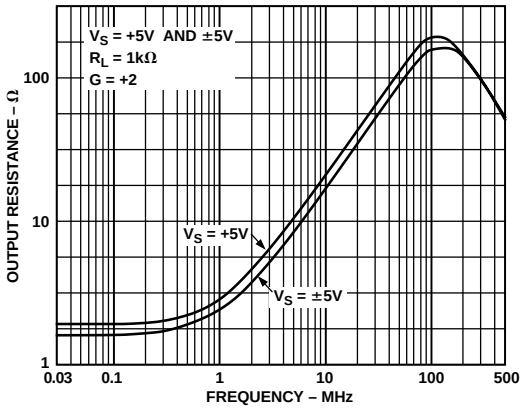


Figure 17. Output Resistance vs. Frequency; V_S = ±5 V and +5 V

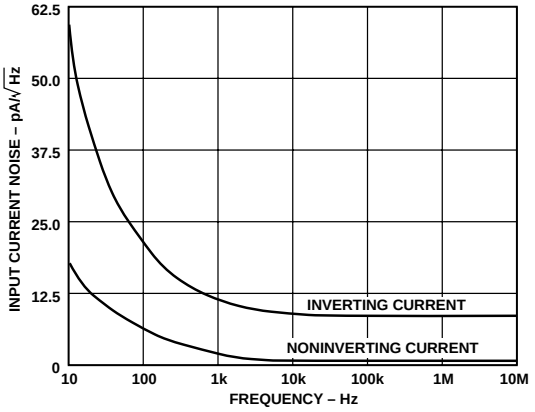


Figure 20. Noise vs. Frequency; V_S = +5 V or ±5 V

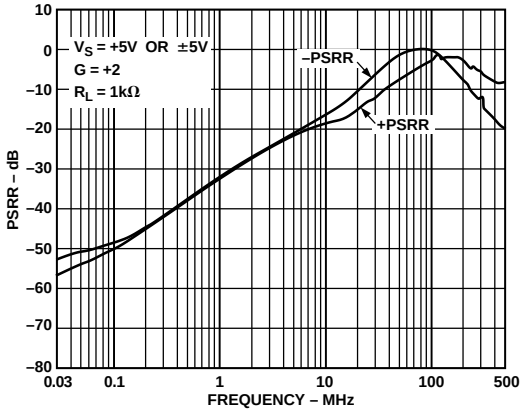


Figure 18. PSRR vs. Frequency; V_S = +5 V or ±5 V

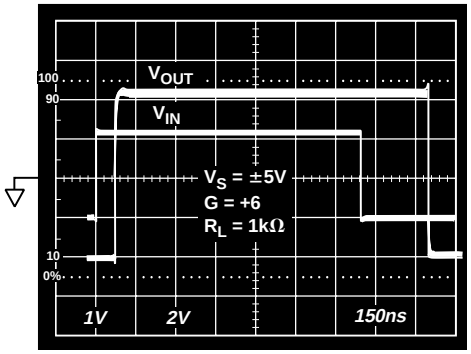


Figure 21. ±Overdrive Recovery, V_S = ±5 V, V_{IN} = 2 V Step

AD8005–Typical Characteristics

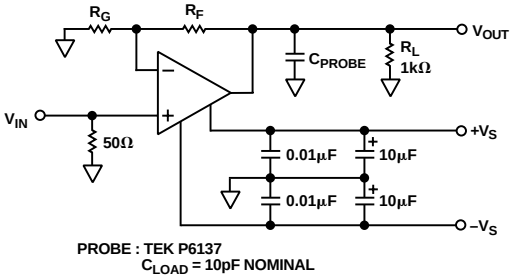


Figure 22. Test Circuit; G = +2; R_F = R_G = 3.01 kΩ for N Package; R_F = R_G = 2.49 kΩ for R and RT Packages

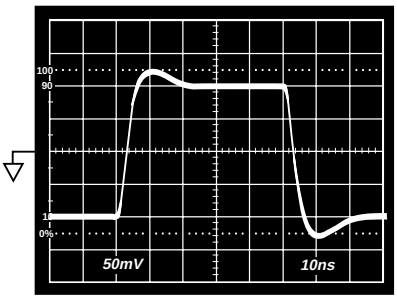


Figure 23. 200 mV Step Response; G = +2, V_S = ±2.5 V or ±5 V

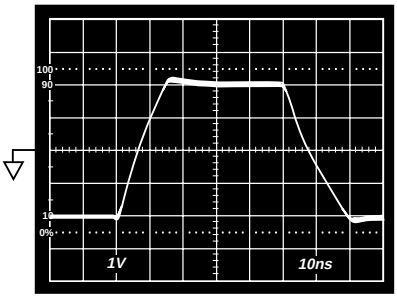


Figure 24. Step Response; G = +2, V_S = ±5 V

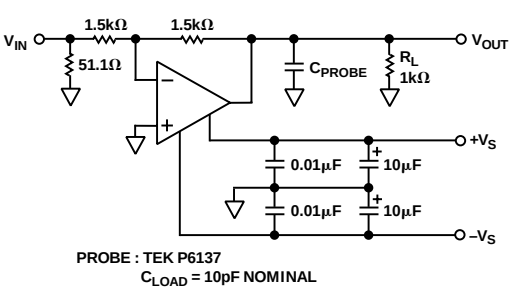


Figure 25. Test Circuit; G = –1, R_F = R_G = 1.5 kΩ for N, R and RT Packages

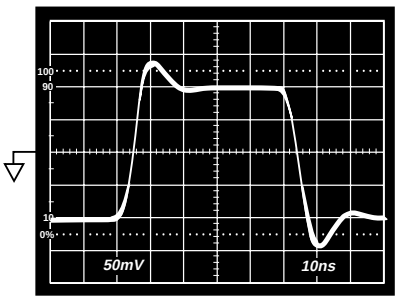


Figure 26. 200 mV Step Response; G = –1, V_S = ±2.5 V or ±5 V

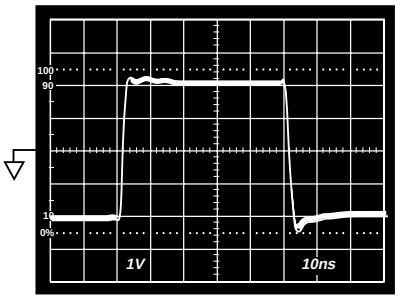


Figure 27. Step Response; G = –1, V_S = ±5 V

APPLICATIONS

Driving Capacitive Loads

Capacitive loads interact with an op amp's output impedance to create an extra delay in the feedback path. This reduces circuit stability, and can cause unwanted ringing and oscillation. A given value of capacitance causes much less ringing when the amplifier is used with a higher noise gain.

The capacitive load drive of the AD8005 can be increased by adding a low valued resistor in series with the capacitive load. Introducing a series resistor tends to isolate the capacitive load from the feedback loop thereby diminishing its influence. Figure 29 shows the effects of a series resistor on capacitive drive for varying voltage gains. As the closed-loop gain is increased, the larger phase margin allows for larger capacitive loads with less overshoot. Adding a series resistor at lower closed-loop gains accomplishes the same effect. For large capacitive loads, the frequency response of the amplifier will be dominated by the roll-off of the series resistor and capacitive load.

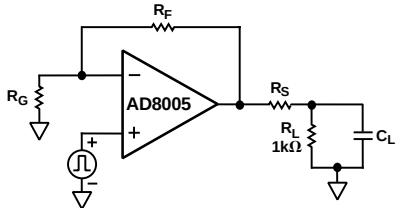


Figure 28. Driving Capacitive Loads

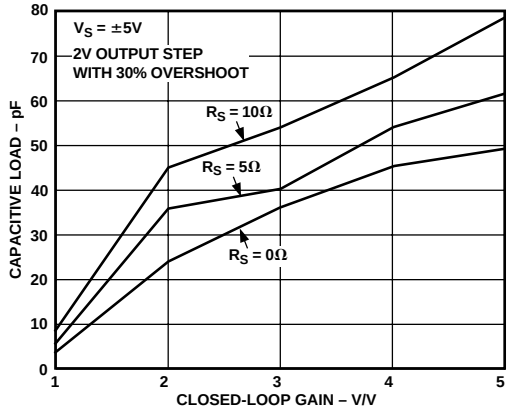


Figure 29. Capacitive Load Drive vs. Closed-Loop Gain

Single-Supply Level Shifter

In addition to providing buffering, many systems require that an op amp provide level shifting. A common example is the level shifting that is required to move a bipolar signal into the unipolar range of many modern analog-to-digital converters (ADCs). In general, single supply ADCs have input ranges that are referenced neither to ground nor supply. Instead the reference level is some point in between, usually halfway between ground and supply (+2.5 V for a single supply 5 V ADC). Because high-speed ADCs typically have input voltage ranges of 1 V to 2 V, the op amp driving it must be single supply but not necessarily rail-to-rail.

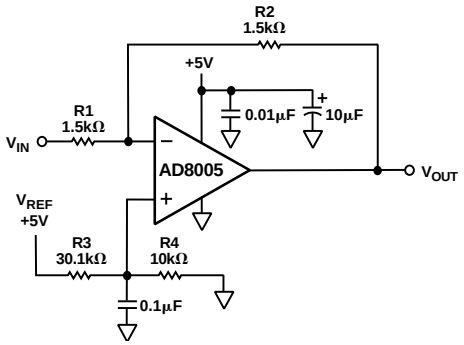


Figure 30. Bipolar to Unipolar Level Shifter

Figure 30 shows a level shifter circuit that can move a bipolar signal into a unipolar range. A positive reference voltage, derived from the +5 V supply, sets a bias level of +1.25 V at the noninverting terminal of the op amp. In ac applications, the accuracy of this voltage level is not important. Noise is however a serious consideration. A 0.1 μF capacitor provides useful decoupling of this noise.

The bias level on the noninverting terminal sets the input common-mode voltage to +1.25 V. Because the output will always be positive, the op amp may therefore be powered with a single +5 V power supply.

The overall gain function is given by the equation:

$$V_{OUT} = -\left(\frac{R2}{R1}\right) V_{IN} + \left(\frac{R4}{R3+R4}\right)\left(1+\frac{R2}{R1}\right) V_{REF}$$

In the above example, the equation simplifies to

$$V_{OUT} = -V_{IN} + 2.5V$$

Single-Ended-to-Differential Conversion

Many single supply ADCs have differential inputs. In such cases, the ideal common-mode operating point is usually halfway between supply and ground. Figure 31 shows how to convert a single-ended bipolar signal into a differential signal with a common-mode level of 2.5 V.

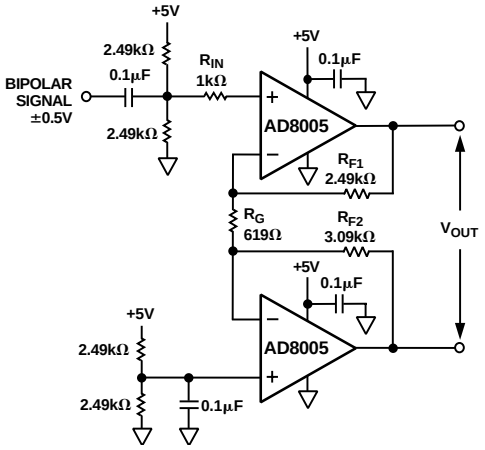


Figure 31. Single-Ended-to-Differential Converter

Amp 1 has its +input driven with the ac-coupled input signal while the +input of Amp 2 is connected to a bias level of +2.5 V. Thus the –input of Amp 2 is driven to virtual +2.5 V by its output. Therefore, Amp 1 is configured for a noninverting gain of five, $(1 + R_{F1}/R_G)$, because RG is connected to the virtual +2.5 V of Amp 2's –input.

When the +input of Amp 1 is driven with a signal, the same signal appears at the –input of Amp 1. This signal serves as an input to Amp 2 configured for a gain of –5, $(-R_{F2}/R_G)$. Thus the two outputs move in opposite directions with the same gain and create a balanced differential signal.

This circuit can be simplified to create a bipolar in/bipolar out single-ended to differential converter. Obviously, a single supply is no longer adequate and the $-V_S$ pins must now be powered with –5 V. The +input to Amp 2 is tied to ground. The ac coupling on the +input of Amp 1 is removed and the signal can be fed directly into Amp 1.

Layout Considerations

In order to achieve the specified high-speed performance of the AD8005 you must be attentive to board layout and component selection. Proper R_F design techniques and selection of components with low parasitics are necessary.

The PCB should have a ground plane that covers all unused portions of the component side of the board. This will provide a low impedance path for signals flowing to ground. The ground plane should be removed from the area under and around the chip (leave about 2 mm between the pin contacts and the ground plane). This helps to reduce stray capacitance. If both signal tracks and the ground plane are on the same side of the PCB, also leave a 2 mm gap between ground plane and track.

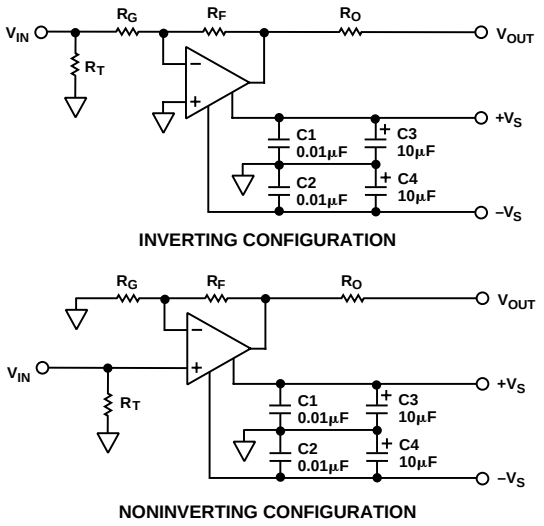


Figure 32. Inverting and Noninverting Configurations

Chip capacitors have low parasitic resistance and inductance and are suitable for supply bypassing (see Figure 32). Make sure that one end of the capacitor is within 1/8 inch of each power pin with the other end connected to the ground plane. An additional large (0.47 μF–10 μF) tantalum electrolytic capacitor should also be connected in parallel. This capacitor supplies current for fast, large signal changes at the output. It must not necessarily be as close to the power pin as the smaller capacitor.

Locate the feedback resistor close to the inverting input pin in order to keep the stray capacitance at this node to a minimum. Capacitance variations of less than 1.5 pF at the inverting input will significantly affect high-speed performance.

Use stripline design techniques for long signal traces (i.e., greater than about 1 inch). Striplines should have a characteristic impedance of either 50 Ω or 75 Ω. For the Stripline to be effective, correct termination at both ends of the line is necessary.

Table I. Typical Bandwidth vs. Gain Setting Resistors

Gain	R_F	R_G	R_T	Small Signal –3 dB BW (MHz), V_S = ±5 V
–1	1.49 kΩ	1.49 kΩ	52.3	120 MHz
–10	1 kΩ	100 Ω	100 Ω	60 MHz
+1	2.49 kΩ	∞	49.9 Ω	270 MHz
+2	2.49 kΩ	2.49 kΩ	49.9 Ω	170 MHz
+10	499 Ω	56.2 Ω	49.9 Ω	40 MHz

Increasing Feedback Resistors

Unlike conventional voltage feedback op amps, the choice of feedback resistor has a direct impact on the closed-loop bandwidth and stability of a current feedback op amp circuit. Reducing the resistance below the recommended value makes the amplifier more unstable. Increasing the size of the feedback resistor reduces the closed-loop bandwidth.

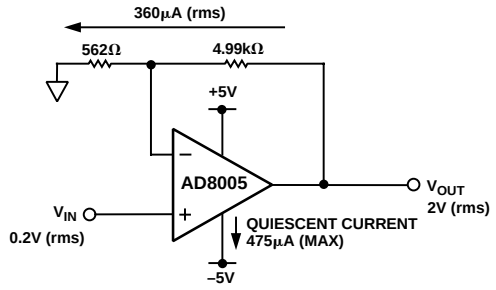


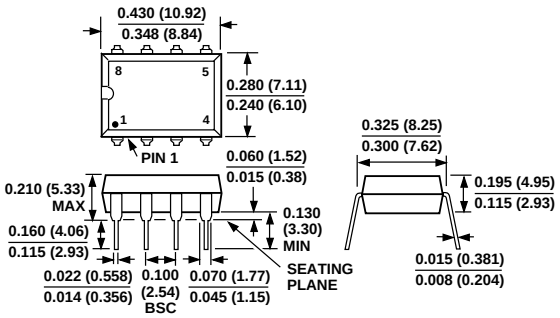
Figure 33. Saving Power by Increasing Feedback Resistor Network

In power-critical applications where some bandwidth can be sacrificed, increasing the size of the feedback resistor will yield significant power savings. A good example of this is the gain of +10 case. Operating from a bipolar supply (±5 V), the quiescent current is 475 μA (excluding the feedback network). The recommended feedback and gain resistors are 499 Ω and 56.2 Ω respectively. In order to drive an rms output voltage of 2 V, the output must deliver a current of 3.6 mA to the feedback network. Increasing the size of the resistor network by a factor of 10 as shown in Figure 33 will reduce this current to 360 μA. The closed loop bandwidth will however decrease to 20 MHz.

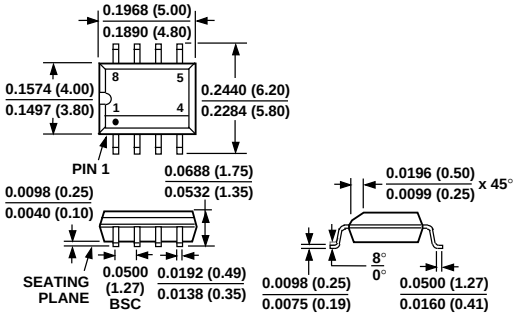
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

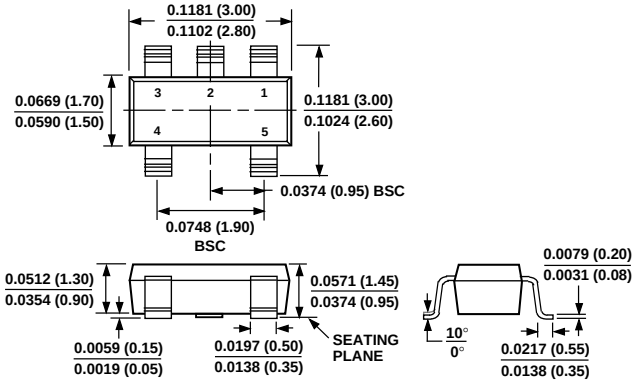
8-Lead Plastic DIP
(N-8)



8-Lead Plastic SOIC
(SO-8)



5-Lead Plastic SOT-23
(RT-5)



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