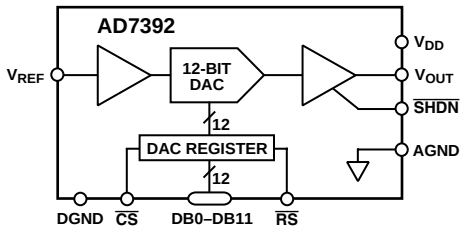
+3 V, Parallel Input Micropower 10- and 12-Bit DACs

AD7392/AD7393

FEATURES
Micropower: 100 μA
0.1 μA Typical Power Shutdown
Single-Supply +2.7 V to +5.5 V Operation
Compact 1.1 mm Height TSSOP-20 Package
AD7392/12-Bit Resolution
AD7393/10-Bit Resolution
0.9 LSB Differential Nonlinearity Error

APPLICATIONS
Automotive 0.5 V to 4.5 V Output Span Voltage
Portable Communications
Digitally Controlled Calibration
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7392/AD7393 family of 10- and 12-bit voltage-output digital-to-analog converters is designed to operate from a single +3 V supply. Built using a CBCMOS process, these monolithic DACs offer the user low cost and ease of use in single-supply +3 V systems. Operation is guaranteed over the supply voltage range of +2.7 V to +5.5 V, making this device ideal for battery operated applications.

The full-scale voltage output is determined by the external reference input voltage applied. The rail-to-rail REF_{IN} to DAC_{OUT} allows for a full-scale voltage set equal to the positive supply V_{DD} or any value in between. The voltage outputs are capable of sourcing 5 mA.

A 12-bit wide data latch loads with a 45 ns write time allowing interface to the fastest processors without wait states.

Additionally, an asynchronous $\overline{RS}$ input sets the output to zero scale at power on or upon user demand.

Both parts are offered in the same pinout to allow users to select the amount of resolution appropriate for their applications without circuit card changes.

The AD7392/AD7393 are specified for operation over the extended industrial (–40°C to +85°C) temperature range. The AD7393AR is specified for the –40°C to +125°C automotive temperature range. AD7392/AD7393s are available in plastic DIP, and 20-lead SOIC packages. The AD7393ARU is available for ultracompact applications in a thin 1.1 mm height TSSOP-20 package.

For serial data input, 8-lead packaged versions, see the AD7390 and AD7391 products.

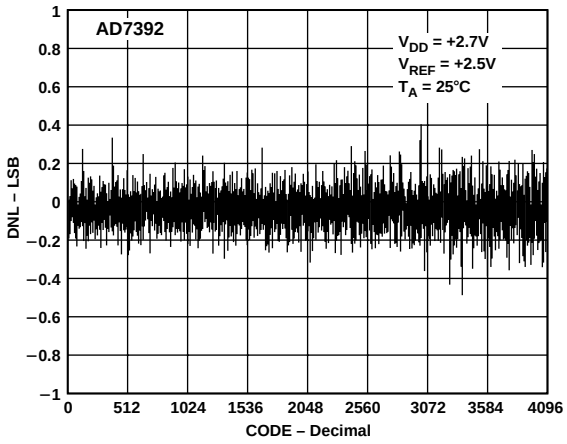


Figure 1. AD7392 Differential Nonlinearity Error vs. Code

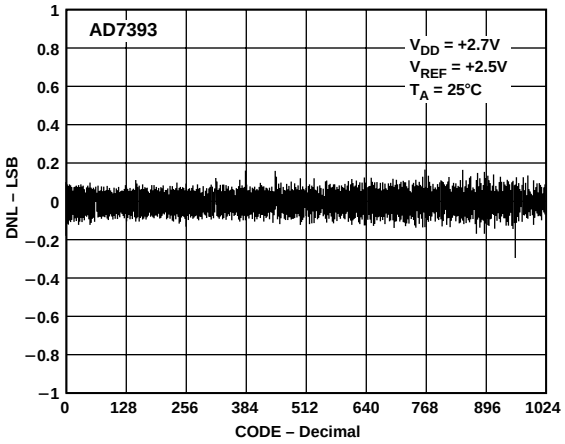


Figure 2. AD7393 Differential Nonlinearity Error vs. Code

REV. A

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AD7392/AD7393–SPECIFICATIONS

AD7392 ELECTRICAL CHARACTERISTICS (@ $V_{REF\ IN}$ = 2.5 V, −40°C < T_A < +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	3 V ± 10%	5 V ± 10%	Units
STATIC PERFORMANCE					
Resolution[1]	N		12	12	Bits
Relative Accuracy[2]	INL	T_A = +25°C	±1.8	±1.8	LSB max
		T_A = −40°C, +85°C	±3	±3	LSB max
Differential Nonlinearity[2]	DNL	T_A = +25°C, Monotonic	±0.9	±0.9	LSB max
		Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H, T_A = +25°C, +85°C	4.0	4.0	mV max
		Data = 000_H, T_A = –40°C	8.0	8.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = +25°C, +85°C, Data = FFF_H	±8	±8	mV max
		T_A = −40°C, Data = FFF_H	±20	±20	mV max
Full-Scale Tempco[3]	TCV_{FS}		28	28	ppm/°C typ
REFERENCE INPUT					
$V_{REF\ IN}$ Range	V_{REF}		0/V_{DD}	0/V_{DD}	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Current (Source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD}−0.6	V_{DD}−0.6	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Chip Select Write Width	t_{CS}		45	45	ns min
Data Setup	t_{DS}		30	15	ns min
Data Hold	t_{DH}		20	5	ns min
Reset Pulsewidth	t_{RS}		40	30	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H	0.05	0.05	V/µs typ
Settling Time[6]	t_S	To ±0.1% of Full Scale	70	60	µs typ
Shutdown Recovery Time	t_{SDR}			80	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nV/s typ
Digital Feedthrough	Q		15	15	nV/s typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V dc +1 V p-p,			
		Data = 000_H, f = 100 kHz	–63	–63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	$\overline{V_{IL}}$ = 0 V, No Load	55/100	55/100	µA typ/max
Shutdown Supply Current	I_{DD_SD}	$\overline{SHDN}$ = 0, V_{IL} = 0 V, No Load	0.1/1.5	0.1/1.5	µA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	300	500	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

NOTES

[1]One LSB = V_{REF}/4096 V for the 12-bit AD7392.

[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.

[3]These parameters are guaranteed by design and not subject to production testing.

[4]Typicals represent average readings measured at +25°C.

[5]All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of 13 V) and timed from a voltage level of 1.6 V.

[6]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

AD7393 ELECTRICAL CHARACTERISTICS (@ $V_{REF\ IN}$ = 2.5 V, −40°C < T_A < +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	3 V ± 10%	5 V ± 10%	Units
STATIC PERFORMANCE					
Resolution[1]	N		10	10	Bits
Relative Accuracy[2]	INL	T_A = +25°C	±1.75	±1.75	LSB max
		T_A = −40°C, +85°C, +125°C	±2.0	±2.0	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±0.8	±0.8	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	9.0	9.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = +25°C, +85°C, +125°C, Data = $3FF_H$	±32	±32	mV max
		T_A = −40°C, Data = $3FF_H$	±42	±42	mV max
Full-Scale Tempco[3]	TCV_{FS}		28	28	ppm/°C typ
REFERENCE INPUT					
$V_{REF\ IN}$ Range	V_{REF}		0/V_{DD}	0/V_{DD}	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (Source)	I_{OUT}	Data = 200_H, ΔV_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 200_H, ΔV_{OUT} = 5 LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD}−0.6	V_{DD}−0.6	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Chip Select Write Width	t_{CS}		45	45	ns
Data Setup	t_{DS}		30	15	ns
Data Hold	t_{DH}		20	5	ns
Reset Pulsewidth	t_{RS}		40	30	ns
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to $3FF_H$ to 000_H	0.05	0.05	V/µs typ
Settling Time[6]	t_S	To ±0.1% of Full Scale	70	60	µs typ
Shutdown Recovery Time	t_{SDR}			80	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nV/s typ
Digital Feedthrough	Q		15	15	nV/s typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V dc +1 V p-p, Data = 000_H, f = 100 kHz	–63	–63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load, T_A = +25°C	55	55	µA typ
		V_{IL} = 0 V, No Load	100	100	µA max
Shutdown Supply Current	I_{DD_SD}	$\overline{SHDN}$ = 0, V_{IL} = 0 V, No Load	0.1/1.5	0.1/1.5	µA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	300	500	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

NOTES
[1]One LSB = V_{REF}/1024 V for the 10-bit AD7393.
[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.
[3]These parameters are guaranteed by design and not subject to production testing.
[4]Typicals represent average readings measured at +25°C.
[5]All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of +3 V) and timed from a voltage level of 1.6 V.
[6]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND ..... –0.3 V, +8 V
V_{REF} to GND ..... –0.3 V, V_{DD}
Logic Inputs to GND ..... –0.3 V, +8 V
V_{OUT} to GND ..... –0.3 V, V_{DD} + 0.3 V
I_{OUT} Short Circuit to GND ..... 50 mA
DGND to AGND ..... –0.3 V, +2 V
Package Power Dissipation ..... $(T_J \text{ max} - T_A)/\theta_{JA}$
Thermal Resistance θ_{JA}
20-Lead Plastic DIP Package (N-20) ..... 57°C/W
20-Lead SOIC Package (R-20) ..... 60°C/W
20-Lead Thin-Shrink Surface Mount (RU-20) ... 155°C/W
Maximum Junction Temperature (T_J max) ..... 150°C
Operating Temperature Range ..... –40°C to +85°C
AD7393AR ..... –40°C to +125°C
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature
N-20 (Soldering, 10 sec) ..... +300°C
R-20 (Vapor Phase, 60 sec) ..... +215°C
RU-20 (Infrared, 15 sec) ..... +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

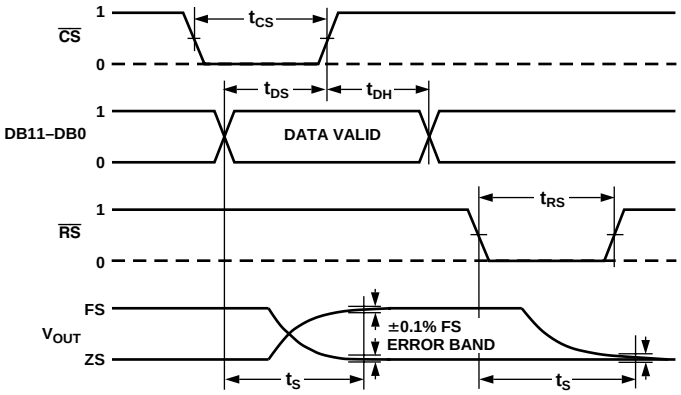


Figure 3. Timing Diagram

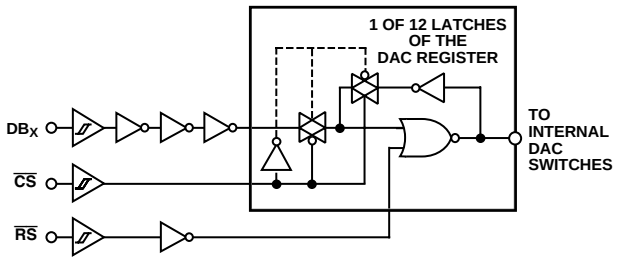
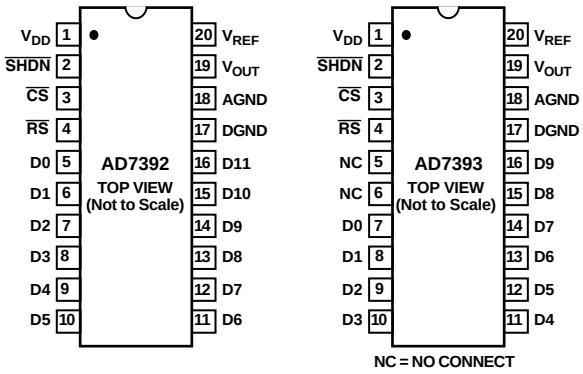


Figure 4. Digital Control Logic

PIN CONFIGURATIONS



PIN DESCRIPTION

#	Name	Function
1	V_{DD}	Positive Power Supply Input. Specified range of operation +2.7 V to +5.5 V.
2	$\overline{SHDN}$	Power Shutdown active low input. DAC register contents are saved as long as power stays on the V_{DD} pin. When $\overline{SHDN}$ = 0, $\overline{CS}$ strobes will write new data into the DAC register.
3	$\overline{CS}$	Chip Select latch enable, active low.
4	$\overline{RS}$	Resets DAC register to zero condition. Asynchronous active low input.
5, 6	NC	No connect Pins 5 and 6 on the AD7393.
17	DGND	Digital Ground.
18	AGND	Analog Ground.
19	V_{OUT}	DAC Voltage Output.
20	V_{REFIN}	DAC Reference Input Pin. Establishes DAC full-scale voltage.
	D0–D11	12 parallel input data bits. D11 = MSB Pin 16, D0 = LSB Pin 5, AD7392.
	D0–D9	10 parallel input data bits. D9 = MSB. Pin 16, D0 = LSB Pin 7, AD7393.

ORDERING GUIDE

Model	Res (LSB)	Temp	Package Description	Package Option
AD7392AN	12	XIND	20-Lead P-DIP	N-20
AD7392AR	12	XIND	20-Lead SOIC	R-20
AD7393AN	10	XIND	20-Lead P-DIP	N-20
AD7393AR	10	AUTO	20-Lead SOIC	R-20
AD7393ARU	10	XIND	TSSOP-20	RU-20

NOTES
XIND = –40°C to +85°C; AUTO = –40°C to +125°C.
The AD7392 contains 709 transistors. The die size measures 78 mil × 85 mil = 6630 sq. mil.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7392/AD7393 feature proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

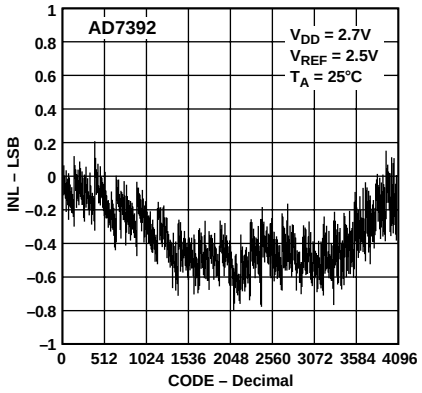


Figure 5. AD7392 Integral Nonlinearity Error vs. Code

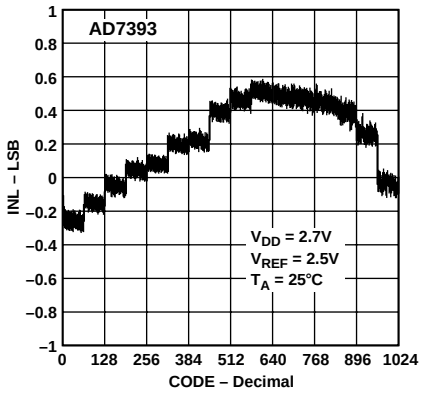


Figure 6. AD7393 Integral Nonlinearity Error vs. Code

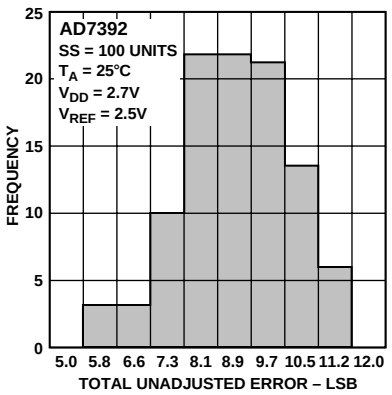


Figure 7. AD7392 Total Unadjusted Error Histogram

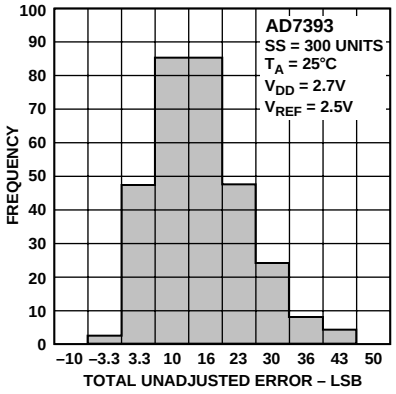


Figure 8. AD7393 Total Unadjusted Error Histogram

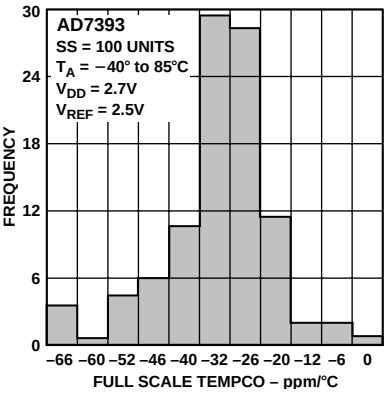


Figure 9. AD7393 Full-Scale Output Tempco Histogram

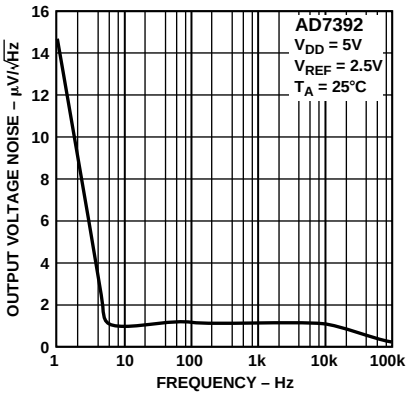


Figure 10. Voltage Noise Density vs. Frequency

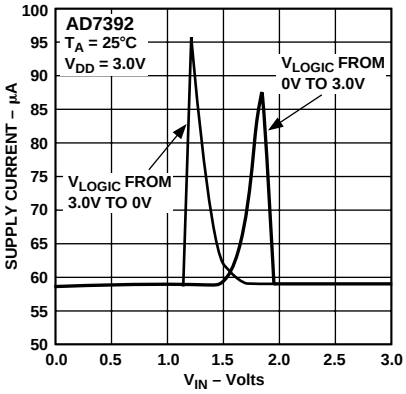


Figure 11. Supply Current vs. Logic Input Voltage

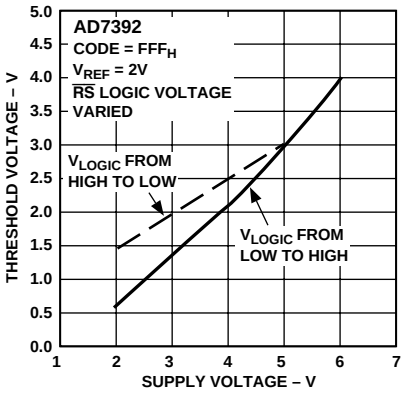


Figure 12. Logic Threshold vs. Supply Voltage

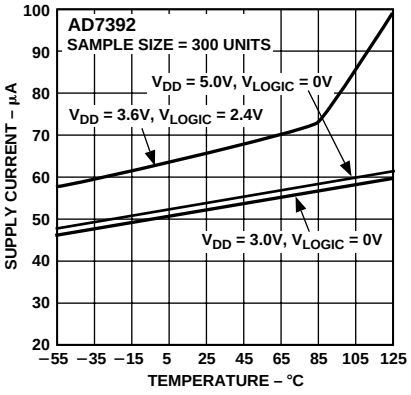


Figure 13. Supply Current vs. Temperature

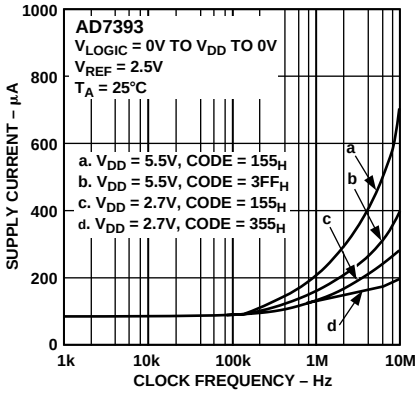


Figure 14. Supply Current vs. Clock Frequency

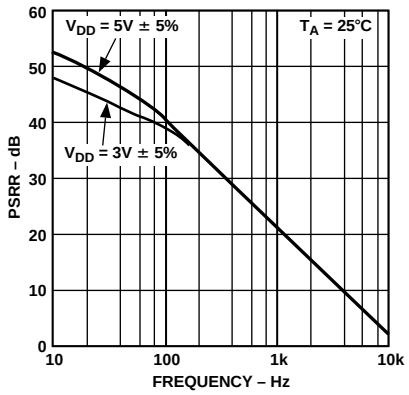


Figure 15. Power Supply Rejection vs. Frequency

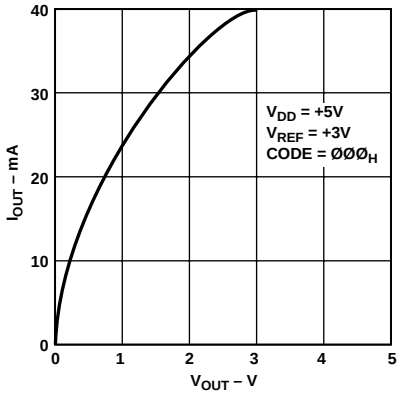


Figure 16. I_{OUT} at Zero Scale vs. V_{OUT}

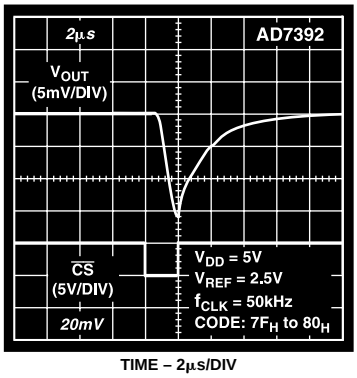


Figure 17. Midscale Transition Performance

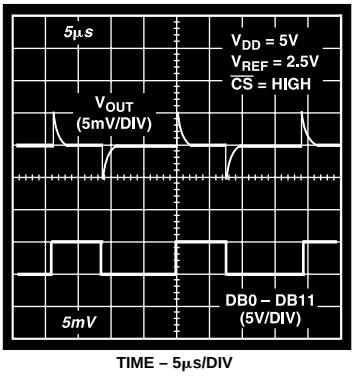


Figure 18. Digital Feedthrough

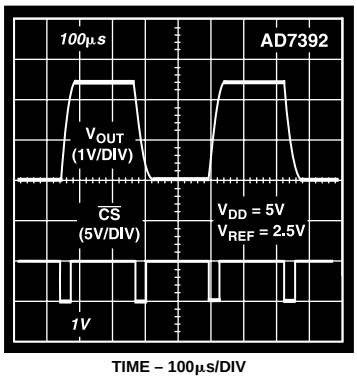


Figure 19. Large Signal Settling Time

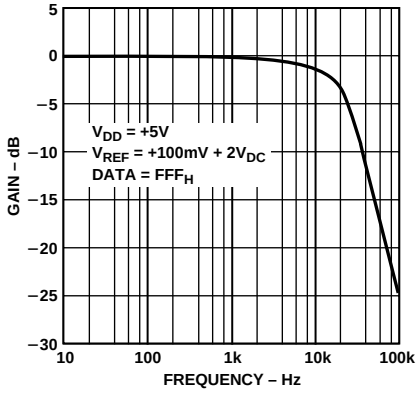


Figure 20. Reference Multiplying Bandwidth

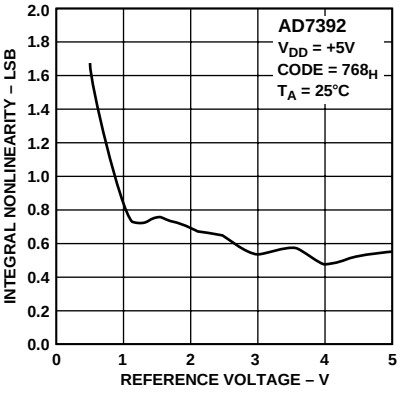


Figure 21. INL Error vs. Reference Voltage

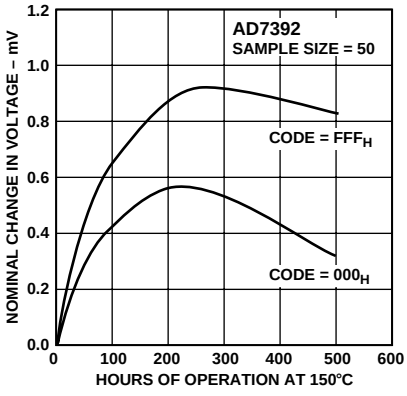


Figure 22. Long-Term Drift Accelerated by Burn-in

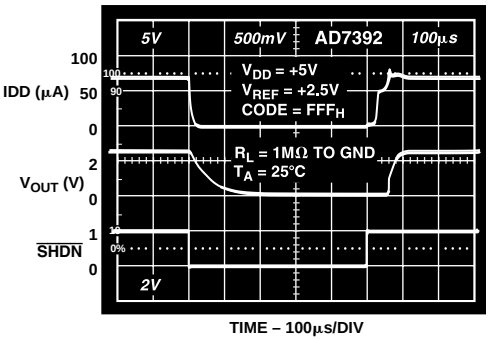


Figure 23. Shutdown Recovery Time

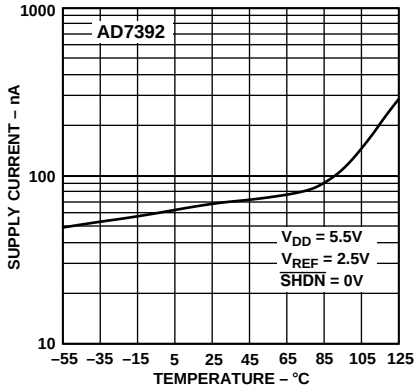


Figure 24. Shutdown Current vs. Temperature

Table I. Control Logic Truth Table

$\overline{CS}$	$\overline{RS}$	DAC Register Function
H	H	Latched
L	H	Transparent
↑	H	Latched with New Data
X	L	Loaded with All Zeros
H	↑	Latched all Zeros

NOTE
↑ Positive logic transition; X Don't Care.

OPERATION

The AD7392 and AD7393 comprise a set of pin compatible, 12-bit/10-bit digital-to-analog converters. These single-supply operation devices consume less than 100 microamps of current while operating from power supplies in the +2.7 V to +5.5 V range making them ideal for battery operated applications. They contain a voltage-switched, 12-bit/10-bit, laser-trimmed digital-to-analog converter, rail-to-rail output op amps, and a parallel-input DAC register. The external reference input has constant input resistance independent of the digital code setting of the DAC. In addition, the reference input can be tied to the same supply voltage as V_{DD}, resulting in a maximum output voltage span of 0 to V_{DD}. The parallel data interface consists of 12 data bits, DB0–DB11, for the AD7392; 10 data bits, DB0–DB9, for the AD7393; and a $\overline{CS}$ write strobe. A $\overline{RS}$ pin is available to reset the DAC register to zero scale. This function is useful for power-on reset or system failure recovery to a known state. Additional power savings are accomplished by activating the $\overline{SHDN}$ pin, resulting in a 1.5 µA maximum consumption sleep mode. As long as the supply voltage remains, data will be retained in the DAC register to reset the DAC output when the part is taken out of shutdown ($\overline{SHDN}$ = 1).

D/A CONVERTER SECTION

The voltage switched R-2R DAC generates an output voltage dependent on the external reference voltage connected to the REF pin according to the following equation:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \qquad \text{Equation 1}$$

where D is the decimal data word loaded into the DAC register, and N is the number of bits of DAC resolution. In the case of the 10-bit AD7393 using a 2.5 V reference, Equation 1 simplifies to:

$$V_{OUT} = 2.5 \times \frac{D}{1024} \qquad \text{Equation 2}$$

Using Equation 2, the nominal midscale voltage at V_{OUT} is 1.25 V for D = 512; full-scale voltage is 2.497 volts. The LSB step size is = 2.5 × 1/1024 = 0.0024 volts.

For the 12-bit AD7392 operating from a 5.0 V reference Equation 1 becomes:

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \qquad \text{Equation 3}$$

Using Equation 3, the AD7392 provides a nominal midscale voltage of 2.50 V for D = 2048, and a full-scale output of 4.998 volts. The LSB step size is = 5.0 × 1/4096 = 0.0012 volts.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. The op amp has a 60 μs typical settling time to 0.1% of full scale. There are slight differences in settling time for negative slewing signals versus positive. Also, negative transition settling-time to within the last 6 LSBs of zero volts has an extended settling time. The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 25 shows an equivalent output schematic of the rail-to-rail-amplifier with its N-channel pull-down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P-channel pull-up device that can source current to GND terminated loads.

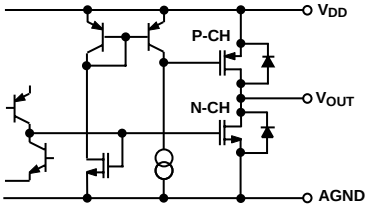


Figure 25. Equivalent Analog Output Circuit

The rail-to-rail output stage provides ±1 mA of output current. The N-channel output pull-down MOSFET, shown in Figure 25, has a 35 Ω ON resistance that sets the sink current capability near ground. In addition to resistive load driving capability, the amplifier also has been carefully designed and characterized for up to 100 pF capacitive load driving capability.

REFERENCE INPUT

The reference input terminal has a constant input resistance independent of digital code, which results in reduced glitches on the external reference voltage source. The high 2.5 MΩ input-resistance minimizes power dissipation within the AD7392/AD7393 D/A converters. The V_{REF} input accepts input voltages ranging from ground to the positive-supply voltage V_{DD}. One of the simplest applications that saves an external reference voltage source is connection of the REF terminal to the positive V_{DD} supply. This connection results in a rail-to-rail voltage output span maximizing the programmed range. The reference input will accept ac signals as long as they are kept within the supply voltage range, $0 < V_{REF\,IN} < V_{DD}$. The reference bandwidth and integral nonlinearity error performance are plotted in the typical performance section (see Figures 20 and 21). The ratiometric reference feature makes the AD7392/AD7393 an ideal companion to ratiometric analog-to-digital converters such as the AD7896.

POWER SUPPLY

The very low power consumption of the AD7392/AD7393 is a direct result of a circuit design optimizing the use of a CBCMOS process. By using the low power characteristics of CMOS for the logic and the low noise, tight-matching of the complementary bipolar transistors, excellent analog accuracy is achieved. One advantage of the rail-to-rail output amplifiers used in the AD7392/AD7393 is the wide range of usable supply voltage. The part is fully specified and tested for operation from +2.7 V to +5.5 V.

POWER SUPPLY BYPASSING AND GROUNDING

Precision analog products, such as the AD7392/AD7393, require a well filtered power source. Since the AD7392/AD7393 operate from a single +3 V to +5 V supply, it seems convenient to simply tap into the digital logic power supply. Unfortunately, the logic supply is often a switch-mode design, which generates noise in the 20 kHz to 1 MHz range. In addition, fast logic gates can generate glitches of hundreds of millivolts in amplitude due to wiring resistance and inductance. The power supply noise generated as a result means that special care must be taken to assure that the inherent precision of the DAC is maintained. Good engineering judgment should be exercised when addressing the power supply grounding and bypassing of the AD7392.

The AD7392 should be powered directly from the system power supply. This arrangement, shown in Figure 26, employs an LC filter and separate power and ground connections to isolate the analog section from the logic switching transients.

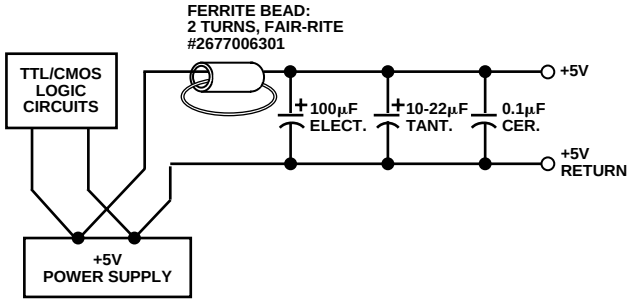


Figure 26. Use Separate Traces to Reduce Power Supply Noise

Whether or not a separate power supply trace is available, generous supply bypassing will reduce supply line induced errors. Local supply bypassing, consisting of a 10 μF tantalum electrolytic in parallel with a 0.1 μF ceramic capacitor, is recommended in all applications (Figure 27).

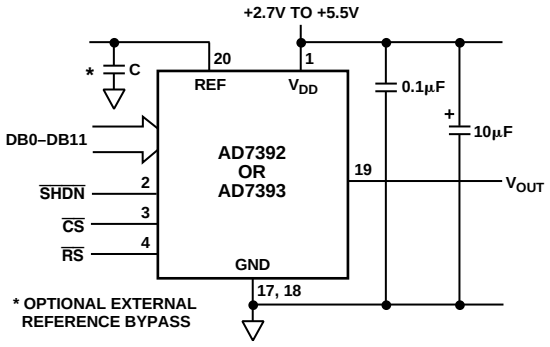


Figure 27. Recommended Supply Bypassing for the AD7392/AD7393

INPUT LOGIC LEVELS

All digital inputs are protected with a Zener-type ESD protection structure (Figure 28) that allows logic input voltages to exceed the V_{DD} supply voltage. This feature can be useful if the user is driving one or more of the digital inputs with a 5 V CMOS logic input-voltage level while operating the AD7392/AD7393 on a +3 V power supply. If this mode of interface is used, make sure that the V_{OL} of the 5 V CMOS meets the V_{IL} input requirement of the AD7392/AD7393 operating at 3 V. See Figure 12 for a graph for digital logic input threshold versus operating V_{DD} supply voltage.

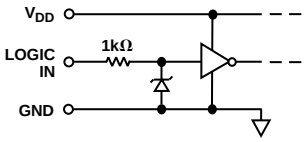


Figure 28. Equivalent Digital Input ESD Protection

In order to minimize power dissipation from input-logic levels that are near the V_{IH} and V_{IL} logic input voltage specifications, a Schmitt trigger design was used that minimizes the input-buffer current consumption compared to traditional CMOS input stages. Figure 11 shows a plot of incremental input voltage versus supply current, showing that negligible current consumption takes place when logic levels are in their quiescent state. The normal cross over current still occurs during logic transitions. A secondary advantage of this Schmitt trigger is the prevention of false triggers that would occur with slow moving logic transitions when a standard CMOS logic interface or opto-isolators are used. The logic inputs DB11–DB0, $\overline{CS}$, $\overline{RS}$, $\overline{SHDN}$ all contain the Schmitt trigger circuits.

DIGITAL INTERFACE

The AD7392/AD7393 have a parallel data input. A functional block diagram of the digital section is shown in Figure 4, while Table I contains the truth table for the logic control inputs. The chip select ($\overline{CS}$) pin controls loading of data from the data inputs on pins DB11–DB0. This active low input places the input register into a transparent state allowing the data inputs to directly change the DAC ladder values. When $\overline{CS}$ returns to logic high within the data setup and hold time specifications, the new value of data in the input-register will be latched. See Truth Table for complete set of conditions.

RESET (RS) PIN

Forcing the asynchronous $\overline{RS}$ pin low will set the DAC register to all zeros and the DAC output voltage will be zero volts. The reset function is useful for setting the DAC outputs to zero at power-up or after a power supply interruption. Test systems and motor controllers are two of many applications that benefit from powering up to a known state. The external reset pulse can be generated by the microprocessor's power-on RESET signal, by an output from the microprocessor or by an external resistor and capacitor. RESET has a Schmitt trigger input which results in a clean reset function when using external resistor/capacitor generated pulses. See the Control-Logic Truth Table I.

POWER SHUTDOWN (SHDN)

Maximum power savings can be achieved by using the power shutdown control function. This hardware activated feature is controlled by the active low input $\overline{SHDN}$ pin. This pin has a Schmitt trigger input that helps desensitize it to slowly changing inputs. By placing a logic low on this pin, the internal consumption of the AD7392 or AD7393 is reduced to nanoamp levels, guaranteed to 1.5 μA maximum over the operating temperature range. If power is present at all times on the V_{DD} pin while in the shutdown mode, the internal DAC register will retain the last programmed data value. The digital interface is still active in shutdown, so that code changes can be made that will produce new DAC settings when the device is taken out of shutdown. This data will be used when the part is returned to the normal active state by placing the DAC back to its programmed voltage setting. Figure 23 shows a plot of shutdown recovery time with both I_{DD} and V_{OUT} displayed. In the shutdown state the DAC output amplifier exhibits an open-circuit high resistance state. Any load connected will stabilize at its termination voltage. If the power shutdown feature is not needed, the user should tie the $\overline{SHDN}$ pin to the V_{DD} voltage thereby disabling this function.

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7392. As shown in Figure 29, the AD7392 has been designed to drive loads as low as 5 kΩ in parallel with 100 pF. The code table for this operation is shown in Table II.

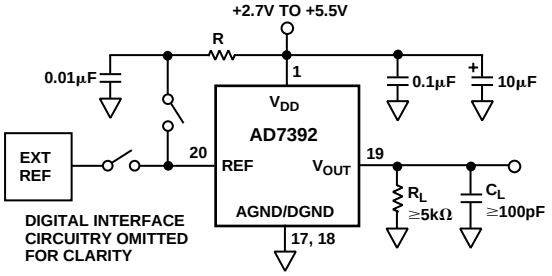


Figure 29. AD7392 Unipolar Output Operation

Table II. Unipolar Code Table

Hexadecimal Number in DAC Register	Decimal Number in DAC Register	Output Voltage (V) V_{REF} = 2.5 V
FFF	4095	2.4994
801	2049	1.2506
800	2048	1.2500
7FF	2047	1.2494
000	0	0

The circuit can be configured with an external reference plus power supply or powered from a single dedicated regulator or reference depending on the application performance requirements.

BIPOLAR OUTPUT OPERATION

Although the AD7393 has been designed for single-supply operation, the output can be easily configured for bipolar operation. A typical circuit is shown in Figure 30. This circuit uses a clean regulated +5 V supply for power, which also provides the circuit's reference voltage. Since the AD7393 output span swings from ground to very near +5 V, it is necessary to choose an external amplifier with a common-mode input voltage range that extends to its positive supply rail. The micropower consumption OP196 has been designed just for this purpose and results in only 50 microamps of maximum current consumption. Connection of the equal valued 470 kΩ resistors results in a differential amplifier mode of operation with a voltage gain of two, which produces a circuit output span of ten volts (that is, –5 V to +5 V). As the DAC is programmed from zero-code 000_H to midscale 200_H to full scale $3FF_H$, the circuit output voltage V_O is set at –5 V, 0 V and +5 V (minus 1 LSB). The output voltage V_O is coded in offset binary according to Equation 4.

$$V_O = \left[\frac{D}{512} - 1\right] \times 5 \qquad \text{Equation 4}$$

where *D* is the decimal code loaded in the AD7393 DAC register. Note that the LSB step size is 10/1024 = 10 mV. This circuit has been optimized for micropower consumption including the 470 kΩ gain setting resistors, which should have low temperature coefficients to maintain accuracy and matching (preferably the same resistor material, such as metal film). If better stability is required, the power supply could be substituted with a precision reference voltage such as the low drop out REF195, which can easily supply the circuit's 162 µA of current, and still provide additional power for the load connected to V_O. The micropower REF195 is guaranteed to source 10 mA output drive current, but only consumes 50 µA internally. If higher resolution is required, the AD7392 can be used with the addition of two more bits of data inserted into the software coding, which would result in a 2.5 mV LSB step size. Table III shows examples of nominal output voltages V_O provided by the Bipolar Operation circuit application.

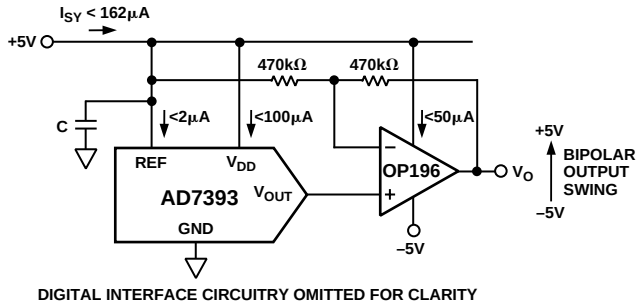


Figure 30. Bipolar Output Operation

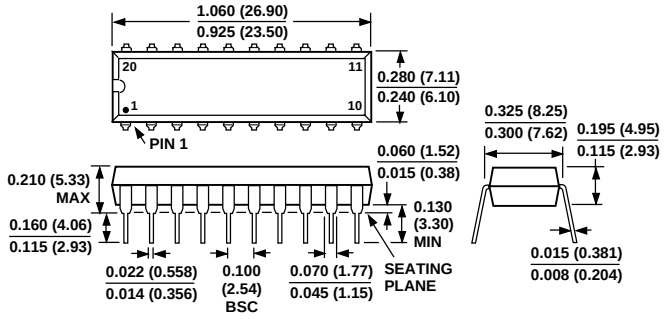
Table III. Bipolar Code Table

Hexadecimal Number In DAC Register	Decimal Number in DAC Register	Analog Output Voltage (V)
3FF	1023	4.9902
201	513	0.0097
200	512	0.0000
1FF	511	–0.0097
000	0	–5.0000

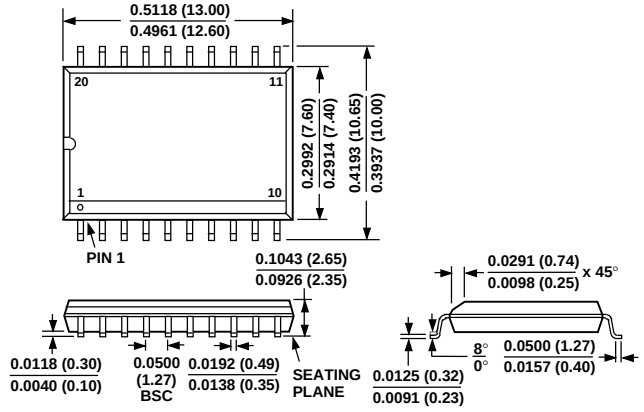
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

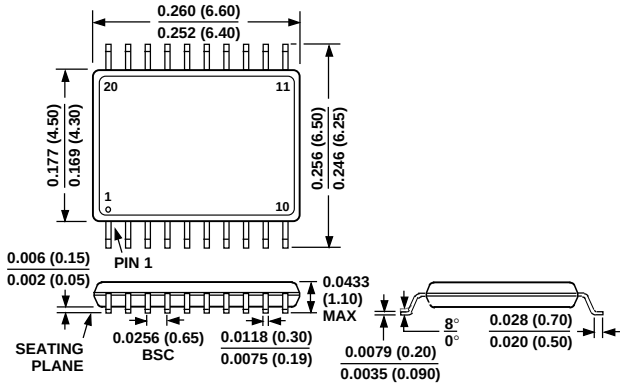
20-Lead Plastic DIP Package
(N-20)



20-Lead SOIC Package
(R-20)



20-Lead Thin Surface Mount TSSOP Package
(RU-20)



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