

1.1 Scope.

This specification covers the detail requirements for a monolithic CMOS 10-bit multiplying digital-to-analog converter with an input buffer and a holding register, allowing direct interface with microprocessors.

1.2 Part Number.

The complete part number per Table 1 of this specification is as follows:

Device	Part Number
-1	AD7522SQ/883B
-2	AD7522TQ/883B
-3	AD7522UQ/883B

1.2.3 Case Outline.

See Appendix I of General Specification ADI-M-1000: package outline: Q-28

1.3 Absolute Maximum Ratings. ($T_A = 25^\circ\text{C}$ unless otherwise noted)

V_{REF} to GND	$\pm 25\text{V}$
V_{DD} to DGND	0V, +17V
V_{CC} to GND	$\pm 17\text{V}$
V_{CC} to V_{DD}	$\pm 0.4\text{V}$
Output Voltage (Pins 6 and 7)	-0.3V, V_{DD}
Digital Input Voltage Range	V_{DD} to GND
Power Dissipation	
Up to +50°C	1000mW
Derates above +75°C	10mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

1.5 Thermal Characteristics.

Thermal Resistance $\theta_{JC} = 35^\circ\text{C/W}$
 $\theta_{JA} = 120^\circ\text{C/W}$

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Test	Symbol	Device	Design Limit $T_{min}-T_{max}$	Sub Group 1	Sub Group 2, 3	Sub Group 4	Test Condition ¹	Units
Resolution	RES	-1, 2, 3	10	-			SC8 = "1"	Bits
Nonlinearity	NL	-1 -2 -3	2 1 1/2	2 2 2	2 1 1/2	1 1/2		± LSB max
Nonlinearity Tempco	TC _{NL}	-1, 2, 3	2					± ppm/°C max
Gain Tempco	TC _{GA}	-1, 2, 3	30					± ppm/°C max
Output Leakage Current Pin 6 Pin 7	I _{OUT1} I _{OUT2}	-1, 2, 3 -1, 2, 3	200 200	200 200	200 200		DB0 thru DB9 = 0 DB0 thru DB9 = 1	± nA max ± nA max
Feedthrough Error	FT	-1, 2, 3	10				V _{REF} = 20V p-p, 10kHz @ +25°C	mV p-p max
Reference Input Resistance	R _{IN}	-1, 2, 3	5 20	5 20	5 20			kΩ min kΩ max
Digital Input High Voltage	V _{IH}	-1, 2, 3	2.4 13.5	2.4 13.5	2.4 13.5		V _{CC} = +5V V _{CC} = +15V	V min V min
Digital Input Low Voltage	V _{IL}	-1, 2, 3	0.8 1.5	0.8 1.5	0.8 1.5		V _{CC} = +5V V _{CC} = +15V	V max V max
LDAC Pulse Width	t _{LD}	-1, 2, 3	500				LDAC: 0 to +3V	ns min
HBS, LBS Pulse Width	t _{BS}	-1, 2, 3	500				HBS, LBS: 0 to +3V	ns min
Serial Clock Frequency	t _{CLK}	-1, 2, 3	1					MHz max
HBS, LBS Data Setup ²	t _{DS}	-1, 2, 3	250					ns min
Data Hold Time ³	t _{DH}	-1, 2, 3	500					ns min
Supply Current from V _{DD}	I _{DD}	-1, 2, 3	2	2	2		In Quiescent State at +25°C All Logic Input V _{IL} or V _{IH} .	mA max
Supply Current from V _{CC}	I _{CC}	-1, 2, 3	2	2	2		In Quiescent State at +25°C All Logic Input V _{IL} or V _{IH} .	mA max

NOTES

¹V_{DD} = +15V; V_{CC} = +5V, V_{REF} = +10V unless otherwise stated.

²Data setup time is the minimum amount of time required for DB0-DB9 to be stable prior to strobing HBS, LBS.

³Data hold time is the minimum amount of time required for DB0-DB9 to be stable after strobing HBS, LBS.

Table 1.

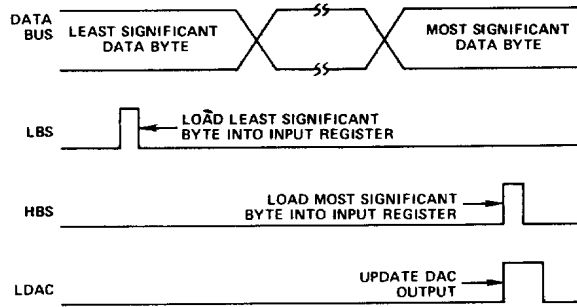


Figure 1. Timing Diagram

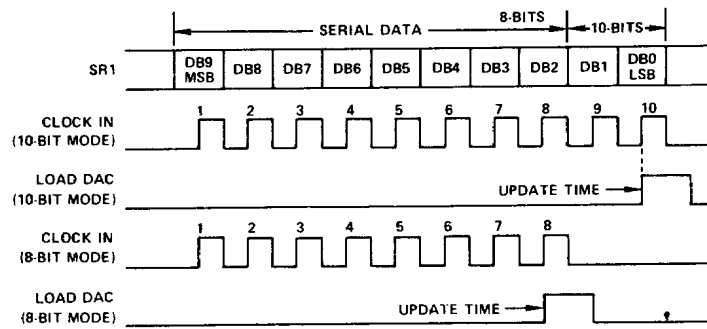


Figure 2. Timing Diagram for Serial 8- and 10-Bit Loading