Low-Cost, High-Speed Differential Amplifier

AD8132

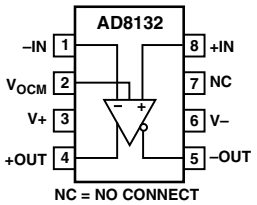
FEATURES

High Speed
350 MHz –3 dB Bandwidth
1200 V/μs Slew Rate
Resistor-Settable Gain
Internal Common-Mode Feedback to Improve Gain and Phase Balance –68 dB @ 10 MHz
Separate Input to Set the Common-Mode Output Voltage
Low Distortion –99 dBc SFDR @ 5 MHz 800 Ω Load
Low Power 10.7 mA @ 5 V
Power Supply Range +2.7 V to ±5.5 V

APPLICATIONS

Low Power Differential ADC Driver
Differential Gain and Differential Filtering
Video Line Driver
Differential In/Out Level-Shifting
Single-Ended Input to Differential Output Driver
Active Transformer

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD8132 is a low-cost differential or single-ended input to differential output amplifier with resistor-settable gain. The AD8132 is a major advancement over op amps for driving differential input ADCs or for driving signals over long lines. The AD8132 has a unique internal feedback feature that provides output gain and phase matching balanced to –68 dB at 10 MHz, suppressing harmonics, and reducing radiated EMI.

Manufactured on ADI's next generation of XFCB bipolar process, the AD8132 has a –3 dB bandwidth of 350 MHz and delivers a differential signal with –99 dBc SFDR at 5 MHz, despite its low cost. The AD8132 eliminates the need for a transformer with high-performance ADCs, preserving the low frequency and dc information. The common-mode level of the differential output is adjustable by applying a voltage on the V_{OCM} pin, easily level-shifting the input signals for driving single supply ADCs. Fast overload recovery preserves sampling accuracy.

The AD8132 can also be used as a differential driver for the transmission of high-speed signals over low-cost twisted pair or coaxial cables. The feedback network can be adjusted to boost the high-frequency components of the signal. The AD8132 can be used for either analog or digital video signals or for other high-speed data transmission. The AD8132 is capable of driving either cat3 or cat5 twisted pair or coaxial with minimal line attenuation. The AD8132 has considerable cost and performance improvements over discrete line driver solutions.

Differential signal processing reduces the effects of ground noise which plagues ground referenced systems. The AD8132 can be used for differential signal processing (gain and filtering) throughout a signal chain, easily simplifying the conversion between differential and single-ended components.

The AD8132 is available in both SOIC and μSOIC packages for operation over –40°C to +85°C temperatures.

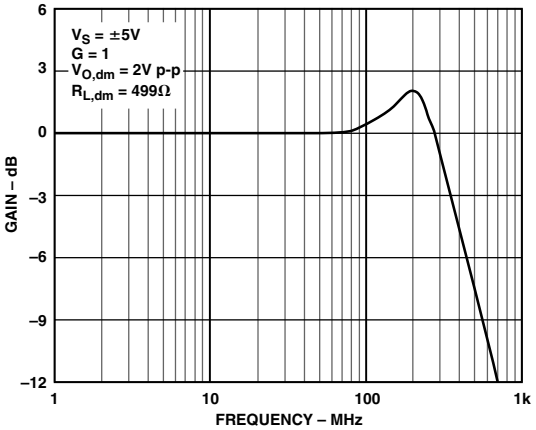


Figure 1. Large Signal Frequency Response

REV. B

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AD8132–SPECIFICATIONS

(@ 25°C, V_S = ±5 V, V_{OCM} = 0 V, G = 1, $R_{L,dm}$ = 499 Ω, R_F = R_G = 348 Ω unless otherwise noted. For G = 2, $R_{L,dm}$ = 200 Ω, R_F = 1000 Ω, R_G = 499 Ω. Refer to TPC 1 and TPC 10 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
±D_{IN} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p	300	350		MHz
	V_{OUT} = 2 V p-p, G = 2		190		MHz
–3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		360		MHz
	V_{OUT} = 0.2 V p-p, G = 2		160		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.2 V p-p		90		MHz
	V_{OUT} = 0.2 V p-p, G = 2		50		MHz
Slew Rate	V_{OUT} = 2 V p-p	1000	1200		V/µs
Settling Time	0.1%, V_{OUT} = 2 V p-p		15		ns
Overdrive Recovery Time	V_{IN} = 5 V to 0 V Step, G = 2		5		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 1 MHz, $R_{L,dm}$ = 800 Ω		–96		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–83		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–73		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 1 MHz, $R_{L,dm}$ = 800 Ω		–102		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–98		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–67		dBc
IMD	20 MHz, $R_{L,dm}$ = 800 Ω		–76		dBc
IP3	20 MHz, $R_{L,dm}$ = 800 Ω		40		dBm
Input Voltage Noise (RTI)	f = 0.1 MHz to 100 MHz		8		nV/$\sqrt{\text{Hz}}$
Input Current Noise	f = 0.1 MHz to 100 MHz		1.8		pA/$\sqrt{\text{Hz}}$
Differential Gain Error	NTSC, G = 2, $R_{L,dm}$ = 150 Ω		0.01		%
Differential Phase Error	NTSC, G = 2, $R_{L,dm}$ = 150 Ω		0.10		Degrees
INPUT CHARACTERISTICS					
Offset Voltage (RTI)	$V_{OS,dm}$ = $V_{OUT,dm}$/2; V_{DIN+} = V_{DIN-} = V_{OCM} = 0 V		±1.0	±3.5	mV
	T_{MIN} to T_{MAX} Variation		10		µV/°C
Input Bias Current			3	7	µA
Input Resistance	Differential		12		MΩ
	Common-Mode		3.5		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			–7 to +6		V
CMRR	$\Delta V_{OUT,dm}/\Delta V_{IN,cm}$; $\Delta V_{IN,cm}$ = ±1 V; Resistors Matched to 0.01%		–70	–60	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; Single-Ended Output		–3.6 to +3.6		V
Output Current			70		mA
Output Balance Error	$\Delta V_{OUT,cm}/\Delta V_{OUT,dm}$; $\Delta V_{OUT,dm}$ = 1 V		–70		dB
V_{OCM} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	ΔV_{OCM} = 600 mV p-p		210		MHz
Slew Rate	ΔV_{OCM} = –1 V to +1 V		400		V/µs
DC PERFORMANCE					
Input Voltage Range			±3.6		V
Input Resistance			150		kΩ
Input Offset Voltage	$V_{OS,cm}$ = $V_{OUT,cm}$; V_{DIN+} = V_{DIN-} = V_{OCM} = 0 V		±1.5	±7	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$[\Delta V_{OUT,dm}/\Delta V_{OCM}]$; ΔV_{OCM} = ±1 V; Resistors Matched to 0.01%		–68		dB
Gain	$\Delta V_{OUT,cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V	0.985	1	1.015	V/V
POWER SUPPLY					
Operating Range		±1.35		±5.5	V
Quiescent Current	V_{DIN+} = V_{DIN-} = V_{OCM} = 0 V	11	12	13	mA
	T_{MIN} to T_{MAX} Variation		16		µA/°C
Power Supply Rejection Ratio	$\Delta V_{OUT,dm}/\Delta V_S$; ΔV_S = ±1 V		–70	–60	dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

SPECIFICATIONS (@ 25°C, V_S = 5 V, V_{OCM} = 2.5 V, G = 1, $R_{L,dm}$ = 499 Ω, R_F = R_G = 348 Ω unless otherwise noted. For G = 2, $R_{L,dm}$ = 200 Ω, R_F = 1000 Ω, R_G = 499 Ω. Refer to TPC 1 and TPC 10 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
±D_{IN} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Large Signal Bandwidth	V_{OUT} = 2 V p-p	250	300		MHz
	V_{OUT} = 2 V p-p, G = 2		180		MHz
–3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		360		MHz
	V_{OUT} = 0.2 V p-p, G = 2		155		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.2 V p-p		65		MHz
	V_{OUT} = 0.2 V p-p, G = 2		50		MHz
Slew Rate	V_{OUT} = 2 V p-p	800	1000		V/µs
Settling Time	0.1%, V_{OUT} = 2 V p-p		20		ns
Overdrive Recovery Time	V_{IN} = 2.5 V to 0 V Step, G = 2		5		ns
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 2 V p-p, 1 MHz, $R_{L,dm}$ = 800 Ω		–97		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–100		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–74		dBc
Third Harmonic	V_{OUT} = 2 V p-p, 1 MHz, $R_{L,dm}$ = 800 Ω		–100		dBc
	V_{OUT} = 2 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–99		dBc
	V_{OUT} = 2 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–67		dBc
IMD	20 MHz, $R_{L,dm}$ = 800 Ω		–76		dBc
IP3	20 MHz, $R_{L,dm}$ = 800 Ω		40		dBm
Input Voltage Noise (RTI)	f = 0.1 MHz to 100 MHz		8		nV/√Hz
Input Current Noise	f = 0.1 MHz to 100 MHz		1.8		pA/√Hz
Differential Gain Error	NTSC, G = 2, $R_{L,dm}$ = 150 Ω		0.025		%
Differential Phase Error	NTSC, G = 2, $R_{L,dm}$ = 150 Ω		0.15		Degree
INPUT CHARACTERISTICS					
Offset Voltage (RTI)	$V_{OS,dm}$ = $V_{OUT,dm}$/2; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V		±1.0	±3.5	mV
	T_{MIN} to T_{MAX} Variation		6		µV/°C
Input Bias Current			3	7	µA
Input Resistance	Differential		10		MΩ
	Common-Mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			–1 to +4		V
CMRR	$\Delta V_{OUT,dm}/\Delta V_{IN,cm}$; $\Delta V_{IN,cm}$ = ±1 V; Resistors Matched to 0.01%		–70	–60	dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; Single-Ended Output		1 to 3.7		V
Output Current			50		mA
Output Balance Error	$\Delta V_{OUT,cm}/\Delta V_{OUT,dm}$; $\Delta V_{OUT,dm}$ = 1 V		–68		dB
V_{OCM} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	ΔV_{OCM} = 600 mV p-p		210		MHz
Slew Rate	ΔV_{OCM} = 1.5 V to 3.5 V		340		V/µs
DC PERFORMANCE					
Input Voltage Range			1 to 3.7		V
Input Resistance			130		kΩ
Input Offset Voltage	$V_{OS,cm}$ = $V_{OUT,cm}$; V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V		±5	±11	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	[$\Delta V_{OUT,dm}/\Delta V_{OCM}$]; ΔV_{OCM} = 2.5 ± 1 V; Resistors Matched to 0.01%		–66		dB
Gain	$\Delta V_{OUT,cm}/\Delta V_{OCM}$; ΔV_{OCM} = 2.5 ± 1 V	0.985	1	1.015	V/V
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current	V_{DIN+} = V_{DIN-} = V_{OCM} = 2.5 V	9.4	10.7	12	mA
	T_{MIN} to T_{MAX} Variation		10		µA/°C
Power Supply Rejection Ratio	$\Delta V_{OUT,dm}/\Delta V_S$; ΔV_S = ±1 V		–70	–60	dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

AD8132–SPECIFICATIONS (@ 25°C, V_S = 3 V, V_{OCM} = 1.5 V, G = 1, $R_{L,dm}$ = 499 Ω, R_F = R_G = 348 Ω unless otherwise noted. For G = 2, $R_{L,dm}$ = 200 Ω, R_F = 1000 Ω, R_G = 499 Ω. Refer to TPC 1 and TPC 10 for test setup and label descriptions. All specifications refer to single-ended input and differential outputs unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
±D_{IN} to ±OUT Specifications					
DYNAMIC PERFORMANCE					
–3 dB Large Signal Bandwidth	V_{OUT} = 1 V p-p		350		MHz
	V_{OUT} = 1 V p-p, G = 2		165		MHz
–3 dB Small Signal Bandwidth	V_{OUT} = 0.2 V p-p		350		MHz
	V_{OUT} = 0.2 V p-p, G = 2		150		MHz
Bandwidth for 0.1 dB Flatness	V_{OUT} = 0.2 V p-p		45		MHz
	V_{OUT} = 0.2 V p-p, G = 2		50		MHz
NOISE/HARMONIC PERFORMANCE					
Second Harmonic	V_{OUT} = 1 V p-p, 1 MHz, $R_{L,dm}$ = 800 Ω		–100		dBc
	V_{OUT} = 1 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–94		dBc
	V_{OUT} = 1 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–77		dBc
Third Harmonic	V_{OUT} = 1 V p-p, 1 MHz, $R_{L,dm}$ = 800 Ω		–90		dBc
	V_{OUT} = 1 V p-p, 5 MHz, $R_{L,dm}$ = 800 Ω		–85		dBc
	V_{OUT} = 1 V p-p, 20 MHz, $R_{L,dm}$ = 800 Ω		–66		dBc
INPUT CHARACTERISTICS					
Offset Voltage (RTI)	$V_{OS,dm}$ = $V_{OUT,dm}$/2; V_{DIN+} = V_{DIN-} = V_{OCM} = 1.5 V		±10		mV
Input Bias Current			3		µA
CMRR	$\Delta V_{OUT,dm}/\Delta V_{IN,cm}$; $\Delta V_{IN,cm}$ = ±0.5 V; Resistors Matched to 0.01%		–60		dB
V_{OCM} to ±OUT Specifications					
DC PERFORMANCE					
Input Offset Voltage	$V_{OS,cm}$ = $V_{OUT,cm}$; V_{DIN+} = V_{DIN-} = V_{OCM} = 1.5 V		±7		mV
Gain	$\Delta V_{OUT,cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±0.5 V		1		V/V
POWER SUPPLY					
Operating Range		2.7		11	V
Quiescent Current	V_{DIN+} = V_{DIN-} = V_{OCM} = 0 V		7.25		mA
Power Supply Rejection Ratio	$\Delta V_{OUT,dm}/\Delta V_S$; ΔV_S = ±0.5 V		–70		dB
OPERATING TEMPERATURE RANGE		–40		+85	°C

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1, 2]

Supply Voltage	±5.5 V
V_{OCM}	$\pm V_S$
Internal Power Dissipation	250 mW
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering 10 sec)	300°C

NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above listed in the operational section of this specification is not implied. Exposure to Absolute Maximum Ratings for any extended periods may affect device reliability.
[2]Thermal resistance measured on SEMI standard 4-layer board.
8-Lead SOIC: θ_{JA} = 121°C/W
8-Lead µSOIC: θ_{JA} = 142°C/W

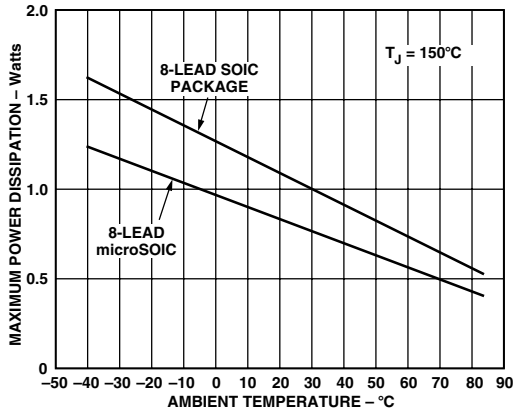
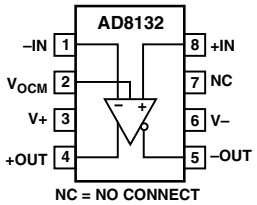


Figure 2. Plot of Maximum Power Dissipation vs. Temperature

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Function
1	–IN	Negative Input
2	V_{OCM}	Voltage applied to this pin sets the common-mode output voltage with a ratio of 1:1. For example, 1 V dc on V_{OCM} will set the dc bias level on +OUT and –OUT to 1 V.
3	V+	Positive Supply Voltage
4	+OUT	Positive Output. Note: the voltage at $-D_{IN}$ is inverted at +OUT.
5	–OUT	Negative Output. Note: the voltage at $+D_{IN}$ is inverted at –OUT.
6	V–	Negative Supply Voltage
7	NC	No Connect
8	+IN	Positive Input

PIN CONFIGURATION



ORDERING GUIDE

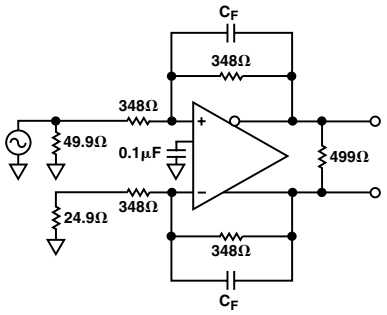
Model	Temperature Range	Package Description	Package Option	Branding Information
AD8132AR	–40°C to +85°C	8-Lead SOIC	SO-8	
AD8132AR-REEL[1]	–40°C to +85°C	8-Lead SOIC	13" Tape and Reel	
AD8132AR-REEL7[2]	–40°C to +85°C	8-Lead SOIC	7" Tape and Reel	
AD8132ARM	–40°C to +85°C	8-Lead µSOIC	RM-8	HMA
AD8132ARM-REEL[3]	–40°C to +85°C	8-Lead µSOIC	13" Tape and Reel	HMA
AD8132ARM-REEL7[2]	–40°C to +85°C	8-Lead µSOIC	7" Tape and Reel	HMA
AD8132-EVAL		Evaluation Board		

NOTES
[1]13" Reels of 2500 each.
[2]7" Reels of 1000 each.
[3]13" Reels of 3000 each.

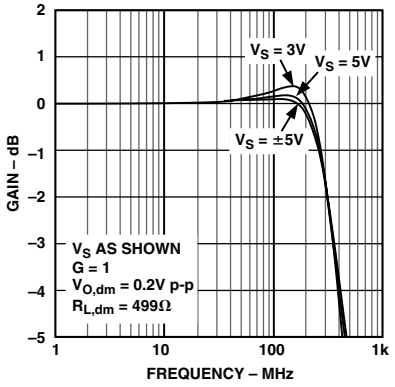
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD8132 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

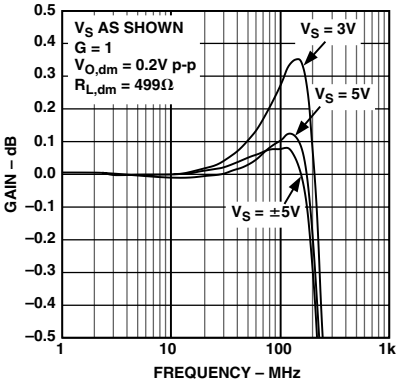
AD8132–Typical Performance Characteristics



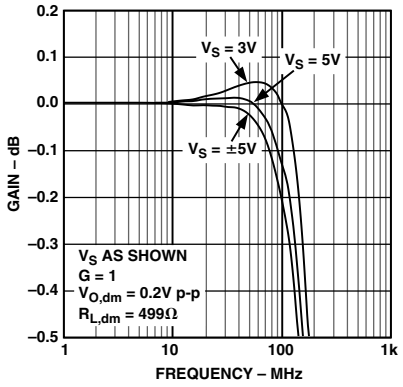
TPC 1. Basic Test Circuit, G = 1



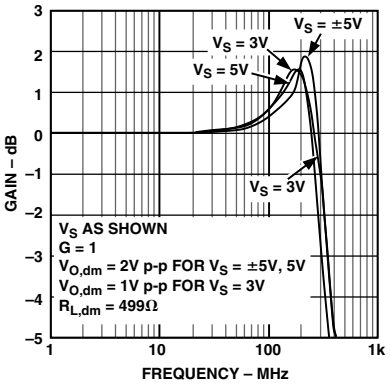
TPC 2. Small Signal Frequency Response



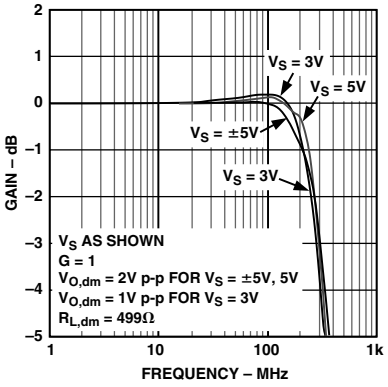
TPC 3. 0.1 dB Flatness vs. Frequency; C_F = 0 pF



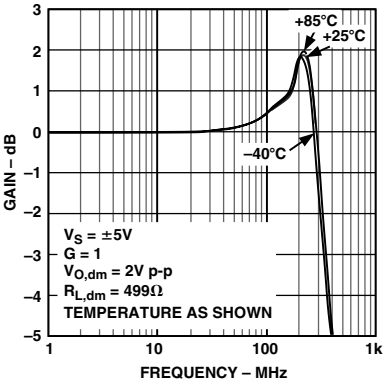
TPC 4. 0.1 dB Flatness vs. Frequency; C_F = 0.5 pF



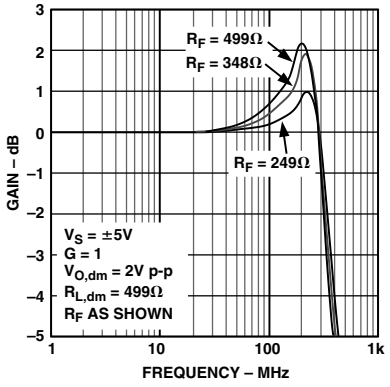
TPC 5. Large Signal Frequency Response; C_F = 0 pF



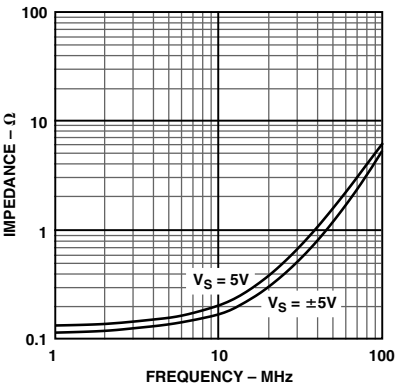
TPC 6. Large Signal Frequency Response; C_F = 0.5 pF



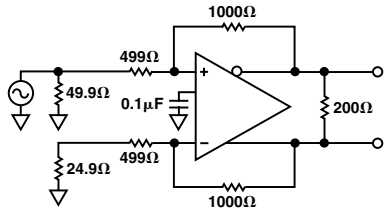
TPC 7. Large Signal Response vs. Temperature



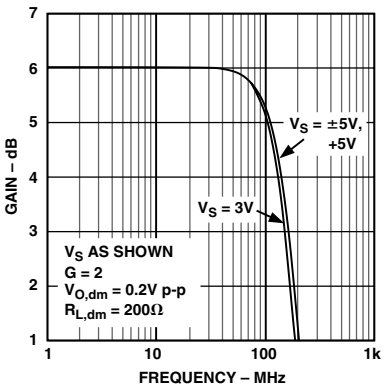
TPC 8. Large Signal Frequency Response vs. R_F



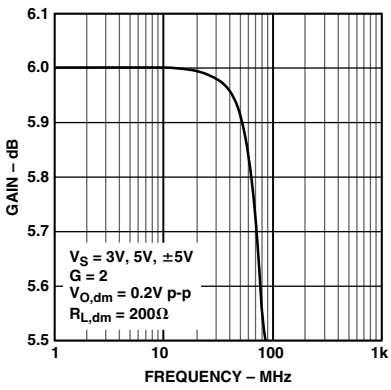
TPC 9. Closed-Loop Single-Ended Z_{OUT} vs. Frequency; G = 1



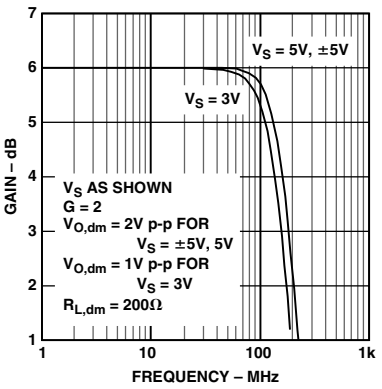
TPC 10. Basic Test Circuit, G = 2



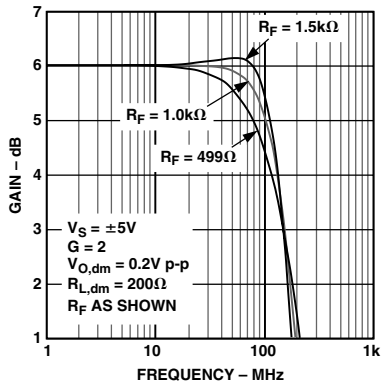
TPC 11. Small Signal Frequency Response



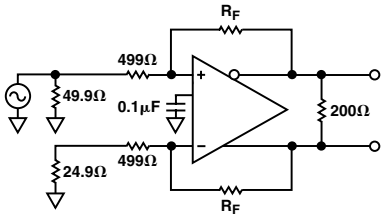
TPC 12. 0.1 dB Flatness vs. Frequency



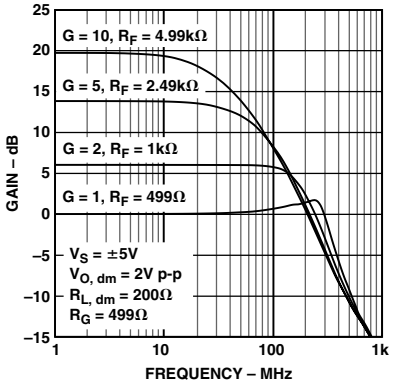
TPC 13. Large Signal Frequency Response



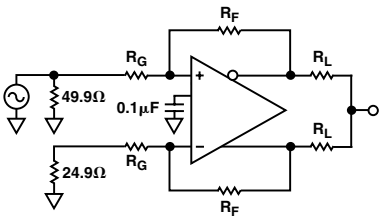
TPC 14. Small Signal Frequency Response vs. R_F



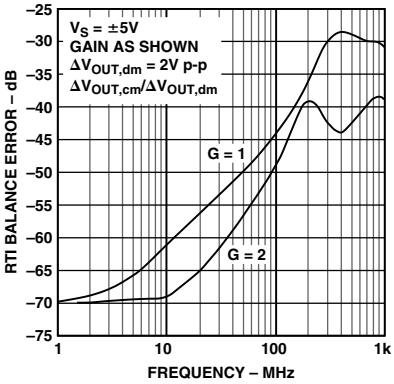
TPC 15. Test Circuit for Various Gains



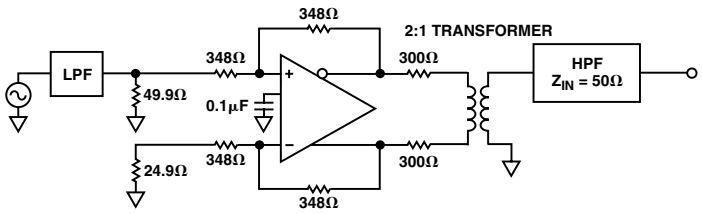
TPC 16. Large Signal Response for Various Gains



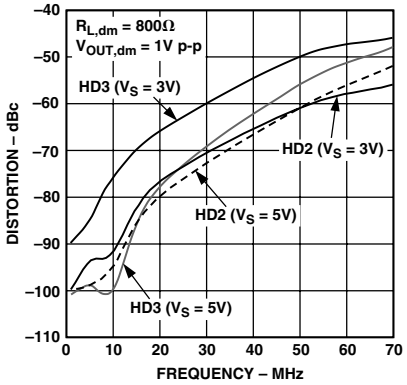
TPC 17. Test Circuit for Output Balance



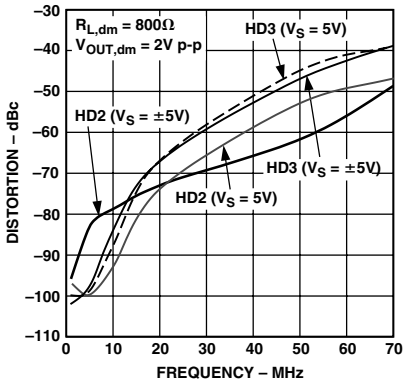
TPC 18. RTI Output Balance Error vs. Frequency



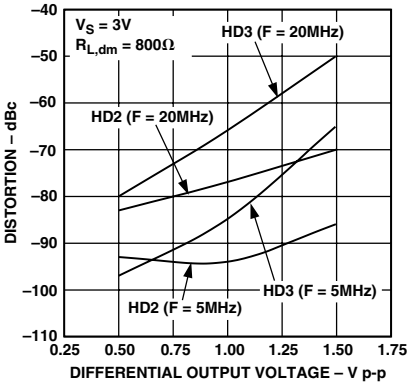
TPC 19. Harmonic Distortion Test Circuit, G = 1, $R_{L,dm}$ = 800 Ω



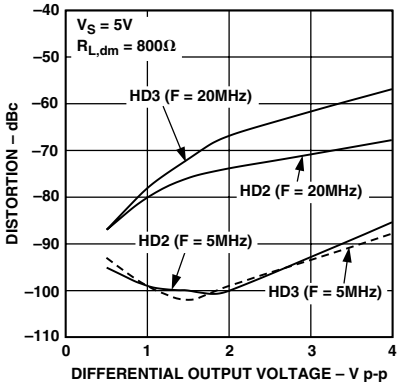
TPC 20. Harmonic Distortion vs. Frequency, G = 1



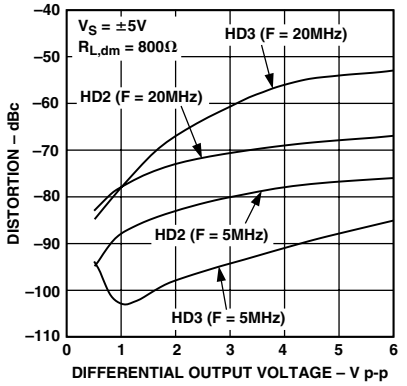
TPC 21. Harmonic Distortion vs. Frequency, G = 1



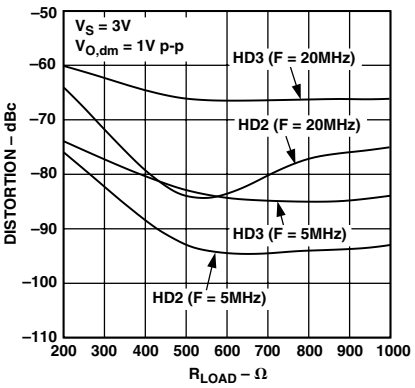
TPC 22. Harmonic Distortion vs. Differential Output Voltage, G = 1



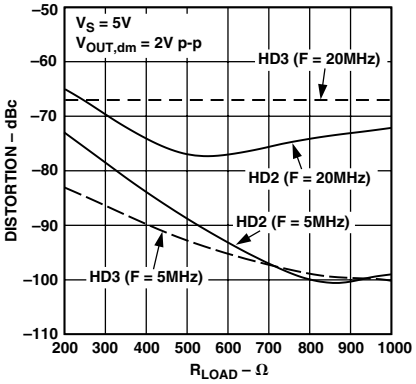
TPC 23. Harmonic Distortion vs. Differential Output Voltage, G = 1



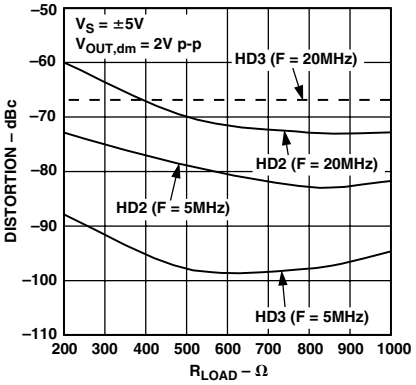
TPC 24. Harmonic Distortion vs. Differential Output Voltage, G = 1



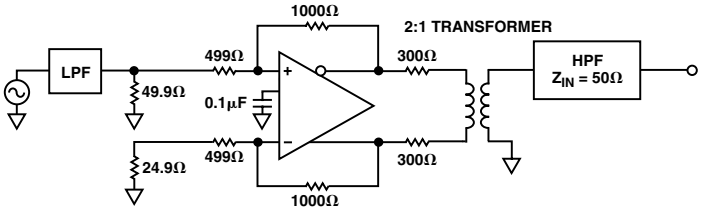
TPC 25. Harmonic Distortion vs. R_{LOAD}, G = 1



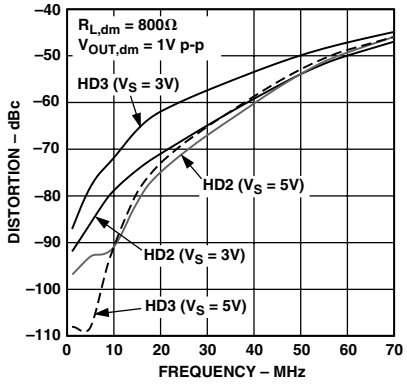
TPC 26. Harmonic Distortion vs. R_{LOAD}, G = 1



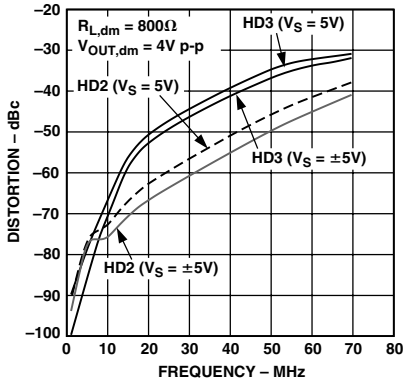
TPC 27. Harmonic Distortion vs. R_{LOAD}, G = 1



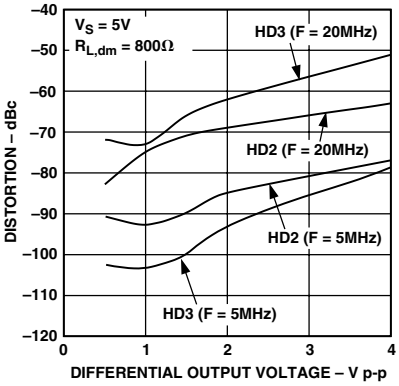
TPC 28. Harmonic Distortion Test Circuit, G = 2, $R_{L,dm}$ = 800 Ω



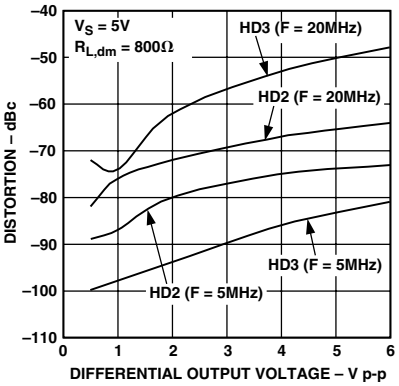
TPC 29. Harmonic Distortion vs. Frequency, G = 2



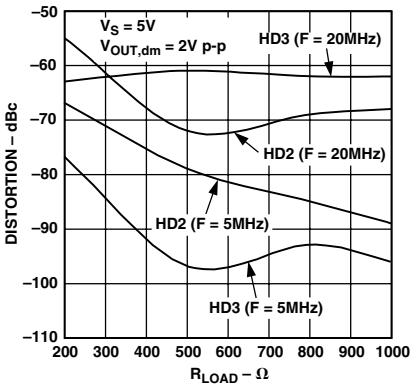
TPC 30. Harmonic Distortion vs. Frequency, G = 2



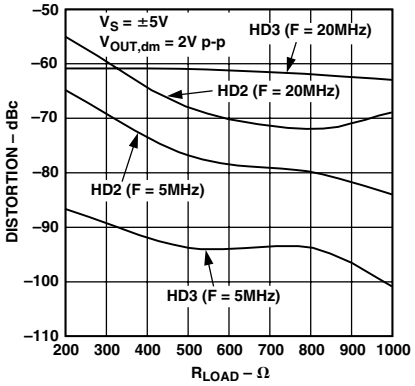
TPC 31. Harmonic Distortion vs. Differential Output Voltage, G = 2



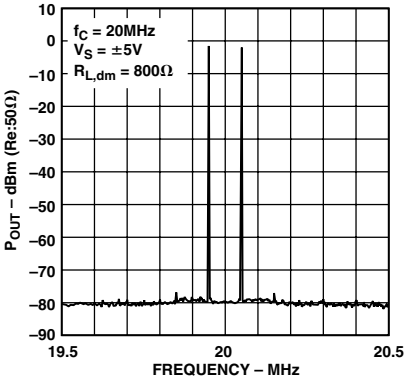
TPC 32. Harmonic Distortion vs. Differential Output Voltage, G = 2



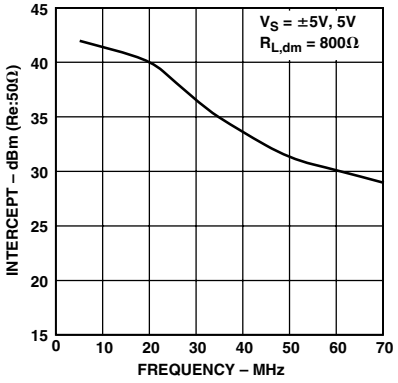
TPC 33. Harmonic Distortion vs. R_{LOAD}, G = 2



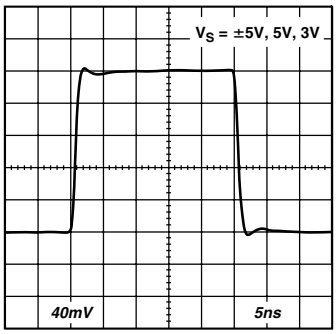
TPC 34. Harmonic Distortion vs. R_{LOAD}, G = 2



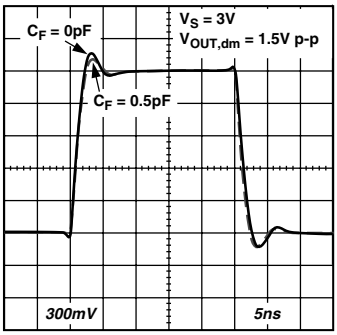
TPC 35. Intermodulation Distortion, G = 1



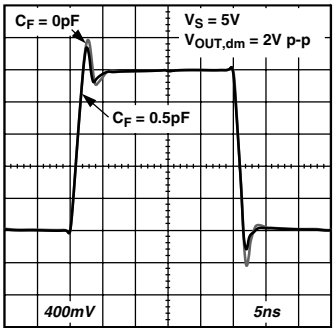
TPC 36. Third Order Intercept vs. Frequency, G = 1



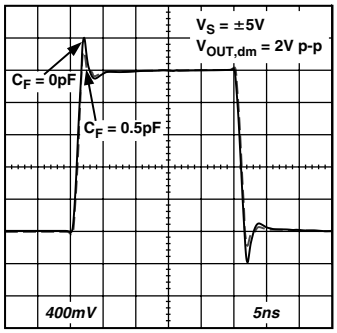
TPC 37. Small Signal Transient Response, G = 1



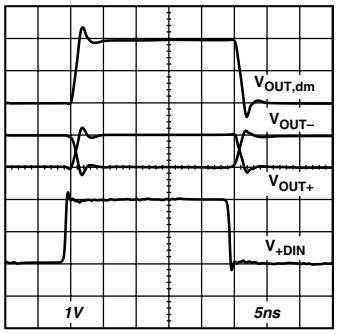
TPC 38. Large Signal Transient Response, G = 1



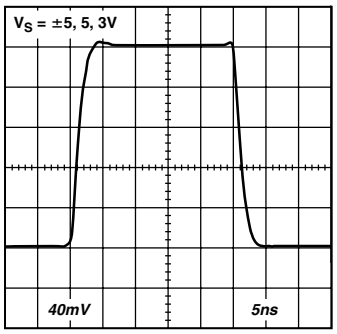
TPC 39. Large Signal Transient Response, G = 1



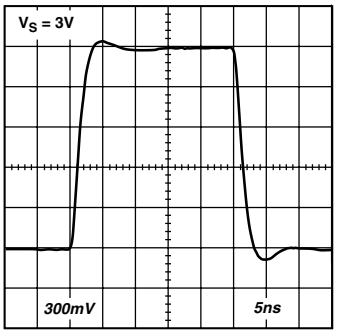
TPC 40. Large Signal Transient Response, G = 1



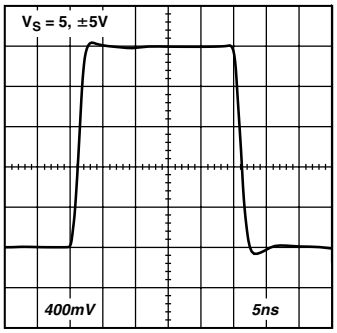
TPC 41. Large Signal Transient Response, G = 1



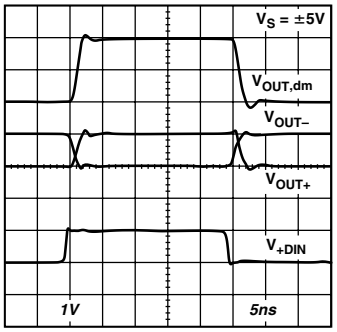
TPC 42. Small Signal Transient Response, G = 2



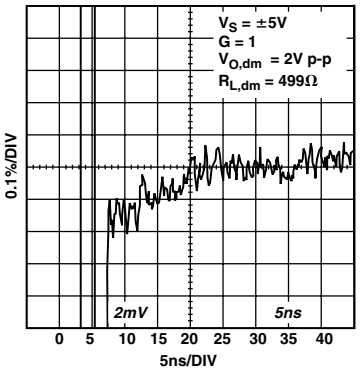
TPC 43. Large Signal Transient Response, G = 2



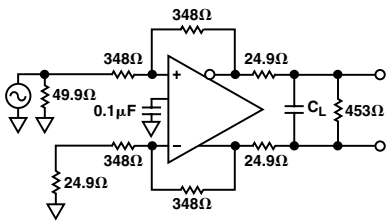
TPC 44. Large Signal Transient Response, G = 2



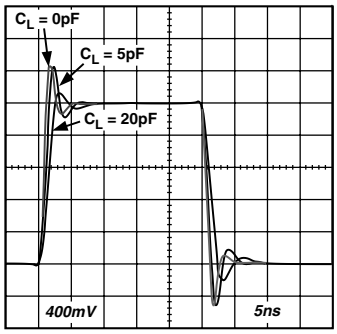
TPC 45. Large Signal Transient Response, G = 2



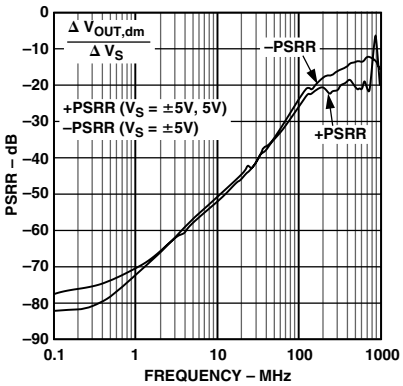
TPC 46. 0.1% Settling Time



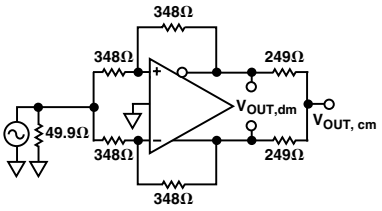
TPC 47. Test Circuit for Capacitor Load Drive



TPC 48. Large Signal Transient Response for Various Capacitor Loads

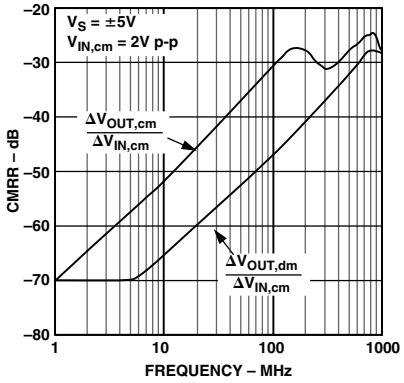


TPC 49. PSRR vs. Frequency

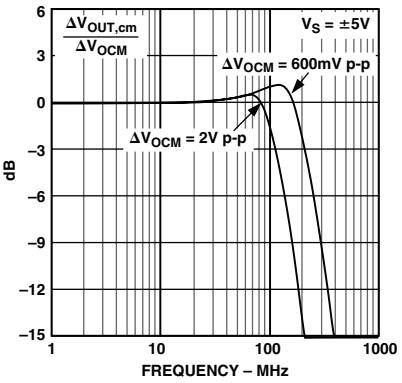


NOTE: RESISTORS MATCHED TO 0.01%.

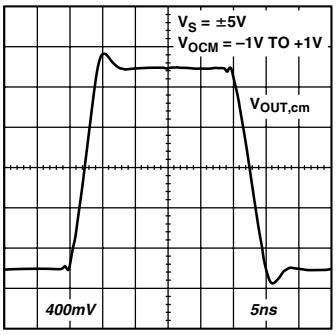
TPC 50. CMRR Test Circuit



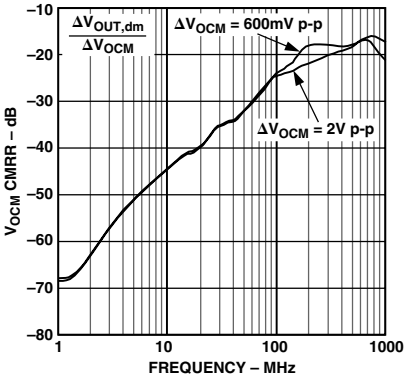
TPC 51. CMRR vs. Frequency



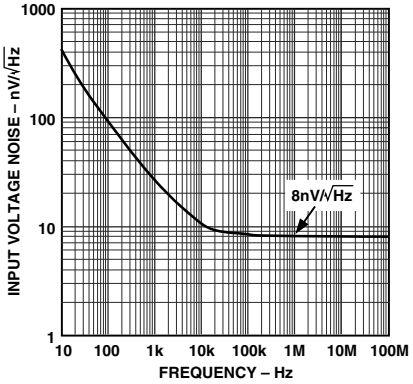
TPC 52. V_{OCM} Gain Response



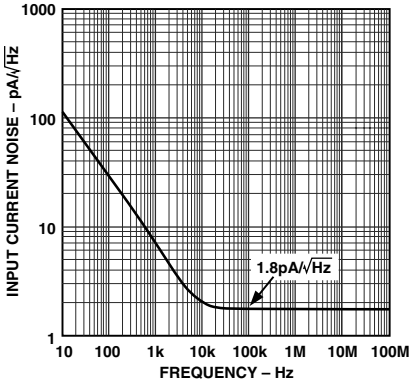
TPC 53. V_{OCM} Transient Response



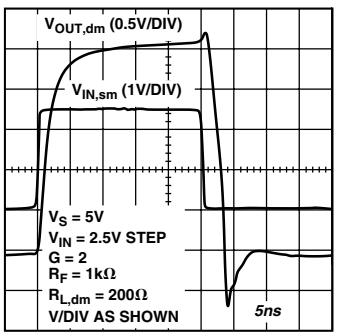
TPC 54. V_{OCM} CMRR vs. Frequency



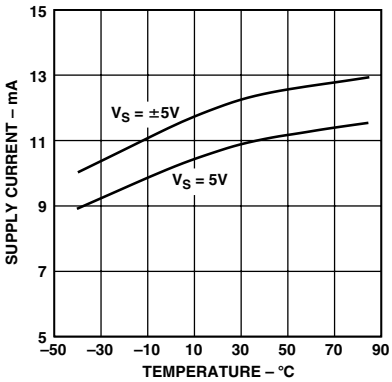
TPC 55. Input Voltage Noise vs. Frequency



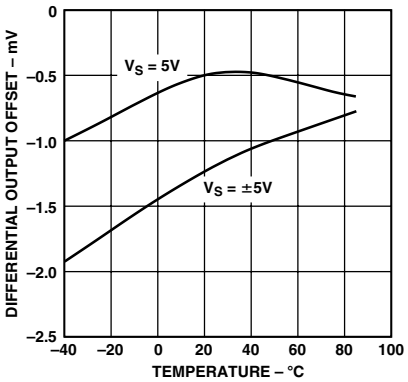
TPC 56. Input Current Noise vs. Frequency



TPC 57. Overdrive Recovery



TPC 58. Quiescent Current vs. Temperature



TPC 59. Differential Offset Voltage vs. Temperature

OPERATIONAL DESCRIPTION

Definition of Terms

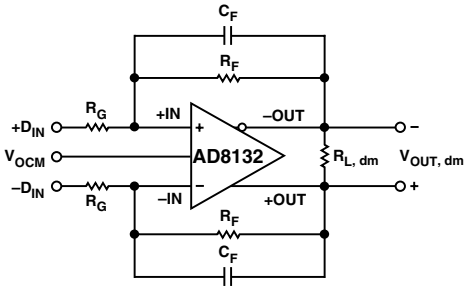


Figure 3. Circuit Definitions

Differential voltage refers to the difference between two node voltages. For example, the output differential voltage (or equivalently output differential-mode voltage) is defined as:

$$V_{OUT,dm} = \left(V_{+OUT} - V_{-OUT}\right)$$

V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and –OUT terminals with respect to a common reference.

Common-mode voltage refers to the average of two node voltages. The output common-mode voltage is defined as:

$$V_{OUT,cm} = \left(V_{+OUT} - V_{-OUT}\right) / 2$$

Basic Circuit Operation

One of the more useful and easy to understand ways to use the AD8132 is to provide two equal-ratio feedback networks. To match the effect of parasitics, these networks should actually be comprised of two equal-value feedback resistors, R_F and two equal-value gain resistors, R_G. This circuit is diagrammed in Figure 3.

Like a conventional op amp, the AD8132 has two differential inputs that can be driven with both a differential-mode input voltage, $V_{IN,dm}$, and a common-mode input voltage, $V_{IN,cm}$.

There is another input, V_{OCM}, which is not present on conventional op amps, but provides another input to consider on the AD8132. It is totally separate from the above inputs.

There are two complementary outputs whose response can be defined by a differential-mode output, $V_{OUT,dm}$ and a common-mode output, $V_{OUT,cm}$.

Table I indicates the gain from any type of input to either type of output.

Table I. Differential and Common-Mode Gains

Input	$V_{OUT,dm}$	$V_{OUT,cm}$
$V_{IN,dm}$	R_F/R_G	0 (By Design)
$V_{IN,cm}$	0	0 (By Design)
V_{OCM}	0	1 (By Design)

The differential output ($V_{OUT,dm}$) is equal to the differential input voltage ($V_{IN,dm}$) times R_F/R_G. In this case, it does not matter if both differential inputs are driven, or only one output is driven and the other is tied to a reference voltage, like ground. As can be seen from the two zero entries in the first column, neither of the common-mode inputs has any effect on this gain.

The gain from $V_{IN,dm}$ to $V_{OUT,cm}$ is 0 and to first order does not depend on the ratio matching of the feedback networks. The common-mode feedback loop within the AD8132 provides a corrective action to keep this gain term minimized. The term "balance error" describes the degree to which this gain term differs from zero.

The gain from $V_{IN,cm}$ to $V_{OUT,dm}$ does directly depend on the matching of the feedback networks. The analogous term for this transfer function, which is used in conventional op amps, is "common-mode rejection ratio" or CMRR. Thus, if it is desirable to have a high CMRR, the feedback ratios must be well matched.

The gain from $V_{IN,cm}$ to $V_{OUT,cm}$ is also ideally 0, and is first-order independent of the feedback ratio matching. As in the case of $V_{IN,dm}$ to $V_{OUT,cm}$, the common-mode feedback loop keeps this term minimized.

The gain from V_{OCM} to $V_{OUT,dm}$ is ideally 0 only when the feedback ratios are matched. The amount of differential output signal that will be created by varying V_{OCM} is related to the degree of mismatch in the feedback networks.

V_{OCM} controls the output common-mode voltage $V_{OUT,cm}$ with a unity-gain transfer function. With equal-ratio feedback networks (as assumed above), its effect on each output will be the same, which is another way to say that the gain from V_{OCM} to $V_{OUT,dm}$ is zero. If not driven, the output common-mode will be at mid-supplies. It is recommended that a 0.1 µF bypass capacitor be connected to V_{OCM}.

When unequal feedback ratios are used, the two gains associated with $V_{OUT,dm}$ become nonzero. This significantly complicates the mathematical analysis along with any intuitive understanding of how the part operates. Some of these configurations will be in another section.

THEORY OF OPERATION

The AD8132 differs from conventional op amps by the external presence of an additional input and output. The additional input, V_{OCM}, controls the output common-mode voltage. The additional output is the analog complement of the single output of a conventional op amp. For its operation, the AD8132 makes use of two feedback loops as compared to the single loop of conventional op amps. While this provides significant freedom to create various novel circuits, basic op amp theory can still be used to analyze the operation.

One of the feedback loops controls the output common-mode voltage, $V_{OUT,cm}$. Its input is V_{OCM} (Pin 2) and the output is the common-mode, or average voltage, of the two differential outputs (+OUT and –OUT). The gain of this circuit is internally set to unity. When the AD8132 is operating in its linear region, this establishes one of the operational constraints: $V_{OUT,cm} = V_{OCM}$.

The second feedback loop controls the differential operation. Similar to an op amp, the gain and gain-shaping of the transfer function is controllable by adding passive feedback networks. However, only one feedback network is required to "close the loop" and fully constrain the operation. But depending on the function desired, two feedback networks can be used. This is possible as a result of having two outputs that are each inverted with respect to the differential inputs.

General Usage of the AD8132

Several assumptions are made here for a first-order analysis, which are the typical assumptions used for the analysis of op amps:

- The input impedances are arbitrarily large and their loading effect can be ignored.
- The input bias currents are sufficiently small so they can be neglected.
- The output impedances are arbitrarily low.
- The open-loop gain is arbitrarily large, which drives the amplifier to a state where the input differential voltage is effectively zero.
- Offset voltages are assumed to be zero.

While it is possible to operate the AD8132 with a purely differential input, many of its applications call for a circuit that has a single-ended input with a differential output.

For a single-ended-to-differential circuit, the R_G of the undriven input will be tied to a reference voltage. For now this is ground, and other conditions will be discussed later. Also, the voltage at V_{OCM}, and hence $V_{OUT,cm}$ will be assumed to be ground for now. Figure 4 shows a generalized schematic of such a circuit using an AD8132 with two feedback paths.

For each feedback network, a feedback factor can be defined, which is the fraction of the output signal that is fed back to the opposite-sign input. These terms are:

$$\beta 1 = R_{G1} / \left(R_{G1} + R_{F1}\right)$$

$$\beta 2 = R_{G2} / \left(R_{G2} + R_{F2}\right)$$

The feedback factor β1 is for the side that is driven, while the feedback factor β2 is for the side that is tied to a reference voltage, (ground for now). Note also that each feedback factor can vary anywhere between 0 and 1.

A single-ended-to-differential gain equation can be derived which is true for all values of β1 and β2:

$$G = 2 \times \left(1 - \beta 1\right) / \left(\beta 1 + \beta 2\right)$$

This expression is not very intuitive, but some further examples can provide better understanding of its implications. One observation that can be made right away is that a tolerance error in β1 does not have the same effect on gain as the same tolerance error in β2.

Resistorless Differential Amplifier (High Input Impedance Inverting Amplifier)

The simplest closed-loop circuit that can be made does not require any resistors and is shown in Figure 7. In this circuit, β1 is equal to zero, and β2 is equal to one. The gain is equal to two.

A more intuitive means to figure the gain is by simple inspection. +OUT is connected to –IN, whose voltage is equal to the voltage at +IN under equilibrium conditions. Thus, $+V_{OUT}$ is equal to V_{IN}, and there is unity gain in this path. Since –OUT has to swing in the opposite direction from +OUT due to the common-mode constraint, its effect will double the output signal and produce a gain of two.

One useful function that this circuit provides is a high input-impedance inverter. If +OUT is ignored, there is a unity-gain, high-input-impedance amplifier formed from +IN to –OUT. Most traditional op amp inverters have relatively low input impedances, unless they are buffered with another amplifier.

V_{OCM} has been assumed to be at midsupply. Since there is still the constraint from the above discussion that $+V_{OUT}$ must equal V_{IN}, changing the V_{OCM} voltage will not change $+V_{OUT}$ ($= V_{IN}$). Therefore, all of the effect of changing V_{OCM} must show up at –OUT.

For example, if V_{OCM} is raised by 1 V, then $-V_{OUT}$ must go up by 2 V. This makes $V_{OUT,cm}$ also go up by 1 V, since it is defined as the average of the two differential output voltages. This means that the gain from V_{OCM} to the differential output is two.

Other β2 = 1 Circuits

The above simple configuration with β2 = 1 and its gain-of-two is the highest gain circuit that can be made under this condition. Since β1 was equal to zero, only higher β1 values are possible. All of these circuits with higher values of β1 will have gains lower than two. However, circuits with β1 equal to one are not practical, because they have no effective input, and result in a gain of 0.

To increase β1 from zero, it is necessary to add two resistors in a feedback network. A generalized circuit that has β1 with a value higher than zero is shown in Figure 6. A couple of different convenient gains that can be created are a gain of 1, when β1 is equal to 1/3, and a gain of 0.5 when β1 equals 0.6.

In all of these circuits with β2 equal to 1, V_{OCM} serves as the reference voltage from which to measure the input voltage and the individual output voltages. In general, when V_{OCM} is varied in these circuits, a differential output signal will be generated in addition to $V_{OUT,cm}$ changing the same amount as the voltage change of V_{OCM}.

Varying β2

While the circuit above sets β2 to 1, another class of simple circuits can be made that set β2 equal to zero. This means that there is no feedback from +OUT to –IN. This class of circuits is very similar to a conventional inverting op amp. However, the AD8132 circuits have an additional output and common-mode input which can be analyzed separately (see Figure 8).

With –IN connected to ground, +IN becomes a "virtual ground" in the same sense that the term is used in conventional op amps. Both inputs must maintain the same voltage for equilibrium operation, so if one is set to ground, the other will be driven to ground. The input impedance can also be seen to be equal to R_G, just as in a conventional op amp.

In this case, however, the positive input and negative output are used for the feedback network. Since a conventional op amp does not have a negative output, only its inverting input can be used for the feedback network. The AD8132 is symmetrical, so the feedback network on either side can be used to produce the same results.

Since +IN is a summing junction, by analogy to conventional op amps, the gain from V_{IN} to –OUT will be $-R_F/R_G$. This will hold true regardless of the voltage on V_{OCM}. And since +OUT will move the same amount in the opposite direction from –OUT, the overall gain will be –2 (R_F/R_G).

V_{OCM} still governs $V_{OUT,cm}$, so +OUT must be the only output that moves when V_{OCM} is varied. Since $V_{OUT,cm}$ is the average of the two outputs, +OUT must move twice as fast and in the same direction as V_{OCM} to create the proper $V_{OUT,cm}$. Therefore, the gain from V_{OCM} to +OUT must be two.

In these circuits with β2 equal to zero, the gain can theoretically be set to any value from close to zero to infinity, just as it can with a conventional op amp in the inverting mode. However, practical real-world limitations and parasitics will limit the range of acceptable gains to more modest values.

β1 = 0

There is yet another class of circuits where there is no feedback from –OUT to +IN. This is the case where β1 = 0. The resistorless differential amplifier described above meets this condition, but it was presented only with the condition that β2 = 1. Recall that this circuit had a gain equal to two.

If β2 is decreased in this circuit from unity, a smaller part of $+V_{OUT}$ will be fed back to –IN and the gain will increase. See Figure 5. This circuit is very similar to a noninverting op amp configuration, except for the presence of the additional complementary output. Therefore, the overall gain is twice that of a noninverting op amp or $2 \times (1 + R_{F2}/R_{G2})$ or $2 \times (1/\beta 2)$.

Once again, varying V_{OCM} will not affect both outputs in the same way, so in addition to varying $V_{OUT,cm}$ with unity gain, there will also be an affect on $V_{OUT,dm}$ by changing V_{OCM}.

Estimating the Output Noise Voltage

Similar to the case of a conventional op amp, the differential output errors (noise and offset voltages) can be estimated by multiplying the input referred terms, at +IN and –IN, by the circuit noise gain. The noise gain is defined as:

$$G_N = 1 + \left(\frac{R_F}{R_G}\right)$$

To compute the total output referred noise for the circuit of Figure 3, consideration must also be given to the contribution of the resistors R_F and R_G. Refer to Table II for estimated output noise voltage densities at various closed-loop gains.

Table II. Recommended Resistor Values and Noise Performance for Specific Gains

Gain	R_G (Ω)	R_F (Ω)	Bandwidth –3 dB	Output Noise AD8132 Only	Output Noise AD8132 + R_G, R_F
1	499	499	360 MHz	16 nV/√Hz	17 nV/√Hz
2	499	1.0 k	160 MHz	24.1 nV/√Hz	26.1 nV/√Hz
5	499	2.49 k	65 MHz	48.4 nV/√Hz	53.3 nV/√Hz
10	499	4.99 k	20 MHz	88.9 nV/√Hz	98.6 nV/√Hz

Calculating an Application Circuit's Input Impedance

The effective input impedance of a circuit such as that in Figure 3, at $+D_{IN}$ and $-D_{IN}$, will depend on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance (R_{IN},dm) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply:

$$R_{IN,dm} = 2 \times R_G$$

In the case of a single-ended input signal (for example if $-D_{IN}$ is grounded and the input signal is applied to $+D_{IN}$), the input impedance becomes:

$$R_{IN,dm} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}}\right)$$

The circuit's input impedance is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

Input Common-Mode Voltage Range in Single Supply Applications

The AD8132 is optimized for level-shifting "ground" referenced input signals. For a single-ended input this would imply, for example, that the voltage at $-D_{IN}$ in Figure 3 would be zero volts when the amplifier's negative power supply voltage (at V–) was also set to zero volts.

Setting the Output Common-Mode Voltage

The AD8132's V_{OCM} pin is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on V+ and V–). Relying on this internal bias will result in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (with $R_{SOURCE} < 10K$), be used. The output common-mode offset specified on pages 2 and 3 assume the V_{OCM} input is driven by a low impedance voltage source.

Driving a Capacitive Load

A purely capacitive load can react with the pin and bondwire inductance of the AD8132 resulting in high frequency ringing in the pulse response. One way to minimize this effect is to place a small capacitor across each of the feedback resistors. The added capacitance should be small to avoid destabilizing the amplifier. An alternative technique is to place a small resistor in series with the amplifier's outputs as shown in TPC 47.

LAYOUT, GROUNDING AND BYPASSING

As a high-speed part, the AD8132 is sensitive to the PCB environment in which it has to operate. Realizing its superior specifications requires attention to various details of good high-speed PCB design.

The first requirement is a good solid ground plane that covers as much of the board area around the AD8132 as possible. The only exception to this is that the two input pins (Pins 1 and 8) should be kept a few mm from the ground plane, and ground should be removed from inner layers and the opposite side of the board under the input pins. This will minimize the stray capacitance on these nodes and help preserve the gain flatness vs. frequency.

The power supply pins should be bypassed as close as possible to the device to the nearby ground plane. Good high-frequency ceramic chip capacitors should be used. This bypassing should be done with a capacitance value of 0.01 μF to 0.1 μF for each supply. Further away, low frequency bypassing should be provided with 10 μF tantalum capacitors from each supply to ground.

The signal routing should be short and direct in order to avoid parasitic effects. Wherever there are complementary signals, a symmetrical layout should be provided to the extent possible to maximize the balance performance. When running differential signals over a long distance, the traces on PCB should be close together or any differential wiring should be twisted together to minimize the area of the loop that is formed. This will reduce the radiated energy and make the circuit less susceptible to interference.

CIRCUITS

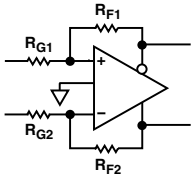


Figure 4. Typical Four-Resistor Feedback Circuit

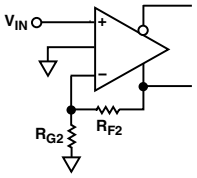


Figure 5. Typical Circuit with β1 = 0

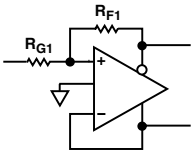


Figure 6. Typical Circuit with β2 = 1

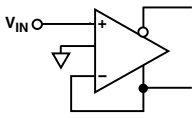


Figure 7. Resistorless G = 2 Circuit with β1 = 0

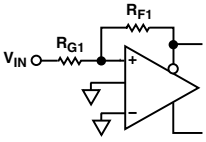


Figure 8. Typical Circuit with β2 = 0

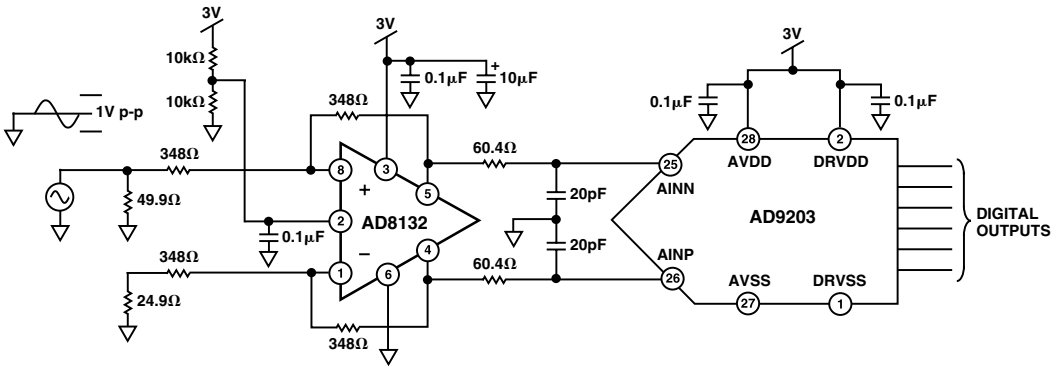


Figure 9. AD8132 Driving AD9203, a 10-Bit 40 MSPS A/D Converter

APPLICATIONS

A/D Driver

Many of the newer high-speed A/D converters are single-supply and have differential inputs. Thus, the driver for these devices should be able to convert from a single-ended to a differential signal and provide output common-mode level-shifting in addition to having low distortion and noise. The AD8132 conveniently performs these functions when driving the AD9203, a 10-bit, 40 MSPS A/D converter.

In Figure 9 a 1 V p-p signal drives the input of an AD8132 configured for unity gain. Both the AD8132 and the AD9203 are powered from a single 3 V supply. A voltage divider biases V_{OCM} at midsupply, which in turn drives $V_{OUT,cm}$ to be half the supply voltage. This is within the common-mode range of the AD9203.

Between the A/D and the driver is a one-pole, differential filter that helps to filter some of the noise and assists the switched-capacitor inputs of the A/D. Each of the A/D inputs will be driven by a 0.5 V p-p signal that goes from 1.25 V dc to 1.75 V dc.

Figure 10 is an FFT plot of the performance of the circuit when running at a clock rate of 40 MSPS and an input frequency of 2.5 MHz.

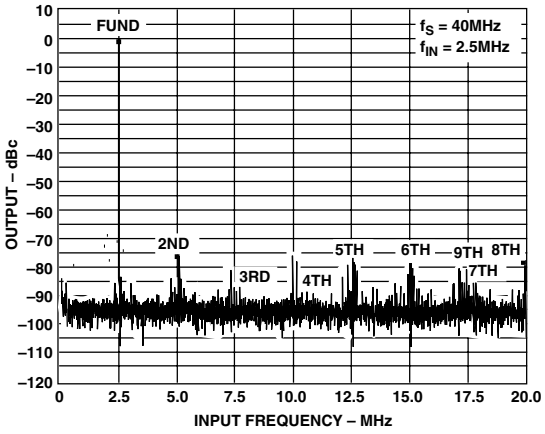


Figure 10. FFT Response for AD8132 Driving AD9203

Balanced Cable Driver

When driving a twisted pair cable, it is desirable to drive only a pure differential signal onto the line. If the signal is purely differential (i.e., fully balanced), and the transmission line is twisted and balanced, there will be a minimum radiation of any signal.

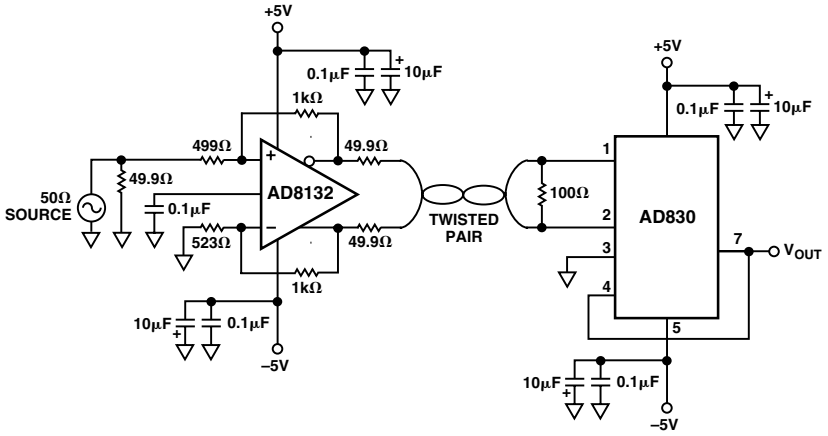


Figure 11. Balanced Line Driver and Receiver Using AD8132 and AD830

The complementary electrical fields will mostly be confined to the space between the two twisted conductors and will not significantly radiate out from the cable. The current in the cable will create magnetic fields that will radiate to some degree. However, the amount of radiation is mitigated by the twists, because for each twist, the two adjacent twists will have an opposite polarity magnetic field. If the twist pitch is tight enough, these small magnetic field loops will contain most of the magnetic flux, and the magnetic far-field strength will be negligible.

Any imbalance in the differential drive signal will appear as a common-mode signal on the cable. This is the equivalent of a single wire that is driven with the common-mode signal. In this case, the wire will act as an antenna and radiate. Thus, in order to minimize radiation when driving differential twisted pair cables, the differential drive signal should be very well balanced.

The common-mode feedback loop in the AD8132 helps to minimize the amount of common-mode voltage at the output, and can therefore be used to create a well-balanced differential line driver. Figure 11 shows an application that uses an AD8132 as a balanced line driver and AD830 as a differential receiver configured for unity gain. This circuit was operated with 10 m of Category 5 cable.

Transmit Equalizer

Any length of transmission line will attenuate the signals it carries. This effect is worse at higher frequencies than at low frequencies. One way to compensate for this is to provide an equalizer circuit that boosts the higher frequencies in the transmitter circuit, so that at the receive end of the cable, the attenuation effects are diminished.

By lowering the impedance of the R_G component of the feedback network at higher frequency, the gain can be increased at high frequency. Figure 12 shows a gain of a two line driver that has its R_Gs shunted by 10 pF capacitors. The effect of this is shown in the frequency response plot of Figure 13.

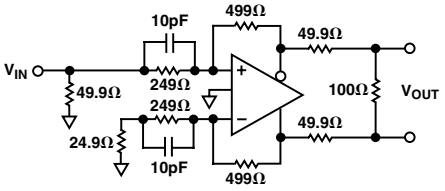


Figure 12. Frequency Boost Circuit

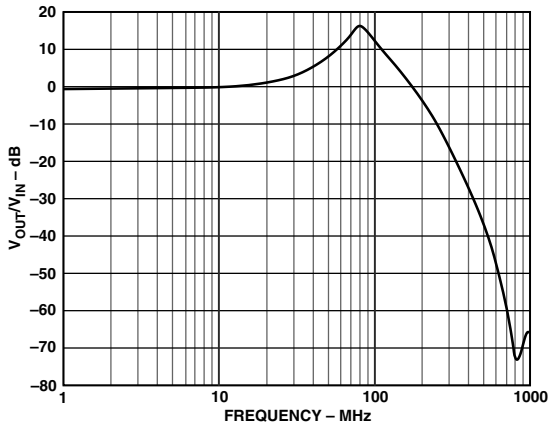


Figure 13. Frequency Response for Transmit Boost Circuit

Low-Pass Differential Filter

Similar to an op amp, various types of active filters can be created with the AD8132. These can have single-ended inputs and differential outputs, which can provide an antialias function when driving a differential A/D converter.

Figure 14 is a schematic of a low-pass, multiple-feedback filter. The active section contains two poles, and an additional pole is added at the output. The filter was designed to have a –3 dB frequency of 1 MHz. The actual –3 dB frequency was measured to be 1.12 MHz as shown in Figure 15.

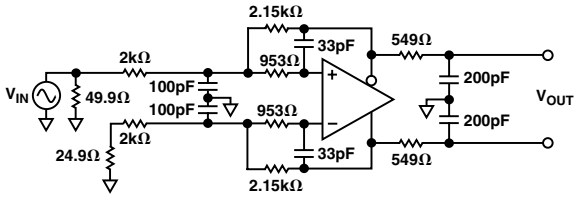


Figure 14. 1 MHz, 3-Pole Differential Output Low-Pass Multiple Feedback Filter

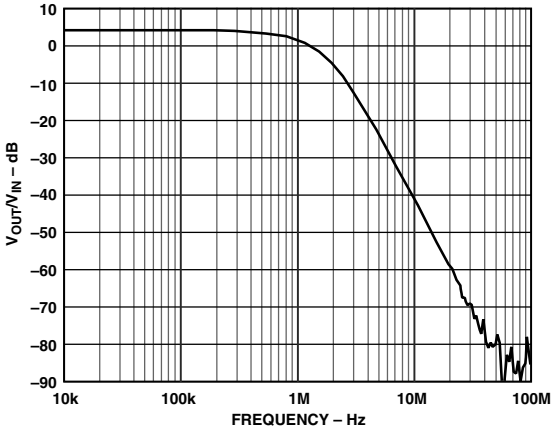


Figure 15. Frequency Response of 1 MHz Low-Pass Filter

High Common-Mode Output Impedance Amplifier

Changing the connection to V_{OCM} (Pin 2) can change the common-mode from low impedance to high impedance. If V_{OCM} is actively set to a particular voltage, the AD8132 will try to force $V_{OUT,cm}$ to the same voltage with a relatively low output impedance. All the previous analysis assumed that this output impedance is arbitrarily low enough to drive the load condition in the circuit.

However, the are some applications that benefit from a high common-mode output impedance. This can be accomplished with the circuit shown in Figure 16.

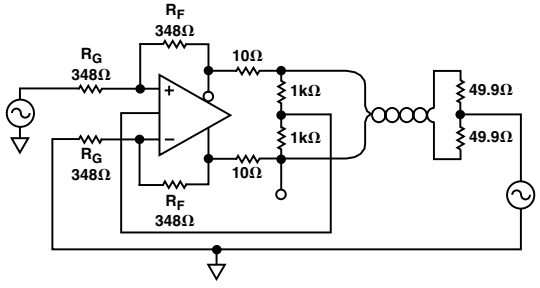


Figure 16. High Common-Mode Output Impedance Differential Amplifier

V_{OCM} is driven by a resistor divider that "measures" the output common- mode voltage. Thus, the common-mode output voltage takes on the value that is set by the driven circuit. In this case it comes from the center point of the termination at the receive end of a 10 m length of Category 5 twisted pair cable.

If the receive end common-mode voltage is set to "ground," it will be well-defined at the receive end. Any common-mode signal that is picked up over the cable length due to noise, will appear at the transmit end, and must be "absorbed" by the transmitter. Thus, it is important that the transmitter have adequate common-mode output range to absorb the full amplitude of the common-mode signal coupled onto the cable and thus prevent clipping.

Another way to look at this is that the circuit performs what is sometimes called "transformer action." One main difference is that the AD8132 passes dc while transformers do not.

A transformer can also be easily configured to have either a high or low common-mode output impedance. If the transformer's center tap is connected to a solid voltage reference, it will set the common-mode voltage on the secondary side of the transformer. In this case, if one of the differential outputs is grounded, the other output will have only half of the differential output signal. This keeps the common-mode voltage at ground, where it is required to be due to the center tap connection. This is analogous to the AD8132 operating with a low output impedance common-mode. See Figure 17.

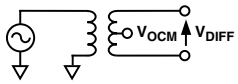


Figure 17. Transformer Whose Low Output Impedance Secondary Is Set at V_{OCM}

If the center tap of the secondary of a transformer is allowed to float (or there is no center tap), the transformer will have a high common-mode output impedance. This means that the common-mode of the secondary will be determined by what it is connected to, and not by anything to do with the transformer itself.

If one of the differential ends of the transformer is grounded, the other end will swing with the full output voltage. This means that the common-mode of the output voltage is one-half of the differential output voltage. But this shows that the common-mode is not forced via a low impedance to a given voltage. The common-mode output voltage can easily be changed to any voltage through its other output terminals.

The AD8132 can exhibit the same performance when one of the outputs in Figure 16 is grounded. The other output will swing at the full differential output voltage. The common-mode signal is "measured" by the voltage divider across the outputs and input to V_{OCM}. This then drives $V_{OUT,cm}$ to the same level. At higher frequencies, it is important to minimize the capacitance on the V_{OCM} node or else phase shifts can compromise the performance. The voltage divider resistances can also be lowered for better frequency response.

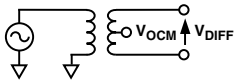


Figure 18. Transformer with High Output Impedance Secondary

Full-Wave Rectifier

The balanced outputs of the AD8132, along with a couple of Schottky diodes, can create a very high-speed full-wave rectifier. Such circuits are useful for measuring ac voltages and other computational tasks.

Figure 19 shows the configuration of such a circuit. Each of the AD8132 outputs drives the anode of an HP2835 Schottky diode. These Schottky diodes were chosen for their high-speed operation. At lower frequencies (approximately lower than 10 MHz), a silicon signal diode, like a 1N4148 can be used. The cathodes of the two diodes are connected together and this output node is connected to ground by a 50 Ω resistor.

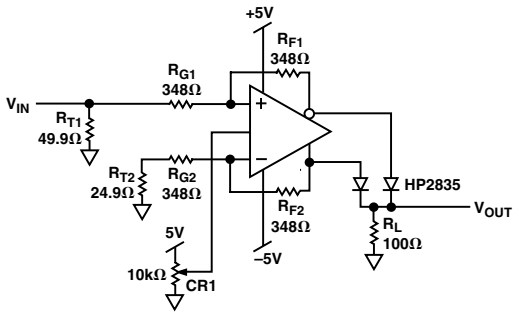


Figure 19. Full-Wave Rectifier

The diodes should be operated such that they are slightly forward-biased when the differential output voltage is zero. For the Schottky diodes, this is about 400 mV. The forward biasing can be conveniently adjusted by CR1, which, in this circuit, raises and lowers $V_{OUT,CM}$ without creating a differential output voltage.

One advantage of this circuit is that the feedback loop is never momentarily opened while the diodes reverse their polarity within the loop. This is the scheme that is sometimes used for full-wave rectifiers that use conventional op amps. These conventional circuits do not work well at frequencies above about 1 MHz.

If there is not enough forward bias ($V_{OUT,cm}$ too low), the lower sharp cusps of the full-wave rectified output waveform will be rounded off. Also, as the frequency increases, there tends to be some rounding of the lower cusps. The forward bias can be increased to yield sharper cusps at higher frequencies.

There is not a reliable, entirely quantifiable, means to measure the performance of a full-wave rectifier. Since the ideal waveform has periodic sharp discontinuities, it should have (mostly even) harmonics that have no upper bound on the frequency. However, for a practical circuit, as the frequency increases, the higher harmonics become attenuated and the sharp cusps that are present at low frequencies become significantly rounded.

The circuit was run at a frequency up to 300 MHz and, while it was still functional, the major harmonic that remained in the output was the second. This made it look like a sine wave at 600 MHz. Figure 20 is an oscilloscope plot of the output when driven by a 100 MHz, 2.5 V p-p input.

Sometimes a second harmonic generator is actually useful, as for creating a clock to oversample a DAC by a factor of two. If the output of this circuit is run through a low-pass filter, it can be used as a second harmonic generator.

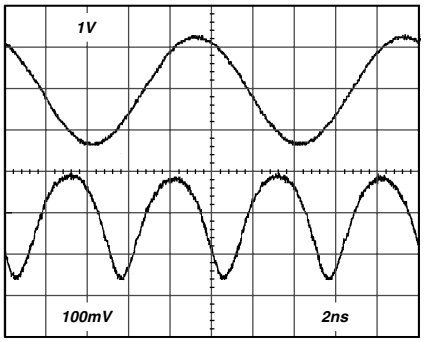


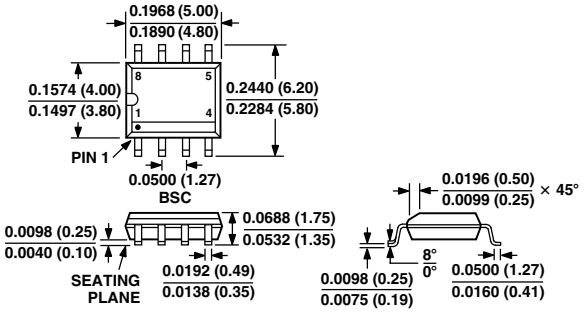
Figure 20. Full-Wave Rectifier Response with 100 MHz Input

C01035–0–1/02(B)

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead SOIC (R-8)



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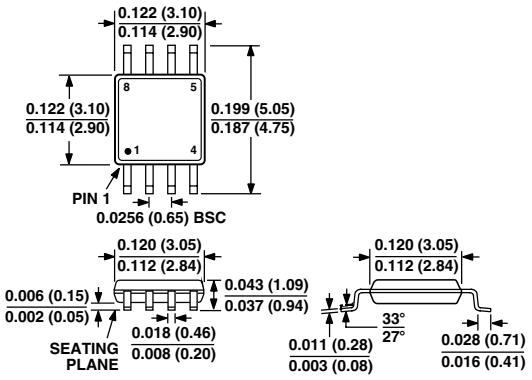
8-Lead microSOIC (RM-8)



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Revision History

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