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# <0.5 $\Omega$ CMOS, Low Voltage, SPST Switches

## ADG801/ADG802

### FEATURES

Low On Resistance < 0.5  $\Omega$  max at 5 V supply  
 0.1  $\Omega$  On Resistance Flatness  
 +1.8 V to +5.5 V Single Supply  
 100pA Leakage Currents  
 14ns Switching Times  
 Extended Temperature Range -40°C to +125°C  
 High Current Carrying Capability  
 Tiny 6 lead SOT23 and 8 Lead  $\mu$ SOIC Packages  
 Low Power Consumption  
 TTL/CMOS Compatible Inputs  
 Pin Compatible with ADG701/ADG702

### APPLICATIONS

Power Routing  
 Audio and Video Signal Routing  
 Cellular Phones  
 Modems  
 PCMCIA Cards  
 Hard Drives  
 Data Acquisition Systems  
 Communication Systems  
 Relay replacement  
 Audio and Video Switching  
 Battery Powered Systems

### GENERAL DESCRIPTION

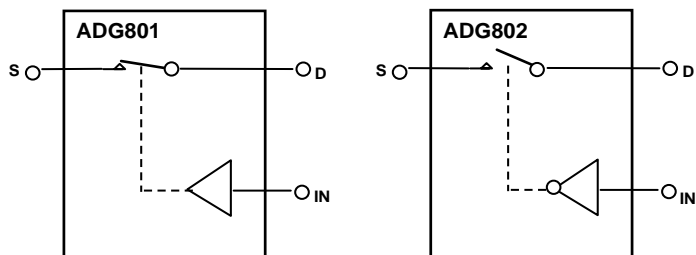
The ADG801/ADG802 are monolithic CMOS SPST (Single Pole, Single Throw) switches with On Resistance of less than 0.5 $\Omega$ . These switches are designed on an advanced submicron process that provides extremely low on resistance, high switching speed and low leakage currents.

The low On Resistance of <0.5 $\Omega$  means these parts are ideal for applications where low on resistance switching is critical.

The ADG801 is a normally open (NO) switch, while the ADG802 is normally closed (NC). Each switch conducts equally well in both directions when ON.

The ADG801 and ADG802 are available in 6-lead SOT-23 and 8 Lead  $\mu$ SOIC packages.

### FUNCTIONAL BLOCK DIAGRAMS



SWITCHES SHOWN FOR A LOGIC "1" INPUT

### PRODUCT HIGHLIGHTS

1. Low On Resistance (0.25  $\Omega$  typical).
2. +1.8V to +5.5V Single Supply Operation.
3. Tiny 6 Lead SOT23 and 8 Lead  $\mu$ SOIC Packages.
4. Pin Compatible with ADG701 (ADG801)  
Pin Compatible with ADG702 (ADG802).

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ADG801/ADG802–SPECIFICATIONS<sup>1</sup>(V<sub>DD</sub> = 5 V ±10%, V<sub>SS</sub> = GND = 0 V. All specifications –40°C to +125°C unless otherwise noted.)

Parameter	+25°C	–40°C to +85°C	–40°C to +125°C	Units	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to V <sub>DD</sub>	V	V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>S</sub> = –10 mA; Test Circuit 1 V <sub>S</sub> = 0 V to V <sub>DD</sub> , I <sub>S</sub> = –10 mA
On Resistance (R <sub>ON</sub> )	0.25			Ω typ	
	0.4	0.5	0.75	Ω max	
On-Resistance Flatness (R <sub>FLAT(ON)</sub> )	0.05	0.1	0.2	Ω typ Ω max	
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage I <sub>S</sub> (OFF)	±0.01			nA typ	V <sub>DD</sub> = +5.5 V V <sub>S</sub> = 4.5 V/1 V, V <sub>D</sub> = 1 V/4.5 V; Test Circuit 2
	±0.5	±1	tbd	nA max	
Drain OFF Leakage I <sub>D</sub> (OFF)	±0.01			nA typ	V <sub>S</sub> = 4.5 V/1 V, V <sub>D</sub> = 1 V/4.5 V; Test Circuit 2
	±0.5	±1	tbd	nA max	
Channel ON Leakage I <sub>D</sub> , I <sub>S</sub> (ON)	±0.01			nA typ	V <sub>S</sub> = V <sub>D</sub> = 1 V, or 4.5 V; Test Circuit 3
	±0.5	±1	tbd	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, V <sub>INH</sub>			2.4	V min	V <sub>IN</sub> = V <sub>INL</sub> or V <sub>INH</sub>
Input Low Voltage, V <sub>INL</sub>			0.8	V max	
Input Current I <sub>INL</sub> or I <sub>INH</sub>	0.005		±0.1	μA typ μA max	
C <sub>IN</sub> , Digital Input Capacitance	5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
t <sub>ON</sub>	30 TBD		TBD	ns typ ns max	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 35 pF V <sub>S</sub> = 3 V; Test Circuit 4
t <sub>OFF</sub>	20 TBD		TBD	ns typ ns max	
Charge Injection	±20			pC typ	V <sub>S</sub> = 0 V, R <sub>S</sub> = 0 Ω, C <sub>L</sub> = 1 nF, Test Circuit 5
Off Isolation	–65			dB typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, f = 1 MHz, Test Circuit 6
Bandwidth –3 dB	30			MHz typ	R <sub>L</sub> = 50 Ω, C <sub>L</sub> = 5 pF, Test Circuit 7
C <sub>S</sub> (OFF)	55			pF typ	f = 1 MHz
C <sub>D</sub> (OFF)	55			pF typ	f = 1 MHz
C <sub>D</sub> , C <sub>S</sub> (ON)	110			pF typ	f = 1 MHz
<b>POWER REQUIREMENTS</b>					
I <sub>DD</sub>	0.001		1.0	μA typ μA max	V <sub>DD</sub> = +5.5 V Digital Inputs = 0 V or 5.5 V

## NOTES

<sup>1</sup>Temperature ranges are as follows: Extended Temperature Range: –40°C to +125°C.<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# SPECIFICATIONS<sup>1</sup>

( $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ ,  $V_{SS} = \text{GND} = 0\text{ V}$ . All specifications  $-40^{\circ}\text{C to }+125^{\circ}\text{C}$  unless otherwise noted.)

Parameter	+25°C	-40°C to +85°C	-40°C to +125°C	Units	Test Conditions/Comments
<b>ANALOG SWITCH</b>					
Analog Signal Range			0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	0.3		1	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = -10\text{ mA}$ ; Test Circuit 1
	0.7	0.8		$\Omega$ max	
On-Resistance Flatness( $R_{FLAT(ON)}$ )	0.1		0.3	$\Omega$ typ	$V_S = 0\text{ V to }V_{DD}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>					
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$			nA typ	$V_{DD} = +3.3\text{ V}$ $V_S = 3\text{ V/1 V}$ , $V_D = 1\text{ V/3 V}$ ; Test Circuit 2
	$\pm 0.5$	$\pm 0.1$	tbd	nA max	
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$			nA typ	$V_S = 3\text{ V/1 V}$ , $V_D = 1\text{ V/3 V}$ ; Test Circuit 2
	$\pm 0.5$	$\pm 0.1$	tbd	nA max	
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$			nA typ	$V_S = V_D = 1\text{ V}$ , or $3\text{ V}$ ; Test Circuit 3
	$\pm 0.5$	$\pm 0.1$	tbd	nA max	
<b>DIGITAL INPUTS</b>					
Input High Voltage, $V_{INH}$			2.0	V min	
Input Low Voltage, $V_{INL}$			0.4	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005			$\mu\text{A}$ typ	$V_{IN} = V_{INL}$ or $V_{INH}$
			$\pm 0.1$	$\mu\text{A}$ max	
$C_{IN}$ , Digital Input Capacitance	5			pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>					
$t_{ON}$	50			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 1.5\text{ V}$ , Test Circuit 4
	TBD		TBD	ns max	
$t_{OFF}$	40			ns typ	$R_L = 50\ \Omega$ , $C_L = 35\text{ pF}$ ns max $V_S = 1.5\text{ V}$ , Test Circuit 4
	TBD		TBD		$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , Test Circuit 5
Charge Injection	$\pm 20$			pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , Test Circuit 5
Off Isolation	-65			dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , Test Circuit 6
Bandwidth -3 dB	30			MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 7
$C_S$ (OFF)	55			pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	55			pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	110			pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>					
$I_{DD}$	0.001			$\mu\text{A}$ typ	$V_{DD} = +3.3\text{ V}$ Digital Inputs = 0 V or 3.3 V
			1.0	$\mu\text{A}$ max	

## NOTES

<sup>1</sup>Temperature ranges are as follows: Extended Temperature Range:  $-40^{\circ}\text{C to }+125^{\circ}\text{C}$ .<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG801/ADG802

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to GND	-0.3 V to +7 V
Analog Inputs <sup>2</sup>	-0.3 V to V <sub>DD</sub> +0.3 V
	or 30 mA, Whichever Occurs First
Continuous Current, S or D	400 mA
Peak Current, S or D	800 mA
	(Pulsed at 1 ms, 10% Duty Cycle Max)
Operating Temperature Range	
Extended	-40°C to +125°C
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
μSOIC Package, Power Dissipation	315 mW
θ <sub>JA</sub> Thermal Impedance	206°C/W
θ <sub>JC</sub> Thermal Impedance	44°C/W
SOT-23 Package, Power Dissipation	282 mW
θ <sub>JA</sub> Thermal Impedance	229.6°C/W
θ <sub>JC</sub> Thermal Impedance	91.99°C/W
Lead Temperature, Soldering (10seconds)	300°C
IR Reflow, Peak Temperature	+220°C
ESD	2kV

## NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

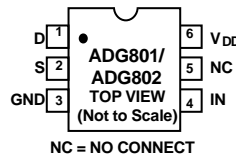
<sup>2</sup>Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. Truth Table

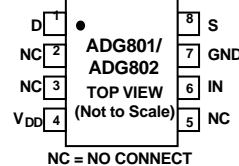
ADG801 In	ADG802 In	Switch Condition
0	1	OFF
1	0	ON

## PIN CONFIGURATIONS

### 6-Lead Plastic Surface Mount (SOT-23) (RT-6)



### 8-Lead Small Outline μSOIC (RM-8)



## ORDERING GUIDE

Model	Temperature Range	Supply Option <sup>1</sup>	Brand <sup>1</sup>	Package Descriptions	Package Options
ADG801BRT	-40°C to +125°C	3 V, 5 V	SLB	SOT-23 (Plastic Surface Mount)	RT-6
ADG801BRM	-40°C to +125°C	3 V, 5 V	SLB	μSOIC (Small Outline)	RM-8
ADG802BRT	-40°C to +125°C	3 V, 5 V	SMB	SOT-23 (Plastic Surface Mount)	RT-6
ADG802BRM	-40°C to +125°C	3 V, 5 V	SMB	μSOIC (Small Outline)	RM-8

<sup>1</sup>Branding on SOT-23 and μSOIC packages is limited to 3 characters due to space constraints.

## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG801/ADG802 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## TERMINOLOGY

$V_{DD}$	Most positive power supply potential.
$I_{DD}$	Positive supply current.
GND	Ground (0 V) reference.
S	Source terminal. May be an input or output.
D	Drain terminal. May be an input or output.
IN	Logic control input.
$V_D (V_S)$	Analog voltage on terminals D, S
$R_{ON}$	Ohmic resistance between D and S.
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on-resistance as measured over the specified analog signal range.
$I_S (OFF)$	Source leakage current with the switch "OFF."
$I_D (OFF)$	Drain leakage current with the switch "OFF."
$I_D, I_S (ON)$	Channel leakage current with the switch "ON."
$V_{INL}$	Maximum input voltage for logic "0".
$V_{INH}$	Minimum input voltage for logic "1".
$I_{INL} (I_{INH})$	Input current of the digital input.
$C_S (OFF)$	"OFF" switch source capacitance. Measured with reference to ground.
$C_D (OFF)$	"OFF" switch drain capacitance. Measured with reference to ground.
$C_D, C_S (ON)$	"ON" switch capacitance. Measured with reference to ground.
$C_{IN}$	Digital input capacitance.
$t_{ON}$	Delay between applying the digital control input and the output switching on. See Test Circuit 4.
$t_{OFF}$	Delay between applying the digital control input and the output switching off.
Charge Injection	A measure of the glitch impulse transferred from the digital input to the analog output during switching.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Crosstalk	A measure of unwanted signal which is coupled through from one channel to another as a result of parasitic capacitance.
Bandwidth	The frequency at which the output is attenuated by 3dBs.
On Response	The Frequency response of the "ON" switch.
Insertion Loss	The loss due to the ON resistance of the switch.

ADG801/ADG802

TYPICAL PERFORMANCE CHARACTERISTICS

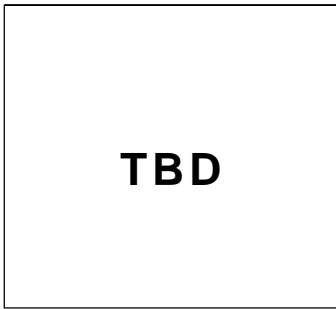


Figure 1. On Resistance as a Function of  $V_D(V_S)$

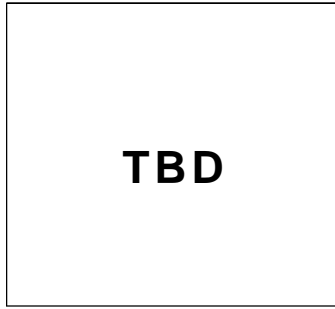


Figure 4. Leakage Currents as a function of  $V_D(V_S)$

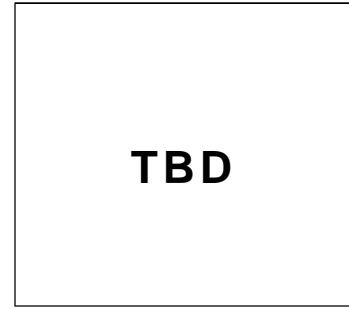


Figure 7. Leakage Currents as a Function of Temperature

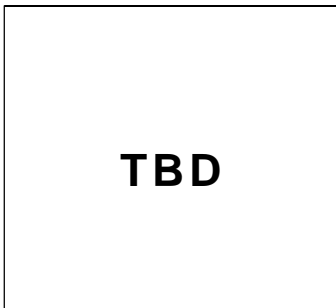


Figure 2. On Resistance as a Function of  $V_D(V_S)$  for Different Temperatures

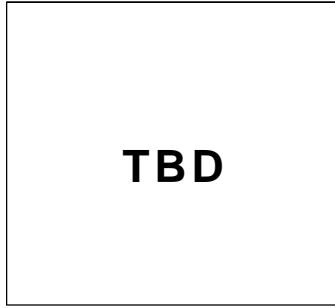


Figure 5. Leakage Currents as a function of  $V_D(V_S)$

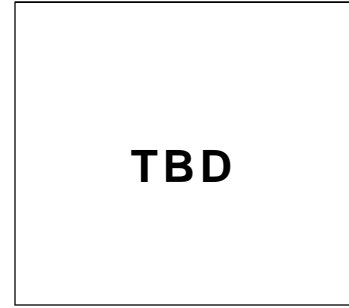


Figure 8. Supply Currents vs. Input Switching Frequency

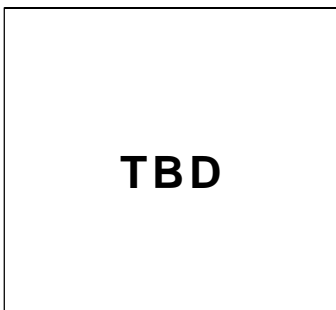


Figure 3. On Resistance as a Function of  $V_D(V_S)$  for Different Temperatures

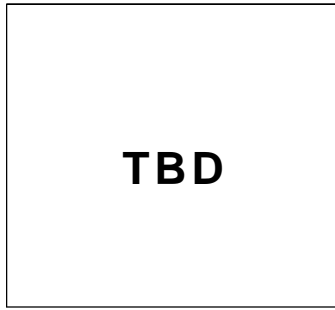


Figure 6. Leakage Currents as a function of Temperature

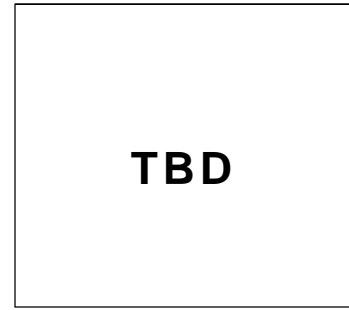


Figure 9. Charge Injection vs. Source Voltage

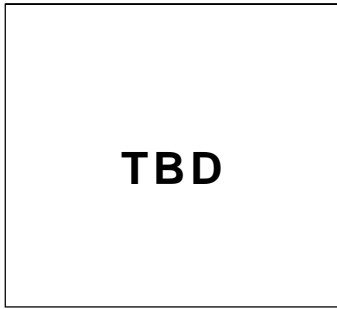


Figure 10.  $T_{ON}/T_{OFF}$  Times vs. Temperature

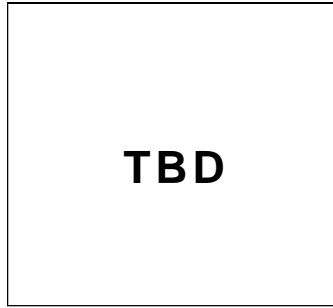


Figure 13. On Response vs. Frequency

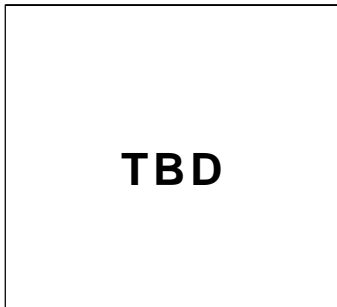


Figure 11. Off Isolation vs. Frequency

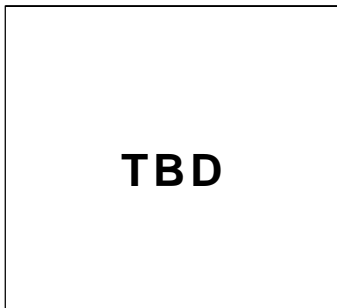
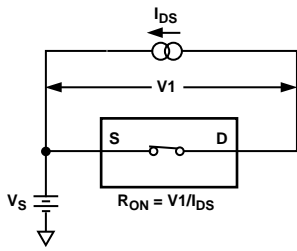


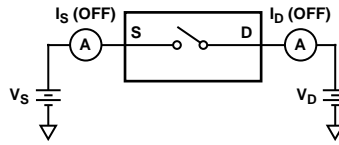
Figure 12. Crosstalk vs. Frequency

ADG801/ADG802

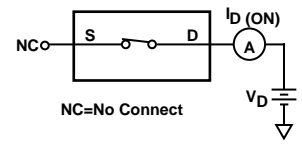
Test Circuits



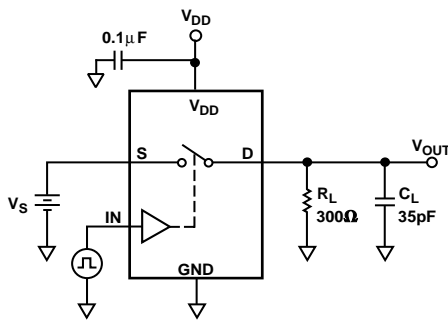
Test Circuit 1. On Resistance



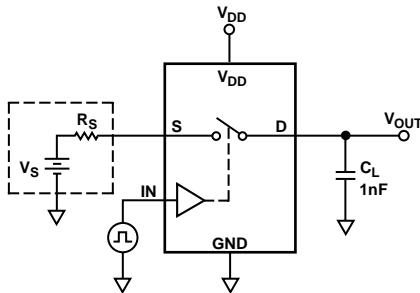
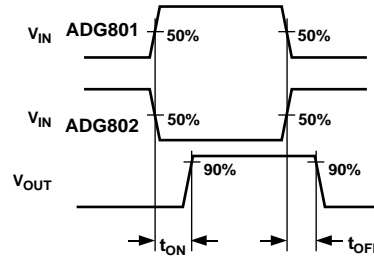
Test Circuit 2. Off Leakage



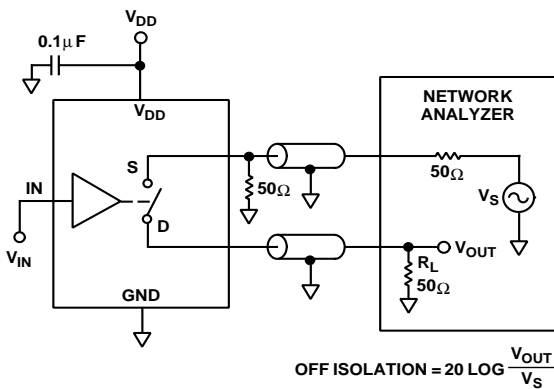
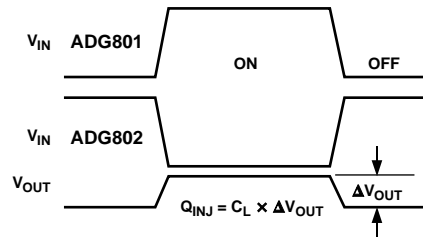
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times

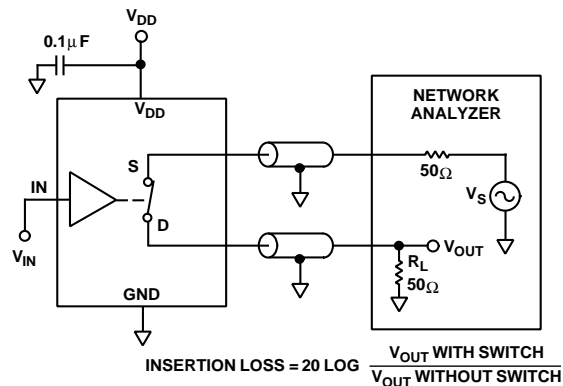


Test Circuit 5. Charge Injection



$$\text{OFF ISOLATION} = 20 \text{ LOG} \frac{V_{\text{OUT}}}{V_S}$$

Test Circuit 6. Off Isolation



$$\text{INSERTION LOSS} = 20 \text{ LOG} \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

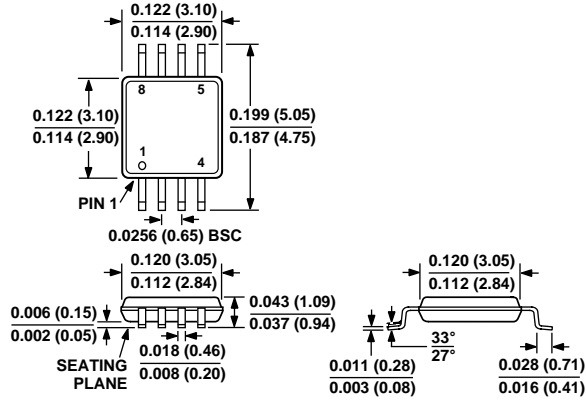
Test Circuit 7. Bandwidth



OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead  $\mu$ SOIC  
(RM-8)



6-Lead SOT-23  
(RT-6)

