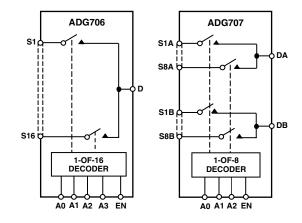


CMOS, 2.5 Ω Low-Voltage, 8-/16-Channel Multiplexers

ADG706/ADG707

FUNCTIONAL BLOCK DIAGRAMS



FEATURES

1.8 V to 5.5 V Single Supply ±3 V Dual Supply
2.5 Ω On Resistance
0.5 Ω On-Resistance Flatness
100 pA Leakage Currents
40 ns Switching Times
Single 16-to-1 Multiplexer ADG706
Differential 8-to-1 Multiplexer ADG707
28-Lead TSSOP Package
Low-Power Consumption
TTL/CMOS-Compatible Inputs

APPLICATIONS

Data Acquisition Systems Communication Systems Relay Replacement Audio and Video Switching Battery-Powered Systems

GENERAL DESCRIPTION

The ADG706 and ADG707 are low-voltage, CMOS analog multiplexers comprising 16 single channels and eight differential channels respectively. The ADG706 switches one of 16 inputs (S1–S16) to a common output, D, as determined by the 4-bit binary address lines A0, A1, A2, and A3. The ADG707 switches one of eight differential inputs to a common differential output as determined by the 3-bit binary address lines A0, A1, and A2. An EN input on both devices is used to enable or disable the device. When disabled, all channels are switched OFF.

Low-power consumption and operating supply range of 1.8 V to 5.5 V make the ADG706 and ADG707 ideal for battery-powered, portable instruments. All channels exhibit break-before-make switching action preventing momentary shorting when switching channels. These devices are also designed to operate from a dual supply of ± 3 V.

These multiplexers are designed on an enhanced submicron process that provides low-power dissipation yet gives highswitching speed, very low on resistance and leakage currents. On resistance is in the region of a few ohms and is closely matched between switches and very flat over the full signal range. These parts can operate equally well as either multiplexers or demultiplexers and have an input signal range which extends to the supplies.

The ADG706 and ADG707 are available in small 28-lead TSSOP packages.

PRODUCT HIGHLIGHTS

- 1. Single/Dual Supply Operation. The ADG706 and ADG707 are fully specified and guaranteed with 3 V and 5 V single supply and ± 3 V dual supply rails.
- 2. Low On Resistance (2.5 Ω typical).
- 3. Low-Power Consumption (<0.01 μ W).
- 4. Guaranteed Break-Before-Make Switching Action.
- 5. Small 28-Lead TSSOP Package.

REV.0

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One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A. Tel: 781/329-4700 World Wide Web Site: http://www.analog.com Fax: 781/326-8703 © Analog Devices, Inc., 2000

$\label{eq:additional} ADG706/ADG707 \\ -SPECIFICATIONS^1 \ (v_{DD} = 5 \ v \ \pm \ 10\%, \ v_{ss} = 0 \ v, \ \text{GND} = 0 \ v, \ \text{unless otherwise noted.})$

| | BV | Version | | |
|---|-----------|------------------------|---------------|--|
| Parameter | 25°C | -40°C to +85°C | Unit | Test Conditions/Comments |
| ANALOG SWITCH | 250 | | | |
| Analog Signal Range | | 0 V to V _{DD} | v | |
| On Resistance (R _{ON}) | 2.5 | | Ω typ | $V_{S} = 0 V$ to V_{DD} , $I_{DS} = 10 mA$; |
| on resistance (RON) | 4.5 | 5 | $\Omega \max$ | Test Circuit 1 |
| On Resistance Match Between | | 0.3 | Ωtyp | $V_{\rm S} = 0$ V to $V_{\rm DD}$, $I_{\rm DS} = 10$ mA |
| Channels (ΔR_{ON}) | | 0.8 | Ω max | |
| On-Resistance Flatness (R _{FLAT(ON)}) | 0.5 | | Ω typ | $V_{S} = 0 V$ to V_{DD} , $I_{DS} = 10 mA$ |
| | | 1.2 | Ω max | |
| LEAKAGE CURRENTS | | | | V _{DD} = 5.5 V |
| Source OFF Leakage I _S (OFF) | ±0.01 | | nA typ | $V_{\rm D} = 4.5 \text{ V/1 V}, V_{\rm S} = 1 \text{ V/4.5 V};$ |
| | ±0.1 | ±0.3 | nA max | Test Circuit 2 |
| Drain OFF Leakage I _D (OFF) | ±0.01 | | nA typ | $V_{\rm D} = 4.5 \text{ V}/1 \text{ V}, V_{\rm S} = 1 \text{ V}/4.5 \text{ V};$ |
| ADG706 | ± 0.4 | ± 1.5 | nA max | Test Circuit 3 |
| ADG707 | ±0.1 | ± 1 | nA max | |
| Channel ON Leakage I _D , I _S (ON) | ±0.01 | | nA typ | $V_{\rm D} = V_{\rm S} = 1$ V, or 4.5 V; |
| ADG706 | ±0.4 | ± 1.5 | nA max | Test Circuit 4 |
| ADG707 | ±0.1 | ± 1 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V _{INH} | | 2.4 | V min | |
| Input Low Voltage, V _{INL} | | 0.8 | V max | |
| Input Current | | | | |
| I _{INL} or I _{INH} | 0.005 | | μA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| | | ± 0.1 | μA max | |
| C _{IN} , Digital Input Capacitance | 5 | | pF typ | |
| DYNAMIC CHARACTERISTICS ² | | | | |
| t _{TRANSITION} | 40 | | ns typ | $R_L = 300 \Omega$, $C_L = 35 pF$, Test Circuit 5; |
| | | 60 | ns max | $V_{S1} = 3 V/0 V, V_{S16} = 0 V/3 V$ |
| Break-Before-Make Time Delay, t _D | 30 | | ns typ | $R_L = 300 \Omega$, $C_L = 35 pF$; |
| | | 1 | ns min | $V_S = 3 V$, Test Circuit 6 |
| t _{on} (EN) | 32 | | ns typ | $R_L = 300 \Omega, C_L = 35 pF;$ |
| | | 50 | ns max | $V_{\rm S}$ = 3 V, Test Circuit 7 |
| t _{OFF} (EN) | 10 | | ns typ | $R_L = 300 \Omega$, $C_L = 35 pF$; |
| | | 14 | ns max | $V_s = 3 V$, Test Circuit 7 |
| Charge Injection | ±5 | | pC typ | $V_{\rm S} = 1 \text{ V}, \text{ R}_{\rm S} = 0 \Omega, \text{ C}_{\rm L} = 1 \text{ nF};$ |
| | (0) | | | Test Circuit 8 P = 50 Q = 5 F $f = 10 MH$ |
| Off Isolation | -60 | | dB typ | $R_L = 50 \Omega, C_L = 5 pF, f = 10 MHz;$ |
| | -80 | | dB typ | R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; Test Circuit 9 |
| Channel-to-Channel Crosstalk | -60 | | dB typ | $R_{L} = 50 \Omega, C_{L} = 5 \text{ pF}, f = 10 \text{ MHz};$ |
| Chalmer-to-Chalmer Crosstalk | -80 | | dB typ | $R_L = 50 \Omega_2, C_L = 5 \text{ pF}, f = 1 \text{ MHz};$ $R_L = 50 \Omega, C_L = 5 \text{ pF}, f = 1 \text{ MHz};$ |
| | -00 | | ubtyp | Test Circuit 10 |
| -3 dB Bandwidth | | | | |
| ADG706 | 25 | | MHz typ | $R_L = 50 \Omega$, $C_L = 5 pF$, Test Circuit 9 |
| ADG707 | 36 | | MHz typ | $R_L = 50 \Omega$, $C_L = 5 pF$, Test Circuit 9 |
| C_{s} (OFF) | 13 | | pF typ | |
| $C_{\rm D}$ (OFF) | | | | |
| ADG706 | 180 | | pF typ | |
| ADG707 | 90 | | pF typ | |
| C_D, C_S (ON) | | | _ | |
| ADG706 | 200 | | pF typ | |
| ADG707 | 100 | | pF typ | |
| POWER REQUIREMENTS | | | | $V_{DD} = 5.5 V$ |
| - | 0.001 | | | |
| I _{DD} | 0.001 | | μA typ | Digital Inputs = 0 V or 5.5 V |

NOTES

¹Temperature range is as follows: B Version: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

$\label{eq:specifications} SPECIFICATIONS^{1} \; (v_{\text{DD}} = 3 \; v \; \pm \; 10\%, \; v_{\text{SS}} = 0 \; v, \; \text{GND} = 0 \; v, \; \text{unless otherwise noted})$

| $\begin{array}{ c c c c c c c c c c c c c c c c c c c$ | | BVe | ersion –40°C | | | |
|--|---|-----------|-------------------|---------------|--|--|
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | Parameter | 25°C | | Unit | Test Conditions/Comments | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | ANALOG SWITCH | | | | | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | | | $0 V$ to V_{DD} | v | | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | | 6 | o i to i DD | | $V_{s} = 0 V to V_{DD}$, $I_{Ds} = 10 mA$; | |
| On-Resistance Match Between Channels (ΔR_{ON}) 0.4 Ω typ $V_S = 0 V to V_{DD}, I_{DS} = 10 mA$ On-Resistance Flatness ($R_{FLAT(ON}$) 3 0 typ $V_S = 0 V to V_{DD}, I_{DS} = 10 mA$ Jenkerstance Flatness ($R_{FLAT(ON}$) 3 0 typ $V_S = 3 V to V_{DD}, I_{DS} = 10 mA$ Jenkerstance Flatness ($R_{FLAT(ON}$) ±0.01 nA typ $V_S = 3 V to V_{DD}, I_{DS} = 10 mA$ Drain OFF Leakage [I_D (OFF) ±0.01 nA max Test Circuit 2 Test Circuit 3 ADG706 ±0.4 ±1.5 nA max Test Circuit 4 Test Circuit 4 ADG706 ±0.4 ±1.5 nA max Test Circuit 4 Test Circuit 4 DIGTAL INPUTS 0.4 ±1.7 nA max Test Circuit 4 Test Circuit 4 Input Low Voltage, V_{NL} 0.04 W max V_N = V_NL or V_{NH} U_N = V_NL or V_{NH} Input Carent 0.005 µA max Pf typ Test Circuit 6 Input Carent 0.005 µA max V_N = 2 V/0 V, V_{NE} = 0 V/2 V Input Carent 0.005 µA max V_N = 2 V/0 V, V_N = 0 V/2 V <tr< td=""><td></td><td></td><td>12</td><td></td><td></td></tr<> | | | 12 | | | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | On-Resistance Match Between | | | | | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | | | | | $v_{S} = 0$ v to v_{DD} , $v_{DS} = 10$ mm | |
| LEAKAGE CURRENTS ± 0.01 ± 0.01 ± 0.01 πA typ N_{N} typ <t< td=""><td></td><td></td><td></td><td></td><td>V = 0 V to V = 1 = 10 mA</td></t<> | | | | | V = 0 V to V = 1 = 10 mA | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | | |) | <u>sz typ</u> | | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | | 10.01 | | A . | | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | Source OFF Leakage I _S (OFF) | | | | | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | | | ± 0.3 | | | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | | | | | | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | ADG706 | ± 0.4 | ± 1.5 | nA max | Test Circuit 3 | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | ADG707 | ±0.1 | ± 1 | nA max | | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | Channel ON Leakage I _D , I _S (ON) | ±0.01 | | nA typ | $V_{\rm S} = V_{\rm D} = 1 {\rm V} {\rm or} 3 {\rm V};$ | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | | | ±1.5 | | | |
| $ \begin{array}{ c c c c c c c c c c c c c c c c c c c$ | | | | | | |
| $ \begin{array}{ c c c c c c c c c c c c c c c c c c c$ | DIGITAL INPUTS | | | | | |
| $ \begin{array}{ c c c c c c c c c c c c c c c c c c c$ | | | 2.0 | V min | | |
| $ \begin{array}{ c c c c c c c c c c c c c c c c c c c$ | | | | | | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | | | V. 1 | , max | | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | - | 0.005 | | | $V_{rr} = V_{rr}$ or V_{rr} | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | I _{INL} of I _{INH} | 0.005 | ± 0.1 | | $\mathbf{v}_{\rm IN} - \mathbf{v}_{\rm INL}$ or $\mathbf{v}_{\rm INH}$ | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | C Disital Issue Consistence | _ | ± 0.1 | | | |
| $ \begin{array}{cccccccccccccccccccccccccccccccccccc$ | | 2 | | рг тур | | |
| Break-Before-Make Time Delay, t_D 75 ns max $V_{SI} = 2 V/0 V, V_{S16} = 0 V/2 V$ t_{ON} (EN) 30 ns typ ns typ $R_L = 300 \Omega, C_L = 35 pF;$ t_{OFF} (EN) 40 ns typ $R_L = 300 \Omega, C_L = 35 pF;$ t_{OFF} (EN) 20 ns max $V_S = 2 V,$ Test Circuit 7 $Charge Injection$ ± 5 PC typ $R_L = 300 \Omega, C_L = 35 pF;$ Off Isolation -60 dB typ $R_L = 300 \Omega, C_L = 35 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ -80 dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $-3 dB$ Bandwidth -60 dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $ADG706$ 25 MHz typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $ADG707$ 36 MHz typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $ADG707$ 36 MHz typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $ADG707$ 36 MHz typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $ADG707$ 36 MHz typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $ADG707$ 90 pF typ P | DYNAMIC CHARACTERISTICS ² | | | | | |
| Break-Before-Make Time Delay, t_D 30 ns typ ns typ $R_L = 300 \Omega, C_L = 35 pF;$ t_{ON} (EN) 40 ns typ $R_L = 300 \Omega, C_L = 35 pF;$ t_{OFF} (EN) 20 ns typ $R_L = 300 \Omega, C_L = 35 pF;$ t_{OFF} (EN) 20 ns typ $R_L = 300 \Omega, C_L = 35 pF;$ $Charge Injection$ ± 5 PC typ $R_L = 300 \Omega, C_L = 35 pF;$ Off Isolation -60 dB typ $R_L = 300 \Omega, C_L = 5 pF, f = 10 MH$ -80 dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ -80 dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$ Test Circuit 10 $R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$ Test Circuit 10 $R_L = 50 \Omega, C_L = 5 pF, Test Circuit R_L = 50 \Omega, C_L = 5 pF, Test Circuit R_L = 50 \Omega, C_L = 5 pF, Test Circuit R_L = 50 \Omega, C_L = 5 pF, Test Circuit R_L = 50 \Omega, C_L = 5 pF, Test Circuit R_L = 50 \Omega, C_L = 5 pF, Test Circuit R_L = 50 \Omega, C_L = 5 pF, Test $ | t _{TRANSITION} | 45 | | ns typ | $R_L = 300 \Omega$, $C_L = 35 pF$, Test Circuit 5 | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | | | 75 | ns max | | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | Break-Before-Make Time Delay, t _D | 30 | | ns typ | $R_{L} = 300 \Omega, C_{L} = 35 pF;$ | |
| $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$ | | | 1 | ns min | $V_{\rm S} = 2 \text{ V}$, Test Circuit 6 | |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$ | t _{ON} (EN) | 40 | | ns typ | $R_L = 300 \Omega, C_L = 35 pF;$ | |
| $\begin{array}{c ccccccccccccccccccccccccccccccccccc$ | | | 70 | | $V_{\rm S} = 2$ V, Test Circuit 7 | |
| Charge Injection28ns max pC typ $V_S = 2 V$, Test Circuit 7 $V_S = 1 V$, $R_S = 0 \Omega$, $C_L = 1 nF$; Test Circuit 8 $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 10 MH$ $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 0 MH$ $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 0 MH$ | t_{OFF} (EN) | 20 | | | | |
| Charge Injection ± 5 pC typ $V_S = 1 V, R_S = 0 \Omega, C_L = 1 nF;$ Test Circuit 8Off Isolation -60 dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$ Test Circuit 9Channel-to-Channel Crosstalk -60 dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 0 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 0 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 0 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 0 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 0 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 0 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 0 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 0 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 0 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 0 MH$ $R_L = 50 \Omega, C_L = 5 pF, Test CirculR_L = 50 \Omega, C_L = 5 pF, Test Circu$ | | | 28 | | | |
| Off Isolation-60 -80dB typ dB typTest Circuit 8 $R_L = 50 \Omega, C_L = 5 \text{ pF}, f = 10 \text{ MH}$ $R_L = 50 \Omega, C_L = 5 \text{ pF}, f = 1 \text{ MHz}$ Test Circuit 9Channel-to-Channel Crosstalk-60 -80dB typ dB typ $R_L = 50 \Omega, C_L = 5 \text{ pF}, f = 10 \text{ MH}$ $R_L = 50 \Omega, C_L = 5 \text{ pF}, f = 10 \text{ MH}$ $R_L = 50 \Omega, C_L = 5 \text{ pF}, f = 1 \text{ MHz}$ Test Circuit 10-3 dB Bandwidth ADG70625 36 C_B (OFF)MHz typ 13 PF typ $R_L = 50 \Omega, C_L = 5 \text{ pF}, \text{ Test Circuit}$ ADG706 ADG707180 PF typpF typADG706 ADG707200 100pF typPOWER REQUIREMENTSV_{DD} = 3.3 V | Charge Injection | ±5 | - | | | |
| Off Isolation-60dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ -80dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$ Channel-to-Channel Crosstalk-60dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ -3 dB Bandwidth-80dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MHz$ -3 dB Bandwidth-80MHz typ $R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$ -3 dB Bandwidth-80MHz typ $R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$ -3 dB Bandwidth-80MHz typ $R_L = 50 \Omega, C_L = 5 pF, Test CirculADG70625MHz typR_L = 50 \Omega, C_L = 5 pF, Test CirculADG70736MHz typR_L = 50 \Omega, C_L = 5 pF, Test CirculC_D (OFF)13pF typADG706180pF typADG706200pF typADG706200pF typADG707100pF typPOWER REQUIREMENTSV_DD = 3.3 V$ | | | | P - JP | | |
| $ \begin{array}{c c c c c c c c c c c c c c c c c c c $ | Off Isolation | -60 | | dB typ | | |
| Channel-to-Channel Crosstalk-60 -80dB typ dB typTest Circuit 9 $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$ Test Circuit 10-3 dB Bandwidth ADG706 ADG70725 36 C_S (OFF)MHz typ pF typ $R_L = 50 \Omega, C_L = 5 pF, Test CircuR_L = 50 \Omega, C_L = 5 pF, Test Ci$ | | | | | | |
| Channel-to-Channel Crosstalk-60 -80dB typ dB typ $R_L = 50 \Omega, C_L = 5 pF, f = 10 MH$ $R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$ Test Circuit 10-3 dB Bandwidth ADG70625 ADG707MHz typ ADG707 $R_L = 50 \Omega, C_L = 5 pF, f = 1 MHz$ Test Circuit 10-3 dB Bandwidth ADG70625 ADG707MHz typ PF typ $R_L = 50 \Omega, C_L = 5 pF, Test CircuitR_L = 50 \Omega, C_L = 5 pF, Test CircuitR_L = 50 \Omega, C_L = 5 pF, Test CircuitPF typ-3 dB BandwidthADG70713PF typPF typC_D (OFF)ADG70618090pF typPF typADG706ADG706200100pF typPOWER REQUIREMENTSVDD = 3.3 V$ | | | | | | |
| $\begin{array}{c c c c c c c c c c c c c c c c c c c $ | Channel_to_Channel Crosstall | _60 | | dB tre | | |
| -3 dB BandwidthTest Circuit 10ADG70625MHz typADG70736MHz typ C_s (OFF)13pF typ C_D (OFF)180pF typADG706180pF typADG70790pF typ C_D, C_s (ON)pF typADG706200pF typADG707100pF typPOWER REQUIREMENTSVDD = 3.3 V | Ghaimer-to-Ghaimer Grusstaik | | | | | |
| -3 dB Bandwidth ADG70625MHz typ MHz typ pF typ $R_L = 50 \Omega, C_L = 5 \text{ pF}, \text{ Test CircuR_L} = 50 \Omega$ | | -80 | | и сы сур | | |
| ADG70625MHz typ $R_L = 50 \Omega, C_L = 5 pF$, Test CircuADG70736MHz typ $R_L = 50 \Omega, C_L = 5 pF$, Test Circu C_S (OFF)13pF typ $R_L = 50 \Omega, C_L = 5 pF$, Test Circu $\Delta DG706$ 180pF typ $\Delta DG707$ 90pF typ C_D, C_S (ON) PF typ $\Delta DG706$ 200pF typ $\Delta DG707$ 100pF typPOWER REQUIREMENTS $V_{DD} = 3.3 V$ | -3 dB Bandwidth | | | | | |
| ADG70736MHz typ pF typ $R_L = 50 \Omega, C_L = 5 pF$, Test Circu $C_S (OFF)$ 13 $pF typ$ $PF typ$ $ADG706$ 180 $pF typ$ $ADG707$ 90 $pF typ$ $C_D, C_S (ON)$ $PF typ$ $ADG706$ 200 $pF typ$ $ADG707$ 100 $pF typ$ POWER REQUIREMENTS $V_{DD} = 3.3 V$ | | 25 | | MH7 two | $R_{r} = 50.0$ $C_{r} = 5$ nF. Test Circuit 0 | |
| $\begin{array}{c c} C_{\rm S} ({\rm OFF}) & 13 & p{\rm F} {\rm typ} \\ C_{\rm D} ({\rm OFF}) & 180 & p{\rm F} {\rm typ} \\ ADG706 & 180 & p{\rm F} {\rm typ} \\ ADG707 & 90 & p{\rm F} {\rm typ} \\ C_{\rm D}, C_{\rm S} ({\rm ON}) & & & \\ ADG706 & 200 & p{\rm F} {\rm typ} \\ ADG707 & 100 & p{\rm F} {\rm typ} \end{array}$ | | | | | | |
| CD (OFF) ADG706 180 pF typ ADG707 90 pF typ CD, Cs (ON) PF typ PF typ ADG706 200 pF typ ADG707 100 pF typ POWER REQUIREMENTS VDD = 3.3 V | | | | | $\kappa_L = 50.52, C_L = 5 \text{ pr}, \text{ 1est Circuit 9}$ | |
| ADG706 180 pF typ ADG707 90 pF typ C _D , C _S (ON) 200 pF typ ADG706 200 pF typ ADG707 100 pF typ POWER REQUIREMENTS V _{DD} = 3.3 V | | 15 | | рг тур | | |
| ADG707 90 pF typ C _D , C _S (ON) 200 pF typ ADG706 200 pF typ ADG707 100 pF typ POWER REQUIREMENTS V _{DD} = 3.3 V | _ , , | 100 | | | | |
| $\begin{array}{c c} C_{D}, C_{S} (ON) \\ ADG706 \\ ADG707 \\ \hline POWER REQUIREMENTS \\ \hline V_{DD} = 3.3 V \\ \hline \end{array}$ | | | | | | |
| ADG706 ADG707 200 100 pF typ pF typ POWER REQUIREMENTS V _{DD} = 3.3 V | | 90 | | pF typ | | |
| ADG707 100 pF typ POWER REQUIREMENTS V _{DD} = 3.3 V | | | | | | |
| POWER REQUIREMENTS $V_{DD} = 3.3 V$ | | 200 | | pF typ | | |
| | ADG707 | 100 | | pF typ | | |
| | POWER REQUIREMENTS | | | | $V_{DD} = 3.3 V$ | |
| I_{DD} 0.001 $\mu A tvp$ Digital Inputs = 0 V or 3 3 V | I _{DD} | 0.001 | | μA typ | Digital Inputs = $0 \text{ V or } 3.3 \text{ V}$ | |
| $1.0 \qquad \mu A max$ | עע־ | | 1.0 | | | |

NOTES

¹Temperature ranges are as follows: B Versions: -40°C to +85°C.

²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ADG706/ADG707 **Dual Supply**¹ (V_{DD} = +3 V ± 10%, V_{SS} = -3 V ± 10%, GND = 0 V, unless otherwise noted.)

| | B | Version | | |
|---|-------------------------|----------------------|----------------------------|---|
| _ | | -40°C | | |
| Parameter | 25°C | to +85°C | Unit | Test Conditions/Comments |
| ANALOG SWITCH | | | | |
| Analog Signal Range | | V_{SS} to V_{DD} | V | |
| On Resistance (R _{ON}) | 2.5 | | Ω typ | $V_{S} = V_{SS}$ to V_{DD} , $I_{DS} = 10$ mA; |
| | 4.5 | 5 | Ω max | Test Circuit 1 |
| On-Resistance Match Between | 1.5 | 0.3 | Ω typ | $V_{\rm S} = V_{\rm SS}$ to $V_{\rm DD}$, $I_{\rm DS} = 10$ mA |
| Channels (ΔR_{ON}) | | 0.8 | $\Omega \max$ | |
| | 0.5 | 0.0 | | $V_{\rm S} = V_{\rm SS}$ to $V_{\rm DD}$, $I_{\rm DS} = 10$ mA |
| On-Resistance Flatness (R _{FLAT(ON)}) | 0.5 | 1.0 | Ω typ | $v_{\rm S} - v_{\rm SS}$ to $v_{\rm DD}$, $r_{\rm DS} - 10$ mA |
| | | 1.2 | Ω max | |
| LEAKAGE CURRENTS | | | | $V_{DD} = +3.3 \text{ V}, V_{SS} = -3.3 \text{ V}$ |
| Source OFF Leakage I _S (OFF) | ±0.01 | | nA typ | $V_{\rm S} = +2.25 \text{ V/}-1.25 \text{ V}, V_{\rm D} = -1.25 \text{ V/}+2.25 \text{ V};$ |
| | ±0.1 | ±0.3 | nA max | Test Circuit 2 |
| Drain OFF Leakage I _D (OFF) | ±0.01 | | nA typ | $V_{\rm S}$ = +2.25 V/-1.25 V, $V_{\rm D}$ = -1.25 V/+2.25 V; |
| ADG706 | ± 0.4 | ±1.5 | nA max | Test Circuit 3 |
| ADG707 | ± 0.1 | ±1 | nA max | |
| Channel ON Leakage I_D , I_S (ON) | ± 0.01 | <u> </u> | nA typ | $V_{\rm S} = V_{\rm D} = +2.25 \text{ V/}-1.25 \text{ V}$, Test Circuit 4 |
| ADG706 | ± 0.01 ± 0.4 | ±1.5 | | $v_{\rm S} = v_{\rm D} = (2.23 \ v) = 1.23 \ v_{\rm s}$ rest Circuit 4 |
| | | | nA max | |
| ADG707 | ±0.1 | ± 1 | nA max | |
| DIGITAL INPUTS | | | | |
| Input High Voltage, V _{INH} | | 2.0 | V min | |
| Input Low Voltage, V _{INL} | | 0.4 | V max | |
| Input Current | | | | |
| I _{INL} or I _{INH} | 0.005 | | µA typ | $V_{IN} = V_{INL}$ or V_{INH} |
| INL OF INH | 0.005 | ± 0.1 | μA max | |
| C _{IN} , Digital Input Capacitance | 5 | ±0.1 | pF typ | |
| | | | prityp | |
| DYNAMIC CHARACTERISTICS ² | | | | |
| t _{TRANSITION} | 40 | | ns typ | $R_L = 300 \Omega$, $C_L = 35 pF$, Test Circuit 5 |
| | | 60 | ns max | $V_{S1} = 1.5 \text{ V/0 V}, V_{S16} = 0 \text{ V/1.5 V}$ |
| Break-Before-Make Time Delay, t _D | 15 | | ns typ | $R_{L} = 300 \Omega, C_{L} = 35 pF;$ |
| | | 1 | ns min | $V_{\rm S} = 1.5$ V, Test Circuit 6 |
| t _{on} (EN) | 32 | | ns typ | $R_{\rm L} = 300 \Omega, C_{\rm L} = 35 \mathrm{pF};$ |
| | | 50 | ns max | $V_s = 1.5 V$, Test Circuit 7 |
| t _{OFF} (EN) | 16 | | ns typ | $R_L = 300 \Omega, C_L = 35 pF;$ |
| -011 () | | 26 | ns max | $V_s = 1.5 V$, Test Circuit 7 |
| Charge Injection | ±8 | 20 | pC typ | $V_{\rm S} = 0$ V, $R_{\rm S} = 0$ Ω , $C_{\rm L} = 1$ nF; |
| Charge Injection | <u> </u> | | pergp | Test Circuit 8 |
| Off Isolation | -60 | | dD true | |
| Oli isolation | | | dB typ | $R_L = 50 \Omega, C_L = 5 pF, f = 10 MHz;$ |
| | -80 | | dB typ | $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; |
| | | | | Test Circuit 9 |
| Channel-to-Channel Crosstalk | -60 | | dB typ | $R_L = 50 \Omega, C_L = 5 pF, f = 10 MHz;$ |
| | -80 | | dB typ | $R_L = 50 \Omega$, $C_L = 5 pF$, $f = 1 MHz$; |
| | | | | Test Circuit 10 |
| –3 dB Bandwidth | | | | |
| ADG706 | 25 | | MHz typ | $R_L = 50 \Omega$, $C_L = 5 pF$, Test Circuit 9 |
| ADG707 | 36 | | MHz typ | $R_L = 50 \Omega$, $C_L = 5 pF$, Test Circuit 9 |
| C _s (OFF) | 13 | | pF typ | |
| $C_{\rm D}$ (OFF) | | | | |
| ADG706 | 180 | | pF typ | |
| ADG707 | 90 | | pF typ | |
| C_D, C_S (ON) | | | P- UP | |
| ADG706 | 200 | | nE turn | |
| | | | pF typ | |
| ADG707 | 100 | | pF typ | |
| DOWED DECLUDENTS | | | | |
| POWER REQUIREMENTS | | | 1 A . | |
| | 0.001 | | µA typ | $V_{DD} = +3.3 V$ |
| IDD | 0.001 | 1.0 | | |
| | 0.001 0.001 | 1.0 | μA typ μA max μA typ | $V_{DD} = +3.3 \text{ V}$ Digital Inputs = 0 V or 3.3 V $V_{SS} = -3.3 \text{ V}$ |

NOTES ¹Temperature range is as follows: B Version: -40° C to $+85^{\circ}$ C. ²Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS¹

| $(T_A = 25^{\circ}C \text{ unless otherwise noted})$ |
|---|
| V_{DD} to V_{SS} |
| V_{DD} to GND |
| V_{SS} to GND |
| Analog Inputs ² $V_{SS} - 0.3$ V to $V_{DD} + 0.3$ V or |
| 30 mA, Whichever Occurs First |
| Digital Inputs ² -0.3 V to V _{DD} + 0.3 V or |
| 30 mA, Whichever Occurs First |
| Peak Current, S or D 100 mA |
| (Pulsed at 1 ms, 10% Duty Cycle max) |
| Continuous Current, S or D 30 mA |
| Operating Temperature Range |
| Industrial (B Version) $\dots \dots -40^{\circ}$ C to $+85^{\circ}$ C |

| Storage Temperature Range65°C to +150°C |
|--|
| Junction Temperature 150°C |
| TSSOP Package |
| θ_{IA} Thermal Impedance |
| $\theta_{\rm JC}$ Thermal Impedance |
| Lead Temperature, Soldering (10 seconds) 300°C |
| IR Reflow, Peak Temperature 220°C |
| NOTES |

¹Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only, functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating condi-

tions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

²Overvoltages at IN, S or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

CAUTION_

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG706/ADG707 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

| Model | Temperature Range | Package Description | Package Option |
|-----------|-------------------|---|----------------|
| ADG706BRU | -40°C to +85°C | Thin Shrink Small Outline Package (TSSOP) | RU-28 |
| ADG707BRU | -40°C to +85°C | Thin Shrink Small Outline Package (TSSOP) | RU-28 |

PIN CONFIGURATIONS

28-Lead TSSOP

| V _{DD} 1 NC 3 S16 5 S15 6 S13 7 S12 9 S10 11 S10 11 S10 11 S10 11 S10 11 S11 11 S10 11 S11 11 | • ADG706 TOP VIEW (Not to Scale) | 28 27 26 25 24 23 22 21 20 19 18 17 16 15 | D V _{SS} S8 S7 S6 S5 S4 S3 S2 S1 EN A0 A1 A2 | | | |
|---|---|---|--|--|--|--|
| NC = NO CONNECT | | | | | | |

| V _{DD} 1 | • | 28 | DA | | |
|-------------------|----------------|----|------------|--|--|
| DB 2 | 1 | 27 | v_{ss} | | |
| NC 3 |] | 26 | S8A | | |
| S8B 4 | 1 | 25 | S7A | | |
| S7B 5 | 1 | 24 | S6A | | |
| S6B 6 | 400707 | 23 | S5A | | |
| S5B 7 | ADG707 | 22 | S4A | | |
| S4B 8 | (Not to Scale) | 21 | S3A | | |
| S3B 9 | | 20 | S2A | | |
| S2B 10 | 1 | 19 | S1A | | |
| S1B 11 | 1 | 18 | EN | | |
| GND 12 | | 17 | A0 | | |
| NC 13 | 1 | 16 | A 1 | | |
| NC 14 | 1 | 15 | A2 | | |
| N | | СТ | | | |
| | | | | | |

Table I. ADG706 Truth Table

| A3 | A2 | A1 | A0 | EN | ON Switch |
|----|----|----|----|----|-----------|
| X | X | X | X | 0 | NONE |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 2 |
| 0 | 0 | 1 | 0 | 1 | 3 |
| 0 | 0 | 1 | 1 | 1 | 4 |
| 0 | 1 | 0 | 0 | 1 | 5 |
| 0 | 1 | 0 | 1 | 1 | 6 |
| 0 | 1 | 1 | 0 | 1 | 7 |
| 0 | 1 | 1 | 1 | 1 | 8 |
| 1 | 0 | 0 | 0 | 1 | 9 |
| 1 | 0 | 0 | 1 | 1 | 10 |
| 1 | 0 | 1 | 0 | 1 | 11 |
| 1 | 0 | 1 | 1 | 1 | 12 |
| 1 | 1 | 0 | 0 | 1 | 13 |
| 1 | 1 | 0 | 1 | 1 | 14 |
| 1 | 1 | 1 | 0 | 1 | 15 |
| 1 | 1 | 1 | 1 | 1 | 16 |
| | 1 | 1 | 1 | 1 | 1 |

Table II. ADG707 Truth Table

| A2 | A1 | A0 | EN | ON Switch Pair |
|----|----|----|----|----------------|
| X | X | X | 0 | NONE |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 | 2 |
| 0 | 1 | 0 | 1 | 3 |
| 0 | 1 | 1 | 1 | 4 |
| 1 | 0 | 0 | 1 | 5 |
| 1 | 0 | 1 | 1 | 6 |
| 1 | 1 | 0 | 1 | 7 |
| 1 | 1 | 1 | 1 | 8 |

X = Don't Care.

X = Don't Care.

TERMINOLOGY

| V _{DD} | Most Positive Power Supply Potential. | C _D (OFF) | "OFF" Switch Drain Capacitance. Measured |
|----------------------|--|-------------------------|---|
| V _{SS} | Most Negative Power Supply in a Dual Sup- ply Application. In single supply applications, this should be tied to ground at the device. | $C_D, C_S(ON)$ | with reference to ground. "ON" Switch Capacitance. Measured with reference to ground. |
| I _{DD} | Positive Supply Current. | C _{IN} | Digital Input Capacitance. |
| I _{SS} | Negative Supply Current. | t _{TRANSITION} | Delay Time Measured Between the 50% and |
| GND | Ground (0 V) Reference. | | 90% Points of the Digital Inputs and the Switch |
| S | Source Terminal. May be an input or output. | | "ON" Condition when Switching from One Address State to Another. |
| D | Drain Terminal. May be an input or output. | t _{ON} (EN) | Delay Time Between the 50% and 90% Points |
| IN | Logic Control Input. | $t_{\rm ON}$ (EIV) | of the EN Digital Input and the Switch "ON" |
| $V_D (V_S)$ | Analog Voltage on Terminals D, S. | | Condition. |
| R _{ON} | Ohmic Resistance Between D and S. | t _{OFF} (EN) | Delay Time Between the 50% and 90% Points |
| $\Delta R_{\rm ON}$ | On Resistance Match Between any Two Chan- nels, i.e., R _{ON} max – R _{ON} min. | | of the EN Digital Input and the Switch "OFF" Condition. |
| $R_{FLAT(ON)}$ | Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog | t _{OPEN} | "OFF" Time Measured Between the 80% Points of Both Switches when Switching from One Address State to Another. |
| | signal range. | Charge | A Measure of the Glitch Impulse Transferred |
| I _S (OFF) | Source Leakage Current with the Switch "OFF." | Injection | from the Digital Input to the Analog Output During Switching. |
| I _D (OFF) | Drain Leakage Current with the Switch "OFF." | Off Isolation | A Measure of Unwanted Signal Coupling through an "OFF" Switch. |
| I_D , I_S (ON) | Channel Leakage Current with the Switch "ON." | Crosstalk | A Measure of Unwanted Signal which is Coupled through from One Channel to |
| V _{INL} | Maximum Input Voltage for Logic "0." | | Another as a Result of Parasitic Capacitance. |
| V _{INH} | Minimum Input Voltage for Logic "1." | Bandwidth | The Frequency at which the Output Is |
| $I_{INL}(I_{INH})$ | Input Current of the Digital Input. | | Attenuated by 3 dBs. |
| C _S (OFF) | "OFF" Switch Source Capacitance. Measured | On Response | The Frequency Response of the "ON" Switch. |
| | with reference to ground. | Insertion Loss | The Loss Due to the ON Resistance of the Switch. |

Typical Performance Characteristics-ADG706/ADG707

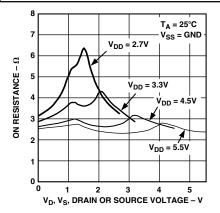


Figure 1. On Resistance as a Function of V_D (V_S) for Single Supply

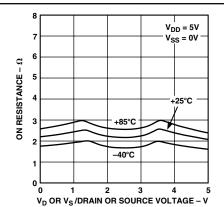


Figure 2. On Resistance as a Function of V_D (V_S) for Different Temperatures, Dual Supply

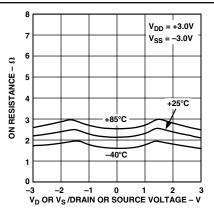


Figure 3. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

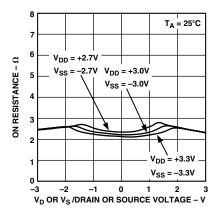


Figure 4. On Resistance as a Function of V_D (V_S) for Dual Supply

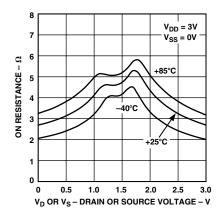


Figure 5. On Resistance as a Function of V_D (V_S) for Different Temperatures, Single Supply

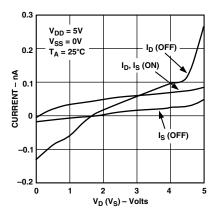


Figure 6. Leakage Currents as a Function of V_D (V_S)

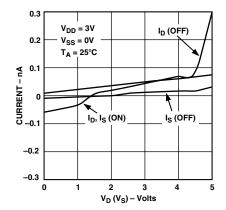


Figure 7. Leakage Currents as a Function of V_D (V_S)

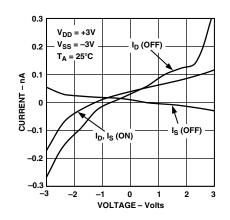


Figure 8. Leakage Currents as a Function of V_D (V_S)

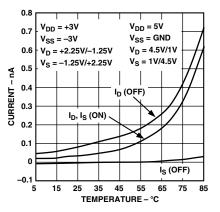


Figure 9. Leakage Currents as a Function of Temperature

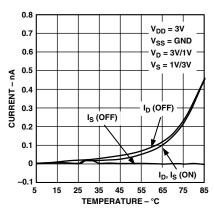


Figure 10. Leakage Currents as a Function of Temperature

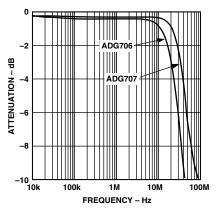


Figure 11. On Response vs. Frequency

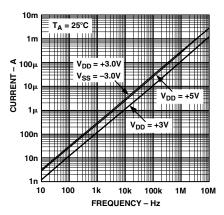


Figure 12. Supply Currents vs. Input Switching Frequency

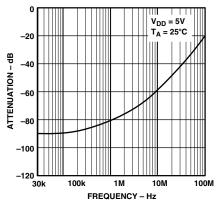


Figure 13. Off Isolation vs. Frequency

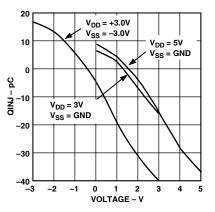


Figure 14. Charge Injection vs. Source Voltage

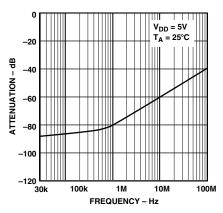
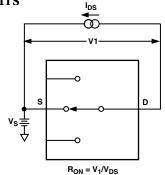
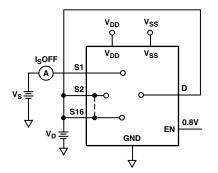


Figure 15. Crosstalk vs. Frequency

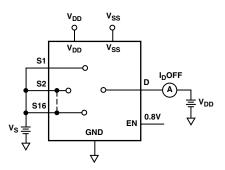
TEST CIRCUITS



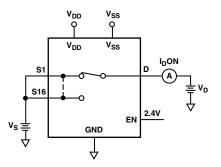
Test Circuit 1. On Resistance



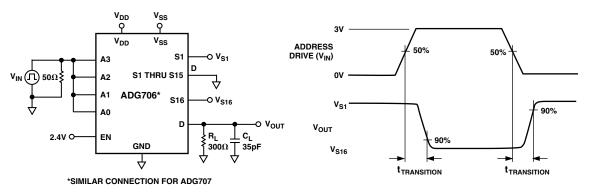
Test Circuit 2. I_S (OFF)



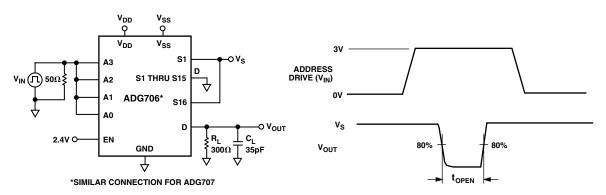
Test Circuit 3. I_D (OFF)



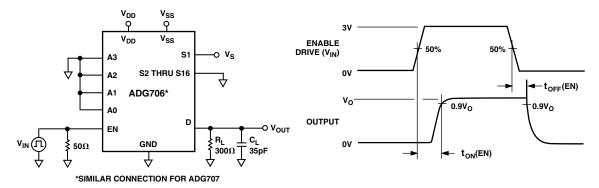
Test Circuit 4. I_D (ON)



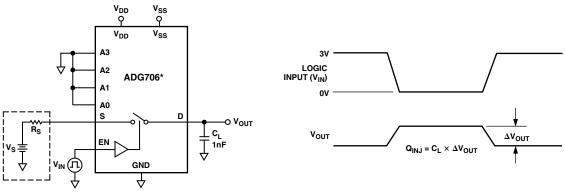
Test Circuit 5. Switching Time of Multiplexer, t_{TRANSITION}



Test Circuit 6. Break-Before-Make Delay, t_{OPEN}

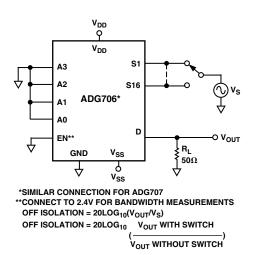


Test Circuit 7. Enable Delay, t_{ON} (EN), t_{OFF} (EN)

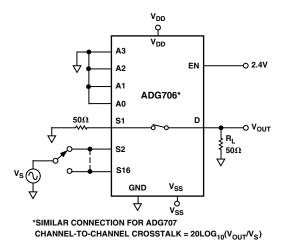


*SIMILAR CONNECTION FOR ADG707

Test Circuit 8. Charge Injection









OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

28-Lead TSSOP

