ANALOG DEVICES

High-Performance Driver/Comparator Active Load on a Single Chip

AD53509

FEATURES
250 MHz Operation
Driver/Comparator and Active Load Included
On-Chip Schottky Diode Bridge
52-Lead LQFP Package with Built-In Heat Sink

APPLICATIONS
Automatic Test Equipment
Semiconductor Test Systems
Board Test Systems
Instrumentation and Characterization Equipment

FUNCTIONAL BLOCK DIAGRAM

NC = NO CONNECT

PRODUCT DESCRIPTION
The AD53509 is a single chip that performs the pin electronics functions of driver, comparator and active load in ATE VLSI and memory testers. In addition, a Schottky diode bridge for the active load and a VCOM buffer are included internally.

The driver is a proprietary design that features three active states: Data High Mode, Data Low Mode and Term Mode as well as an Inhibit State. This facilitates the implementation of high speed active termination. The output voltage range is –2 V to +7 V to accommodate a wide variety of test devices. The output leakage is typically less than 250 nA over the entire signal range.

The dual comparator, with an input range equal to the driver output range, features built-in latches and ECL-compatible outputs. The outputs are capable of driving 50 Ω signal lines terminated to –2 V. Signal tracking capability is upwards of 5 V/ns.
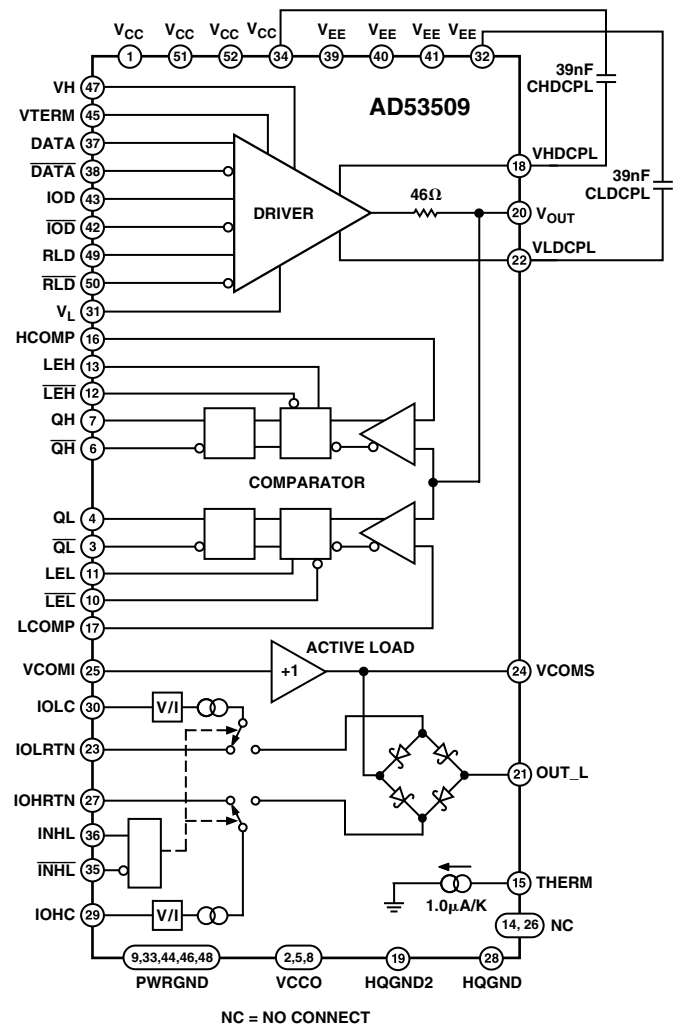
The active load can be set for up to 40 mA load current with less than a 10 μA linearity error through the entire set range. I_{OH}, I_{OL} and the buffered VCOM are independently adjustable. On-board Schottky diodes provide high speed switching and low capacitance.

Also included on the chip is an on-board temperature sensor whose purpose is to give an indication of the surface temperature of the DCL. This information can be used to measure θ_{JC} and θ_{JA} or flag an alarm if proper cooling is lost. Output from the sensor is a current sink that is proportional to absolute temperature. The gain is trimmed to a nominal value of 1.0 μA/K. As an example, the output current can be sensed by using a 10 kΩ resistor connected from 10 V to the THERM (IOUT) pin. A voltage drop across the resistor will be developed that equals:
$10K \times 1$ μA/K = 10 mV/K = 2.98 V at room temperature.

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DRIVER SPECIFICATIONS

(All specifications are at T_J = 85°C ± 5°C, V_S = 11 V ± 3%, $-V_S$ = –6 V = ±3% unless otherwise noted. All temperature coefficients are measured at T_J = 75°C to 95°C.)

Parameter	Min	Typ	Max	Unit	Test Conditions
DIFFERENTIAL INPUT CHARACTERISTICS					
(DATA to $\overline{DATA}$, IOD to $\overline{IOD}$, RLD to $\overline{RLD}$)					
Input Voltage	–2		+3	V	
Differential Input Range			2	V	All Digital Inputs Within a 2 V Range
Bias Current	–250		+250	µA	V_{IN} = –2 V, +3 V
REFERENCE INPUTS					
Bias Currents	–50		+50	µA	V_L, V_H, V_T = 5 V
OUTPUT CHARACTERISTICS					
Logic High Range	–2		+7	V	DATA = H, V_H = –2 V to +7 V, V_L = –2 V, V_T = 0 V
Logic Low Range	–2		+6	V	DATA = L, V_L = –2 V to +6 V, V_H = 7 V, V_T = 0 V
Amplitude (V_H and V_L)	0.1		9	V	V_L = 0.0 V, V_H = 0.1 V, V_T = 0 V
Absolute Accuracy					V_L = –2 V, V_H = +7 V, V_T = 0 V
V_H Offset	–50		+50	mV	DATA = H, V_H = 0 V, V_L = –2 V, V_T = –1 V
V_H Gain + Linearity Error	0.3 – 5		+0.3 + 5	% of V_H + mV	DATA = H, V_H = –1 V to +7 V, V_L = –2 V, V_T = –2 V
V_L Offset	–50		+50	mV	DATA = L, V_L = 0 V, V_H = 5 V, V_T = 3 V
V_L Gain + Linearity Error	–0.3 – 5		+0.3 + 5	% of V_L + mV	DATA = L, V_L = –2 V to +6 V, V_H = 7 V, V_T = 7 V
Offset TC		0.5		mV/°C	V_L = –2 V, V_H = 0 V, V_T = –1 V (V_H Offset)
					V_L = 0 V, V_H = 5 V, V_T = 3 V (V_L Offset)
Output Resistance					
V_H = –2 V	44	46	48	Ω	V_L = –2 V, V_T = 0 V, I_{OUT} = 0, +1, +30 mA
V_H = +7 V	44	46	48	Ω	V_L = –1 V, V_T = 0 V, I_{OUT} = 0, –1, –30 mA
V_L = –2 V	44	46	48	Ω	V_H = 6 V, V_T = 0 V, I_{OUT} = 0, 1, 30 mA
V_L = +6 V	44	46	48	Ω	V_H = 7 V, V_T = 0 V, I_{OUT} = 0, –1, –30 mA
V_H = +3 V		46		Ω	V_L = 0 V, V_T = 0 V, I_{OUT} = –30 mA (Trim Point)
Dynamic Current Limit		>100		mA	C_{BYP} = 39 nF, V_H = 6 V, V_L = –2 V, V_T = 0 V
Static Current Limit	–85		+85	mA	Output to –2 V, V_H = 7 V, V_L = –1 V, V_T = 0 V
					DATA = H and Output to 7 V, V_H = 6 V,
					V_L = –2 V, V_T = 0 V, DATA = L
V_{TERM}					
Voltage Range	–2		+7	V	TERM MODE, V_T = –2 V to +7 V, V_L = 0 V, V_H = 3 V
V_{TERM} Offset	–50		+50	mV	TERM MODE, V_T = 0 V, V_L = 0 V, V_H = 3 V
V_{TERM} Gain + Linearity Error	–0.3 +10		+0.3 +10	% of V_{SET} + mV	TERM MODE, V_T = –2 V to +7 V, V_L = 0 V, V_H = 3 V
Offset TC		0.5		mV/°C	V_T = 0 V, V_L = 0 V, V_H = 3 V
Output Resistance	44	46	49	Ω	I_{OUT} = +30 mA, +1.0 mA, V_T = –2.0 V, V_H = 3 V, V_L = 0 V
					I_{OUT} = –30 mA, –1.0 mA, V_T = +7.0 V, V_H = 3 V, V_L = 0 V
					I_{OUT} = ±30 mA, ±1.0 mA, V_T = 0 V, V_H = 3 V, V_L = 0 V
DYNAMIC PERFORMANCE, (V_H AND V_L)					
Propagation Delay Time		1.5		ns	Measured at 50%, V_H = +400 mV, V_L = –400 mV, V_T = 0 V
Propagation Delay TC		2		ps/°C	Measured at 50%, V_H = +400 mV, V_L = –400 mV, V_T = 0 V
Delay Matching, Edge to Edge		<100		ps	Measured at 50%, V_H = +400 mV, V_L = –400 mV, V_T = 0 V
Rise and Fall Times					
1 V Swing		0.42		ns	Measured 20%–80%, V_L = 0 V, V_H = 1 V, V_T = 0 V
3 V Swing		0.75		ns	Measured 20%–80%, V_L = 0 V, V_H = 3 V, V_T = 0 V
5 V Swing		1.65		ns	Measured 10%–90%, V_L = 0 V, V_H = 5 V, V_T = 0 V
9 V Swing		3.0		ns	Measured 10%–90%, V_L = –2 V, V_H = 7 V, V_T = 0 V
Rise and Fall Time Temperature Coefficient					
1 V Swing		±1		ps/°C	Measured 20%–80%, V_L = 0 V, V_H = 1 V
3 V Swing		±2		ps/°C	Measured 20%–80%, V_L = 0 V, V_H = 3 V
5 V Swing		±4		ps/°C	Measured 10%–90%, V_L = 0 V, V_H = 5 V
Overshoot and Preshoot		<3 + 50		% of Step + mV	V_L, V_H = –0.1 V, 0.1 V, V_L, V_H = 0.0 V, 1.0 V
					V_L, V_H = 0.0 V, 3.0 V, V_L, V_H = 0.0 V, 5.0 V
					V_L, V_H = –2.0 V, 7.0 V
Settling Time					
to 15 mV		<50		ns	V_L = 0 V, V_H = 0.5 V, V_T = –2 V
to 4 mV		<10		µs	V_L = 0 V, V_H = 0.5 V, V_T = –2 V

Parameter	Min	Typ	Max	Unit	Test Conditions
Delay Change vs. Pulsewidth		50		ps	V_L = 0 V, V_H = 2 V, Pulsewidth = 2.5 ns/7.5 ns, 30 ns/90 ns
Minimum Pulsewidth					
3 V Swing		1.4		ns	V_L = 0 V, V_H = 3 V, 90% (2.7 V) Reached, Measure @ 50%
5 V Swing		2.0		ns	V_L = 0 V, V_H = 5 V, 90% (4.5 V) Reached, Measure @ 50%
Toggle Rate		250		MHz	V_L = 0 V, V_H = 5 V, VDUT > 3.0 V p-p
DYNAMIC PERFORMANCE, INHIBIT					
Delay Time, Active to Inhibit		3.3		ns	Measured at 50%, V_H = +2 V, V_L = –2 V, V_T = 0 V
Delay Time, Inhibit to Active		2.9		ns	Measured at 50%, V_H = +2 V, V_L = –2 V, V_T = 0 V
Delay Time Matching (Z)		<2		ns	Z = Delay Time Active to Inhibit Test (Above)—
					Delay Time Inhibit to Active Test (Above)
					(Of Worst Two Edges)
I/O Spike		150		mV, p-p	V_H = 0 V, V_L = 0 V, V_T = 0 V
Rise, Fall Time, Active to Inhibit		1.6		ns	V_H = +2 V, V_L = –2 V (Measured 20%/80% of 1 V Output)
Rise, Fall Time, Inhibit to Active		1.4		ns	V_H = +2 V, V_L = –2 V (Measured 20%/80% of 1 V Output)
DYNAMIC PERFORMANCE , V_{TERM}					
Delay Time, V_H to V_{TERM}, V_L to V_{TERM}		2.5		ns	Measured at 50%, V_L = –1 V, V_H = +1 V, V_{TERM} = 0 V
Delay Time, V_{TERM} to V_H and V_{TERM} to V_L		2.5		ns	Measured at 50%, V_L = V_H = +0.4 V, V_{TERM} = –0.4 V
Overshoot and Preshoot		<3.0 + 75		% of Step + mV	V_H/V_L, V_{TERM} = (0 V, –1 V), (0 V, –2.0 V),
					(0 V, 6.0 V)
V_{TERM} Mode Rise Time		2.2		ns	V_L = –2 V, V_H = +2 V, V_{TERM} = 0 V, 20%–80%
V_{TERM} Mode Fall Time		2.2		ns	V_L = –2 V, V_H = +2 V, V_{TERM} = 0 V, 20%–80%
PSRR, DRIVE or TERM Mode		35		dB	V_S = V_S ± 3%

Specifications subject to change without notice.

COMPARATOR SPECIFICATIONS

(All specifications are at T_J = 85°C ± 5°C. [Outputs terminated in 150 Ω to GND, +V_S = 11 V ± 3% –V_S = 6 V ± 3%, VCCO = 3.3 V unless otherwise specified.] All temperatures coefficients are measured at T_J = 75°C to 95°C.)

Parameter	Min	Typ	Max	Unit	Test Conditions
DC INPUT CHARACTERISTICS					
Offset Voltage (V_{OS})	–25		+25	mV	CMV = 0 V
Offset Voltage (Drift)		50		μV/°C	CMV = 0 V
HCOMP, LCOMP Bias Current	–50		+50	μA	V_{IN} = 0 V
Voltage Range (V_{CM})	–2		+7.0	V	
Differential Voltage (V_{DIFF})			9.0	V	
Gain and Linearity	–0.05		+0.05	% FSR	V_{IN} = –2 V to +7 V (9 V FSR)
LATCH ENABLE INPUTS					
Logic "1" Current (I_{IH})			250	μA	LEA, $\overline{LEA}$, LEB, $\overline{LEB}$ = +3 V
Logic "0" Current (I_{IL})	–250			μA	LEA, $\overline{LEA}$, LEB, $\overline{LEB}$ = –2 V
Logic Input Range	–2		+3	V	
DIGITAL OUTPUTS					
Logic "1" Voltage (V_{OH})	VCCO – 0.98			V	Q or $\overline{Q}$, 16.7 mA Load
Logic "0" Voltage (V_{OL})			VCCO – 1.5	V	Q or $\overline{Q}$, 10 mA Load
Slew Rate		1		V/ns	
VCCO Range	0		8	V	
SWITCHING PERFORMANCE					
Propagation Delay					
Input to Output		1.8		ns	V_{IN} = 2 V p-p,
Latch Enable to Output		2		ns	HCOMP = 1 V, LCOMP = 1 V
Propagation Delay Temperature Coefficient		2		ps/°C	
Propagation Delay Change with Respect to					
Slew Rate: 0.5 V, 1.0 V, 3.0 V/ns		<±100		ps	V_{IN} = 0 V to 5 V
Slew Rate: 5.0 V/ns		<±350		ps	V_{IN} = 0 V to 5 V
Amplitude: 1.0 V, 3.0 V, 5.0 V		<±200		ps	V_{IN} = 1.0 V/ns
Equivalent Input Rise Time		450		ps	V_{IN} = 0 V to 3 V, 3 V/ns
Pulsewidth Linearity		<±200		ps	V_{IN} = 0 V to 3 V, 3 V/ns, PW = 3 ns–8 ns
Settling Time		25		ns	Settling to ±8 mV, V_{IN} = 1 V to 0 V
Latch Timing					
Input Pulsewidth		1.68		ns	
Setup Time		1.0		ns	
Hold Time		1.1		ns	
Hysteresis		6		mV	Latch Inputs Programmed for Hysteresis

Specifications subject to change without notice.

AD53509–SPECIFICATIONS

ACTIVE LOAD SPECIFICATIONS

(All specifications are at T_J = 85°C ± 5°C, $+V_S$ = 11 V ± 3%, $-V_S$ = –6 V = ±3% unless otherwise noted. All temperature coefficients are measured at T_J = 75°C to 95°C.)

Parameter	Min	Typ	Max	Unit	Test Conditions
INPUT CHARACTERISTICS					
INHL, $\overline{\text{INHL}}$					
Input Voltage	–2		+3	V	IOHC = 1 V, IOLC = 1 V, VCOM = 2 V, OUT_L = 0 V
Bias Current	–250		250	µA	INHL, $\overline{\text{INHL}}$ = –2 V, +3 V
IOHC Current Program Range					
IOH = 0 mA to –40 mA	0		4	V	OUT_L = –0.7 V, +7 V
IOLC Current Program Range					
IOL = 0 mA to +40 mA	0		4	V	OUT_L = –2 V, +5.7 V
IOHC, IOLC Input Bias Current	–300		+300	µA	IOLC = 0 V, 4.0 V and IOHC = 0 V, 4.0 V
IOLRTN, IOHRTN Range	–2		+7	V	IOL = +40 mA, IOH = –40 mA, OUT_L = –2 V, +7 V
VDUT Range	–2		+7	V	IOL = +40 mA, IOH = –40 mA, IOUT_L–VCOMI >1.3 V
VDUT Range, IOH = 0 mA to –40 mA	–0.7		+7	V	OUT_L –VCOM > 1.3 V
VDUT Range, IOL = 0 mA to +40 mA	–2		+5.7	V	VCOM–VDUT > 1.3 V
VCOMI Input Range	–2		+7	V	IOL = +40 mA, IOH = –40 mA
OUTPUT CHARACTERISTICS					
Accuracy					
Absolute Accuracy Error, Load Current	–0.3 – 100		+0.3 + 100	% I_{SET} + µA	IOL, IOH = 25 µA–40 mA, VCOM = 0 V, OUT_L = ±2 V and IOL = 25 µA–40 mA, VCOM = +7 V, OUT_L = +5.7 V and IOH = 25 µA–40 mA, VCOM = –2 V, OUT_L = –0.7 V
VCOM Buffer					
Offset Error	–50		+50	mV	IOL, IOH = 40 mA, VCOMI = 0 V, OUT_L = VCOM
Bias Current	–10	+1	+10	µA	VCOMI = 0 V, OUT_L = VCOM
Gain Error	–0.2		+0.2	%	IOL, IOH = 40 mA, VCOMI = –1 V to +6 V, VOUT = VCOM
Linearity Error	–10		+10	mV	IOL, IOH = 40 mA, VCOMI = –1 V to +6 V, VOUT = VCOM
Output Current TC		<±2		µA/°C	Measured at IOH, IOL = 200 µA
DYNAMIC PERFORMANCE					
Propagation Delay					
$\pm I_{OUT}$ to Inhibit		1.9		ns	VCOM = ±2 V, IOL = +20 mA, IOH = –20 mA
Inhibit to $\pm I_{OUT}$		2.8		ns	VCOM = ±2 V, IOL = +20 mA, IOH = 20 mA
Propagation Delay Matching		<1.8		ns	
I/O Spike		240		mV	VCOM = 0 V, IOL = +20 mA, IOH = –20 mA
Settling Time to 15 mV		<50		ns	IOL = +20 mA, IOH = –20 mA, 50 Ω Load, to ±15 mV
Settling Time to 4 mV		<10		µs	IOL = +20 mA, IOH = –20 mA, 50 Ω Load, to ±4 mV

Specifications subject to change without notice.

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TOTAL FUNCTION SPECIFICATIONS

(All specifications are at T_J = 85°C $\pm$ 5°C, V_S = 11 V $\pm$ 3%, $-V_S$ = -6 V = $\pm$3% unless otherwise noted. All temperature coefficients are measured at T_J = 75°C to 95°C.)

Parameter	Min	Typ	Max	Unit	Test Conditions
OUTPUT CHARACTERISTICS					
Output Leakage Current, V_{OUT} = -1 V to +5 V	-250		$+250$	nA	
Output Leakage Current, V_{OUT} = -2 V to +7 V	-500		$+500$	μA	
Output Capacitance		8		pF	Driver and Load INHIBITED
POWER SUPPLIES					
Total Supply Range		17		V	
Positive Supply		11		V	
Negative Supply		-6		V	
Positive Supply Current			280	mA	Driver = I_{NH}, I_{LOAD} Program = 40 mA, Load = Active
Negative Supply Current			290	mA	Driver = I_{NH}, I_{LOAD} Program = 40 mA, Load = Active
VCCO Current		65		mA	VCCO = 3.3 V, Comparator Output 150 Ω to GND
Total Power Dissipation			4.8	W	Driver = I_{NH}, I_{LOAD} Program = 40 mA, Load = Active
Temperature Sensor Gain Factor		1		μA/K	R_{LOAD} = 10 kΩ, V_{SOURCE} = 11 V

NOTES
Connecting or shorting the decoupling pins to ground will result in the destruction of the device.
Specifications subject to change without notice.

Table I. Driver Truth Table

DATA	$\overline{DATA}$	IOD	$\overline{IOD}$	RLD	$\overline{RLD}$	OUTPUT STATE
0	1	1	0	X	X	V_L
1	0	1	0	X	X	V_H
X	X	0	1	0	1	INH
X	X	0	1	1	0	V_{TERM}

Table II. Comparator Truth Table

VOUT		LEH	$\overline{LEH}$	LEL	$\overline{LEL}$	OUTPUT STATES			
						QH	$\overline{QH}$	QL	$\overline{QL}$
>HCOMP	>LCOMP	1	0	1	0	1	0	1	0
>HCOMP	<LCOMP	1	0	1	0	1	0	0	1
<HCOMP	>LCOMP	1	0	1	0	0	1	1	0
<HCOMP	<LCOMP	1	0	1	0	0	1	0	1
X	X	0	1	0	1	QH (t – 1)	$\overline{QH}$ (t – 1)	QL (t – 1)	$\overline{QL}$ (t – 1)

Table III. Active Load Truth Table

OUT_L	INHL	$\overline{INHL}$	OUTPUT STATES (Including Diode Bridge)		
			IOH	IOL	I(OUT_L)
<VCOM	0	1	V(IOHC) × 10 mA	V(IOLC) × 10 mA	IOL
>VCOM	0	1	V(IOHC) × 10 mA	V(IOLC) × 10 mA	IOH
X	1	0	0	0	0

AD53509

ABSOLUTE MAXIMUM RATINGS[1]

Power Supply Voltage

    VCC to GND .... 13 V
    VEE to GND .... –8 V
    VCC to VEE .... 20 V
    VCCO to GND .... 10 V
    PWR GND HQ GND .... ±0.4 V

Inputs

    DATA, $\overline{\text{DATA}}$, IOD, $\overline{\text{IOD}}$, RLD, $\overline{\text{RLD}}$ ...... +5 V, –2 V
    DATA to $\overline{\text{DATA}}$, IOD to $\overline{\text{IOD}}$, RLD to $\overline{\text{RLD}}$ .... ±3 V
    LEL, $\overline{\text{LEL}}$, LEH, $\overline{\text{LEH}}$ .... +5 V, –2 V
    LEL to $\overline{\text{LEL}}$, LEH to $\overline{\text{LEH}}$ .... ±3 V
    INHL, $\overline{\text{INHL}}$ .... +5 V, –2 V
    INHL to $\overline{\text{INHL}}$ .... ±3 V
    VH, VL, VTERM, VCOM_I to GND .... +8 V, –3 V
    VH to VL .... ±10 V
    (VH–VTERM) and (VTERM – VL) .... ±10 V
    IOHC .... ±6 V
    IOLC .... ±6 V
    HCOMP .... +8 V, –3 V
    LCOMP .... +8 V, –3 V
    HCOMP, LCOMP to V_{OUT} .... ±10 V

Outputs

    V_{OUT} Short Circuit Duration .... Indefinite[2]
    V_{OUT} Inhibit Mode .... +8 V, –3 V
    VHDCPL .... Do Not Connect Except for Cap to V_{CC}
    VLDCPL .... Do Not Connect Except for Cap to V_{EE}
    QH, $\overline{\text{QH}}$, QL, $\overline{\text{QL}}$ Maximum I_{OUT}
        Continuous .... 50 mA
        Surge .... 100 mA
    THERM .... 13 V, 0 V
    IOHRTN, IOLRTN .... +8.5 V, –3.5 V
    VCOM_S Short Circuit Duration .... 3 sec[2]

Environmental

    Operating Temperature (Junction) .... 175°C
    Storage Temperature .... –65°C to +150°C
    Lead Temperature (Soldering, 10 sec)[3] .... 260°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Absolute maximum limits apply individually, not in combination. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]Output short circuit protection is guaranteed as long as proper heat sinking is employed to ensure compliance with the operating temperature limits.

[3]To ensure lead coplanarity (±0.002 inches) and solderability, handling with bare hands should be avoided and the device should be stored in environments at 24°C ±5°C (75°F ± 10°F) with relative humidity not to exceed 65%.

Table IV. Package Thermal Characteristics

Air Flow, FM	θ_{JA}, °C/W
0	33
200	25
400	22

ORDERING GUIDE

Model	Package Description	Shipment Method Quantity per Shipping Container	Package Option
AD53509JSQ	52-Lead LQFP-EDQUAD	90	SQ-52

REV. A

PIN CONFIGURATION

Top pins (left to right): 52 V_{CC}, 51 V_{CC}, 50 $\overline{RLD}$, 49 RLD, 48 PWRGND, 47 VH, 46 PWRGND, 45 VTERM, 44 PWRGND, 43 IOD, 42 $\overline{IOD}$, 41 V_{EE}, 40 V_{EE}

Left pins (top to bottom):
1 V_{CC}
2 VCCO
3 $\overline{QL}$
4 QL
5 VCCO
6 $\overline{QH}$
7 QH
8 VCCO
9 PWRGND
10 $\overline{LEL}$
11 LEL
12 $\overline{LEH}$
13 LEH

PIN 1 IDENTIFIER

AD53509
HEAT SINK UP
(Not to Scale)

Right pins (top to bottom):
39 V_{EE}
38 $\overline{DATA}$
37 DATA
36 INHL
35 $\overline{INHL}$
34 V_{CC}
33 PWRGND
32 V_{EE}
31 V_L
30 IOLC
29 IOHC
28 HQGND
27 IOHRTN

Bottom pins (left to right): 14 NC, 15 THERM, 16 HCOMP, 17 LCOMP, 18 VHDCPL, 19 HQGND2, 20 V_{OUT}, 21 OUT_L, 22 VLDCPL, 23 IOLRTN, 24 VCOMS, 25 VCOMI, 26 NC

NC = NO CONNECT

AD53509
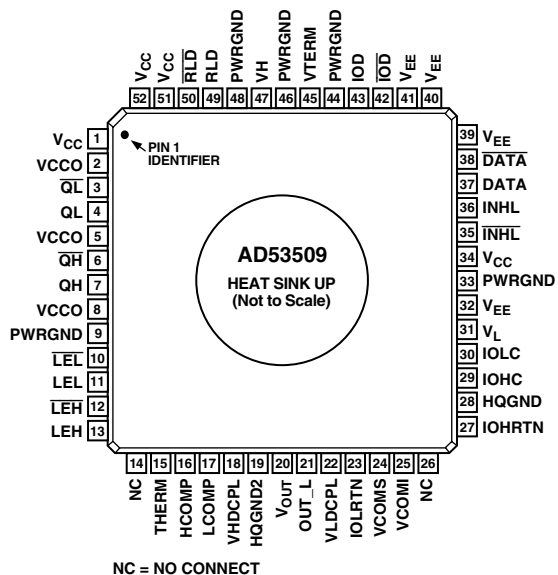
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

52-Lead LQFP–EDQUAD with Integral Heat Slug
(SQ-52)

CENTER FIGURES ARE TYPICAL UNLESS OTHERWISE NOTED

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