ANALOG DEVICES

14-Bit, 165 MSPS TxDAC® D/A Converter

AD9744*

FEATURES

High-Performance Member of Pin-Compatible
    TxDAC Product Family
Excellent Spurious-Free Dynamic Range Performance
SFDR to Nyquist:
    83 dBc @ 5 MHz Output
    80 dBc @ 10 MHz Output
    73 dBc @ 20 MHz Output
SNR @ 5 MHz Output, 125 MSPS: 77 dB
Two's Complement or Straight Binary Data Format
Differential Current Outputs: 2 mA to 20 mA
Power Dissipation: 135 mW @ 3.3 V
Power-Down Mode: 15 mW @ 3.3 V
On-Chip 1.20 V Reference
CMOS-Compatible Digital Interface
Package: 28-Lead SOIC and TSSOP Packages
Edge-Triggered Latches

APPLICATIONS

Wideband Communication Transmit Channel:
    Direct IF
    Base Stations
    Wireless Local Loop
    Digital Radio Link
    Direct Digital Synthesis (DDS)
    Instrumentation

FUNCTIONAL BLOCK DIAGRAM

PRODUCT DESCRIPTION

The AD9744 is a 14-bit resolution, wideband, third generation member of the TxDAC series of high-performance, low power CMOS digital-to-analog converters (DACs). The TxDAC family, consisting of pin-compatible 8-, 10-, 12-, and 14-bit DACs, is specifically optimized for the transmit signal path of communication systems. All of the devices share the same interface options, small outline package, and pinout, providing an upward or downward component selection path based on performance, resolution, and cost. The AD9744 offers exceptional ac and dc performance while supporting update rates up to 165 MSPS.

The AD9744's low power dissipation makes it well suited for portable and low power applications. Its power dissipation can be further reduced to a mere 60 mW with a slight degradation in performance by lowering the full-scale current output. Also, a power-down mode reduces the standby power dissipation to approximately 15 mW. A segmented current source architecture is combined with a proprietary switching technique to reduce spurious components and enhance dynamic performance. Edge-triggered input latches and a 1.2 V temperature compensated
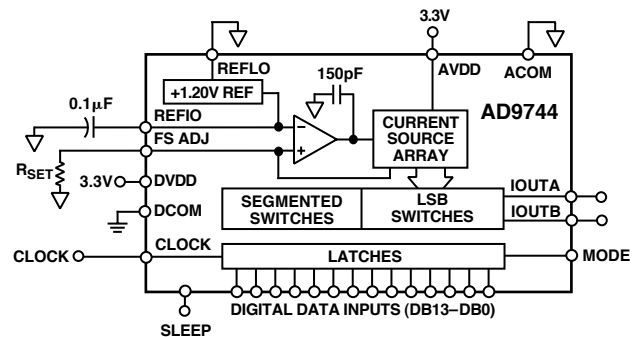
band gap reference have been integrated to provide a complete monolithic DAC solution. The digital inputs support 3 V CMOS logic families.

PRODUCT HIGHLIGHTS

1. The AD9744 is the 14-bit member of the pin-compatible TxDAC family that offers excellent INL and DNL performance.

2. Data input supports two's complement or straight binary data coding.

3. High-speed, single-ended CMOS clock input supports 165 MSPS conversion rate.

4. Low power: Complete CMOS DAC function operates on 135 mW from a 3.0 V to 3.6 V single supply. The DAC full-scale current can be reduced for lower power operation, and a sleep mode is provided for low power idle periods.

5. On-chip voltage reference: The AD9744 includes a 1.2 V temperature-compensated band gap voltage reference.

6. Industry standard 28-lead SOIC and TSSOP packages.

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*Protected by U.S. Patent Numbers 5568145, 5689257, and 5703519.

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AD9744–SPECIFICATIONS

DC SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
RESOLUTION	14			Bits
DC ACCURACY[1]				
Integral Linearity Error (INL)	−5	±0.8	+5	LSB
Differential Nonlinearity (DNL)	−3	±0.5	+3	LSB
ANALOG OUTPUT				
Offset Error	−0.02		+0.02	% of FSR
Gain Error (Without Internal Reference)	−0.5	±0.1	+0.5	% of FSR
Gain Error (With Internal Reference)	−0.5	±0.1	+0.5	% of FSR
Full-Scale Output Current[2]	2.0		20.0	mA
Output Compliance Range	−1.0		+1.25	V
Output Resistance		100		kΩ
Output Capacitance		5		pF
REFERENCE OUTPUT				
Reference Voltage	1.14	1.20	1.26	V
Reference Output Current[3]		100		nA
REFERENCE INPUT				
Input Compliance Range	0.1		1.25	V
Reference Input Resistance (Ext. Ref)		1		MΩ
Small Signal Bandwidth		0.5		MHz
TEMPERATURE COEFFICIENTS				
Offset Drift		0		ppm of FSR/°C
Gain Drift (Without Internal Reference)		±50		ppm of FSR/°C
Gain Drift (With Internal Reference)		±100		ppm of FSR/°C
Reference Voltage Drift		±50		ppm/°C
POWER SUPPLY				
Supply Voltages				
AVDD	3.0	3.3	3.6	V
DVDD	3.0	3.3	3.6	V
Analog Supply Current (I_{AVDD})		33	36	mA
Digital Supply Current (I_{DVDD})[4]		8	9	mA
Supply Current Sleep Mode (I_{AVDD})		5	6	mA
Power Dissipation[4]		135	145	mW
Power Dissipation[5]		145		mW
Power Supply Rejection Ratio—AVDD[6]	−1		+1	% of FSR/V
Power Supply Rejection Ratio—DVDD[6]	−0.04		+0.04	% of FSR/V
OPERATING RANGE	−40		+85	°C

NOTES
[1]Measured at IOUTA, driving a virtual ground.
[2]Nominal full-scale current, I_{OUTFS}, is 32 times the I_{REF} current.
[3]An external buffer amplifier with input bias current <100 nA should be used to drive any external load.
[4]Measured at f_{CLOCK} = 25 MSPS and f_{OUT} = 1.0 MHz.
[5]Measured as unbuffered voltage output with I_{OUTFS} = 20 mA and 50 Ω R_{LOAD} at IOUTA and IOUTB, f_{CLOCK} = 100 MSPS and f_{OUT} = 40 MHz.
[6]±5% Power supply variation.

Specifications subject to change without notice.

DYNAMIC SPECIFICATIONS

(T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, Differential Transformer Coupled Output, 50 Ω Doubly Terminated, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE				
Maximum Output Update Rate (f_{CLOCK})	165			MSPS
Output Settling Time (t_{ST}) (to 0.1%)[1]		11		ns
Output Propagation Delay (t_{PD})		1		ns
Glitch Impulse		5		pV-s
Output Rise Time (10% to 90%)[1]		2.5		ns
Output Fall Time (10% to 90%)[1]		2.5		ns
Output Noise (I_{OUTFS} = 20 mA)[2]		50		pA/√$\overline{Hz}$
Output Noise (I_{OUTFS} = 2 mA)[2]		30		pA/√$\overline{Hz}$
Noise Spectral Density[3]		–154		dBm/Hz
AC LINEARITY				
Spurious-Free Dynamic Range to Nyquist				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz				
0 dBFS Output	77	90		dBc
–6 dBFS Output		87		dBc
–12 dBFS Output		82		dBc
–18 dBFS Output		82		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 1.00 MHz		85		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 2.51 MHz		84		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 10 MHz		80		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 15 MHz		75		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 25 MHz		74		dBc
f_{CLOCK} = 165 MSPS; f_{OUT} = 21 MHz		73		dBc
f_{CLOCK} = 165 MSPS; f_{OUT} = 41 MHz		60		dBc
Spurious-Free Dynamic Range within a Window				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz; 2 MHz Span	84	90		dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 5.02 MHz; 2 MHz Span		90		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 5.03 MHz; 2.5 MHz Span		87		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 5.04 MHz; 4 MHz Span		87		dBc
Total Harmonic Distortion				
f_{CLOCK} = 25 MSPS; f_{OUT} = 1.00 MHz		–86	–77	dBc
f_{CLOCK} = 50 MSPS; f_{OUT} = 2.00 MHz		–77		dBc
f_{CLOCK} = 65 MSPS; f_{OUT} = 2.00 MHz		–77		dBc
f_{CLOCK} = 125 MSPS; f_{OUT} = 2.00 MHz		–77		dBc
Signal-to-Noise Ratio				
f_{CLOCK} = 65 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 20 mA		82		dB
f_{CLOCK} = 65 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 5 mA		88		dB
f_{CLOCK} = 125 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 20 mA		77		dB
f_{CLOCK} = 125 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 5 mA		78		dB
f_{CLOCK} = 165 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 20 mA		70		dB
f_{CLOCK} = 165 MSPS; f_{OUT} = 5 MHz; I_{OUTFS} = 5 mA		70		dB
Multitone Power Ratio (8 Tones at 400 kHz Spacing)				
f_{CLOCK} = 78 MSPS; f_{OUT} = 15.0 MHz to 18.2 MHz				
0 dBFS Output		66		dBc
–6 dBFS Output		68		dBc
–12 dBFS Output		62		dBc
–18 dBFS Output		61		dBc

NOTES

[1] Measured single-ended into 50 Ω load.

[2] Output noise is measured with a full-scale output set to 20 mA with no conversion activity. It is a measure of the thermal noise only.

[3] Noise spectral density is the average noise power normalized to a 1 Hz bandwidth, with the DAC converting and producing an output tone.

Specifications subject to change without notice.

AD9744

DIGITAL SPECIFICATIONS (T_{MIN} to T_{MAX}, AVDD = 3.3 V, DVDD = 3.3 V, I_{OUTFS} = 20 mA, unless otherwise noted.)

Parameter	Min	Typ	Max	Unit
DIGITAL INPUTS				
Logic "1" Voltage	2.1	3		V
Logic "0" Voltage		0	0.9	V
Logic "1" Current	−10		+10	µA
Logic "0" Current	−10		+10	µA
Input Capacitance		5		pF
Input Setup Time (t_S)	2.0			ns
Input Hold Time (t_H)	1.5			ns
Latch Pulsewidth (t_{LPW})	1.5			ns
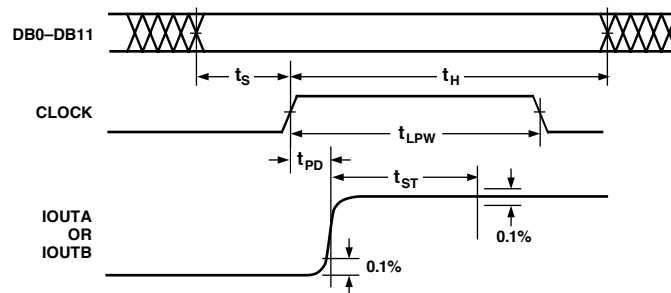
Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS*

Parameter	With Respect to	Min	Max	Unit
AVDD	ACOM	−0.3	+3.9	V
DVDD	DCOM	−0.3	+3.9	V
ACOM	DCOM	−0.3	+0.3	V
AVDD	DVDD	−3.9	+3.9	V
CLOCK, SLEEP	DCOM	−0.3	DVDD + 0.3	V
Digital Inputs	DCOM	−0.3	DVDD + 0.3	V
IOUTA, IOUTB	ACOM	−1.0	AVDD + 0.3	V
REFIO, REFLO, FSADJ	ACOM	−0.3	AVDD + 0.3	V
Junction Temperature			150	°C
Storage Temperature		−65	+150	°C
Lead Temperature (10 sec)			300	°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may effect device reliability.

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Options*
AD9744AR	−40°C to +85°C	28-Lead 300 Mil SOIC	R-28
AD9744ARU	−40°C to +85°C	28-Lead TSSOP	RU-28
AD9744-EB		Evaluation Board	

*R = Small Outline IC; RU = Thin Shrink Small Outline Package

THERMAL CHARACTERISTICS
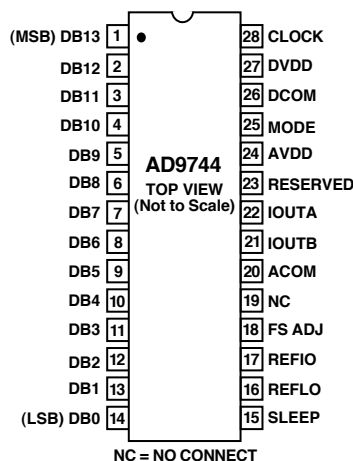**Thermal Resistance**
28-Lead 300-Mil SOIC
  θ_{JA} = 71.4°C/W
28-Lead TSSOP
  θ_{JA} = 97.9°C/W

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PIN CONFIGURATION

```
    (MSB) DB13 |1       •      28| CLOCK
          DB12 |2              27| DVDD
          DB11 |3              26| DCOM
          DB10 |4              25| MODE
           DB9 |5              24| AVDD
           DB8 |6    AD9744    23| RESERVED
           DB7 |7   TOP VIEW   22| IOUTA
           DB6 |8 (Not to Scale)21| IOUTB
           DB5 |9              20| ACOM
           DB4 |10             19| NC
           DB3 |11             18| FS ADJ
           DB2 |12             17| REFIO
           DB1 |13             16| REFLO
     (LSB) DB0 |14             15| SLEEP
```

NC = NO CONNECT

PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	DB13	Most Significant Data Bit (MSB)
2–13	DB12–DB1	Data Bits 12-1
14	DB0	Least Significant Data Bit (LSB)
15	SLEEP	Power-Down Control Input. Active high. Contains active pull-down circuit; it may be left unterminated if not used.
16	REFLO	Reference Ground when internal 1.2 V reference used. Connect to AVDD to disable internal reference.
17	REFIO	Reference Input/Output. Serves as reference input when internal reference disabled (i.e., tie REFLO to AVDD). Serves as 1.2 V reference output when internal reference activated (i.e., tie REFLO to AGND). Requires 0.1 µF capacitor to AGND when internal reference activated.
18	FS ADJ	Full-Scale Current Output Adjust
19	NC	No Internal Connection
20	ACOM	Analog Common
21	IOUTB	Complementary DAC Current Output. Full-scale current when all data bits are 0s.
22	IOUTA	DAC Current Output. Full-scale current when all data bits are 1s.
23	RESERVED	Reserved. Do Not Connect to Common or Supply.
24	AVDD	Analog Supply Voltage (3.3 V)
25	MODE	Selects Input Data Format. Connect to DGND for straight binary, DVDD for two's complement
26	DCOM	Digital Common
27	DVDD	Digital Supply Voltage (3.3 V)
28	CLOCK	Clock Input. Data latched on positive edge of clock.

AD9744

DEFINITIONS OF SPECIFICATIONS

Linearity Error (Also Called Integral Nonlinearity or INL)
Linearity error is defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero to full scale.

Differential Nonlinearity (or DNL)
DNL is the measure of the variation in analog value, normalized to full scale, associated with a 1 LSB change in digital input code.

Monotonicity
A D/A converter is monotonic if the output either increases or remains constant as the digital input increases.

Offset Error
The deviation of the output current from the ideal of zero is called the offset error. For IOUTA, 0 mA output is expected when the inputs are all 0s. For IOUTB, 0 mA output is expected when all inputs are set to 1s.

Gain Error
The difference between the actual and ideal output span. The actual span is determined by the output when all inputs are set to 1s minus the output when all inputs are set to 0s.

Output Compliance Range
The range of allowable voltage at the output of a current output DAC. Operation beyond the maximum compliance limits may cause either output stage saturation or breakdown resulting in nonlinear performance.

Temperature Drift
Temperature drift is specified as the maximum change from the ambient (25°C) value to the value at either T_{MIN} or T_{MAX}. For offset and gain drift, the drift is reported in ppm of full-scale range (FSR) per °C. For reference drift, the drift is reported in ppm per °C.

Power Supply Rejection
The maximum change in the full-scale output as the supplies are varied from nominal to minimum and maximum specified voltages.

Settling Time
The time required for the output to reach and remain within a specified error band about its final value, measured from the start of the output transition.

Glitch Impulse
Asymmetrical switching times in a DAC give rise to undesired output transients that are quantified by a glitch impulse. It is specified as the net area of the glitch in pV-s.

Spurious-Free Dynamic Range
The difference, in dB, between the rms amplitude of the output signal and the peak spurious signal over the specified bandwidth.

Total Harmonic Distortion
THD is the ratio of the rms sum of the first six harmonic components to the rms value of the measured input signal. It is expressed as a percentage or in decibels (dB).

Multitone Power Ratio
The spurious free dynamic range containing multiple carrier tones of equal amplitude. It is measures as the difference between the rms amplitude of a carrier tone to the peak spurious signal in the region of a removed tone.
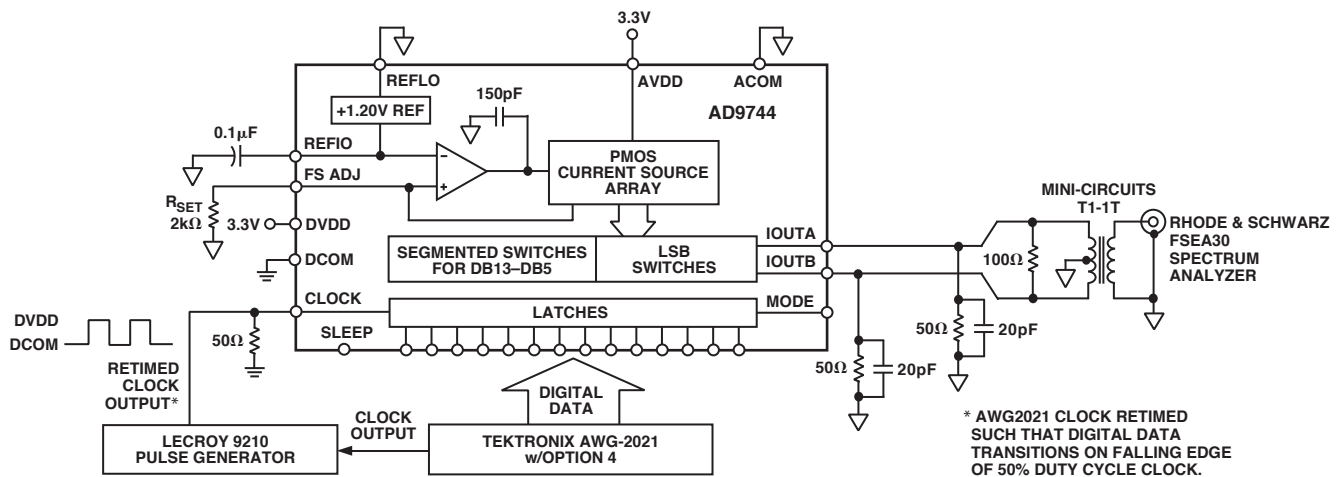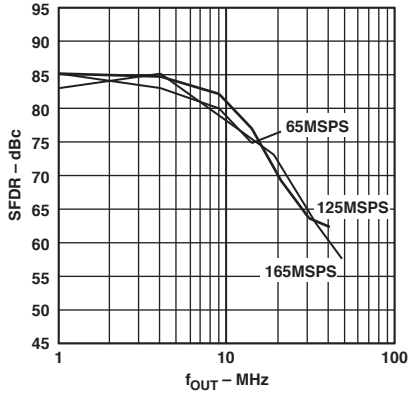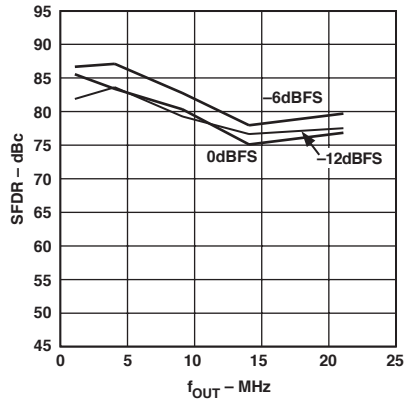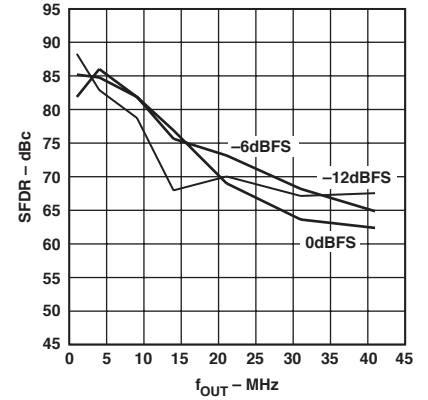

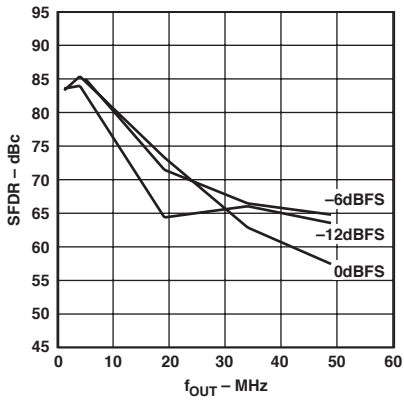Figure 2. Basic AC Characterization Test Set-Up
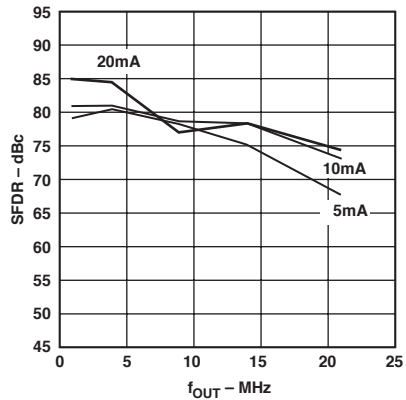
TPC 1. SFDR vs. f_{OUT} @ 0 dBFS

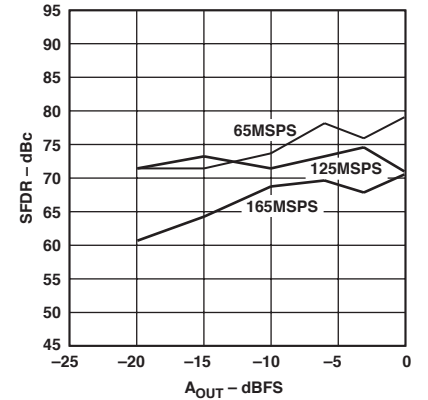TPC 2. SFDR vs. f_{OUT} @ 65 MSPS

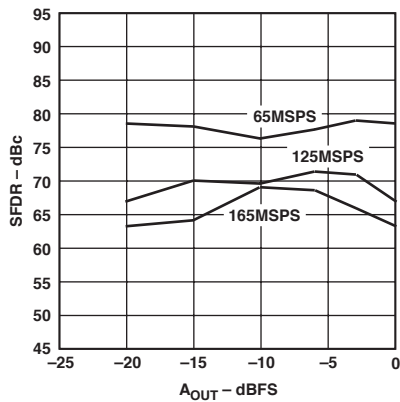TPC 3. SFDR vs. f_{OUT} @ 125 MSPS
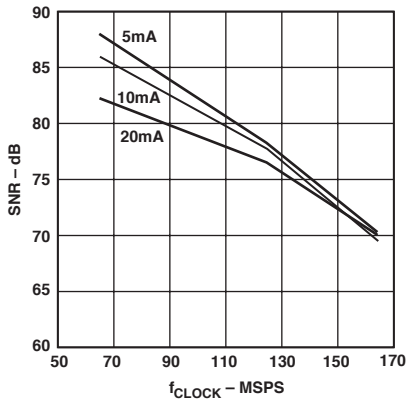

TPC 4. SFDR vs. f_{OUT} @ 165 MSPS

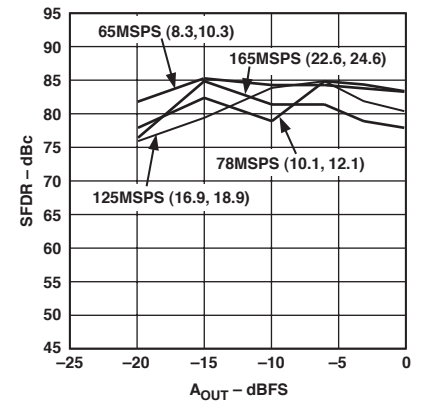TPC 5. SFDR vs. f_{OUT} and I_{OUTFS} @ 65 MSPS and 0 dBFS

TPC 6. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/11$

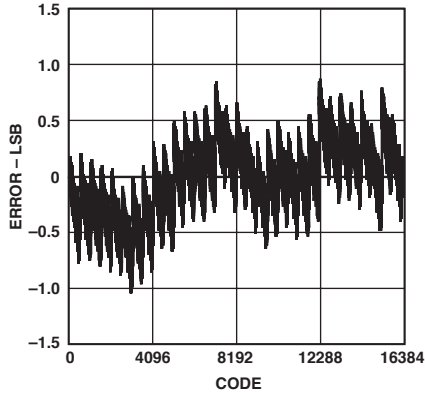TPC 7. Single-Tone SFDR vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/5$

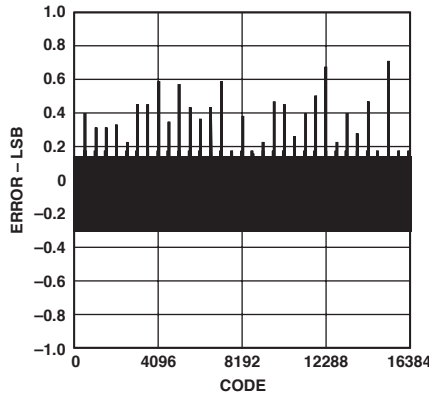TPC 8. SNR vs. f_{CLOCK} and I_{OUTFS} @ $f_{OUT} = 5$ MHz and 0 dBFS

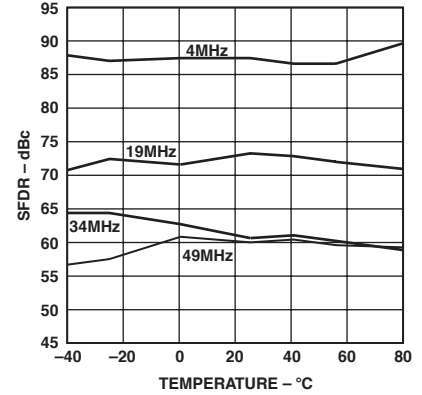TPC 9. Dual-Tone IMD vs. A_{OUT} @ $f_{OUT} = f_{CLOCK}/7$
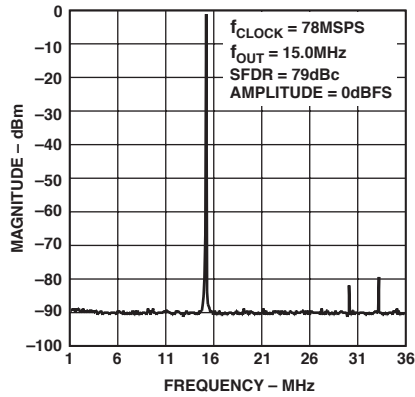
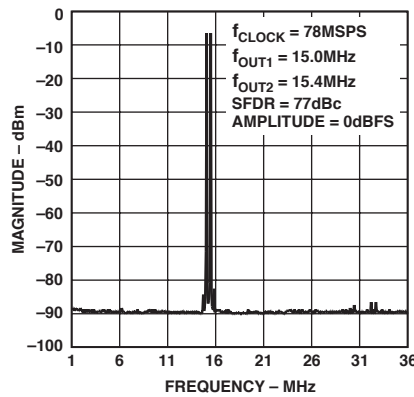# AD9744

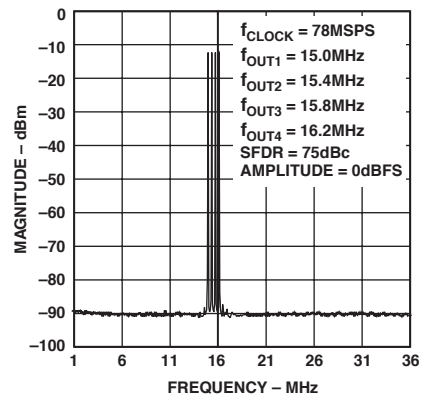TPC 10. Typical INL

TPC 11. Typical DNL

TPC 12. SFDR vs. Temperature @ 165 MSPS, 0 dBFS
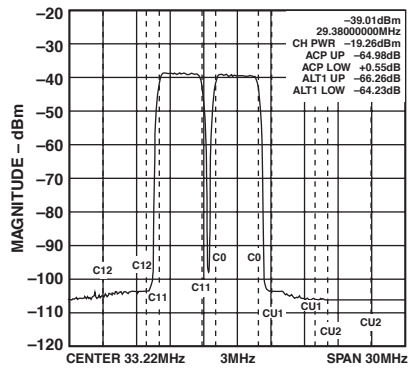

TPC 13. Single-Tone SFDR

TPC 14. Dual-Tone SFDR

TPC 15. Four-Tone SFDR

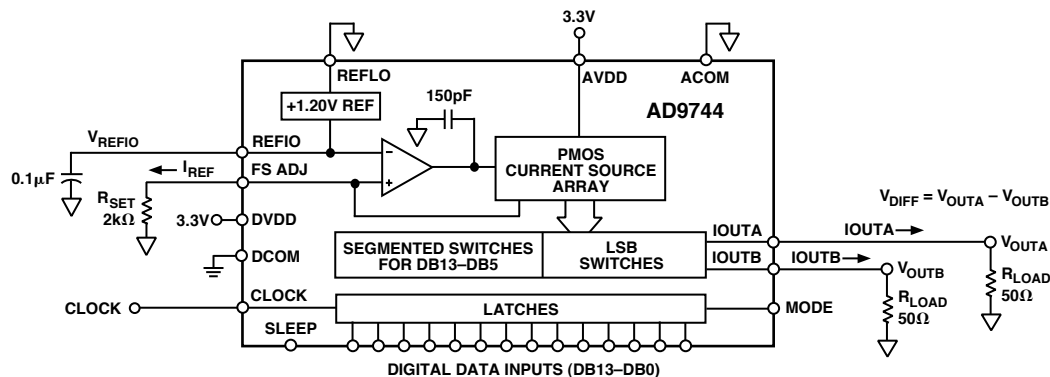TPC 16. Two-Carrier UMTS Spectrum (ACLR = 64 dB)

Figure 3. Simplified Block Diagram

FUNCTIONAL DESCRIPTION

Figure 3 shows a simplified block diagram of the AD9744. The AD9744 consists of a DAC, digital control logic, and full-scale output current control. The DAC contains a PMOS current source array capable of providing up to 20 mA of full-scale current (I_{OUTFS}). The array is divided into 31 equal currents that make up the five most significant bits (MSBs). The next four bits, or middle bits, consist of 15 equal current sources whose value is 1/16th of an MSB current source. The remaining LSBs are binary weighted fractions of the middle bits current sources. Implementing the middle and lower bits with current sources, instead of an R-2R ladder, enhances its dynamic performance for multitone or low amplitude signals and helps maintain the DAC's high output impedance (i.e., >100 kΩ).

All of these current sources are switched to one or the other of the two output nodes (i.e., IOUTA or IOUTB) via PMOS differential current switches. The switches are based on the architecture that was pioneered in the AD9764 family, with further refinements to reduce distortion contributed by the switching transient. This switch architecture also reduces various timing errors and provides matching complementary drive signals to the inputs of the differential current switches.

The analog and digital sections of the AD9744 have separate power supply inputs (i.e., AVDD and DVDD) that can operate independently over a 3.0 V to 3.6 V range. The digital section, which is capable of operating up to a 165 MSPS clock rate, consists of edge-triggered latches and segment decoding logic circuitry. The analog section includes the PMOS current sources, the associated differential switches, a 1.2 V band gap voltage reference, and a reference control amplifier.

The DAC full-scale output current is regulated by the reference control amplifier and can be set from 2 mA to 20 mA via an external resistor, R_{SET}, connected to the full-scale adjust (FSADJ) pin. The external resistor, in combination with both the reference control amplifier and voltage reference V_{REFIO}, sets the reference current I_{REF}, which is replicated to the segmented current sources with the proper scaling factor. The full-scale current, I_{OUTFS}, is 32 times I_{REF}.

REFERENCE OPERATION

The AD9744 contains an internal 1.2 V band gap reference. The internal reference can be disabled by raising REFLO to AVDD. It can also be easily overridden by an external reference with no effect on performance. REFIO serves as either an input or output depending on whether the internal or an external reference is used. To use the internal reference, simply decouple the REFIO pin to ACOM with a 0.1 μF capacitor and connect REFLO to ACOM via a resistance less than 5 Ω. The internal reference voltage will be present at REFIO. If the voltage at REFIO is to be used anywhere else in the circuit, an external buffer amplifier with an input bias current of less than 100 nA should be used. An example of the use of the internal reference is given in Figure 4.
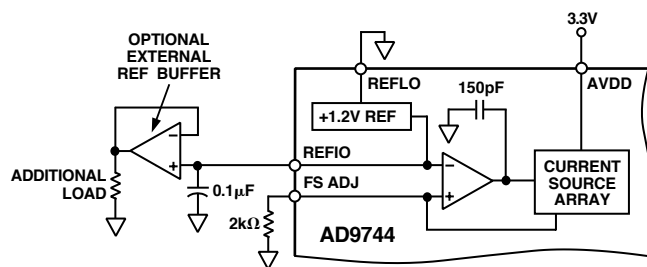

Figure 4. Internal Reference Configuration

An external reference can be applied to REFIO as shown in Figure 5. The external reference may provide either a fixed reference voltage to enhance accuracy and drift performance or a varying reference voltage for gain control. Note that the 0.1 μF compensation capacitor is not required since the internal reference is overridden, and the relatively high input impedance of REFIO minimizes any loading of the external reference.
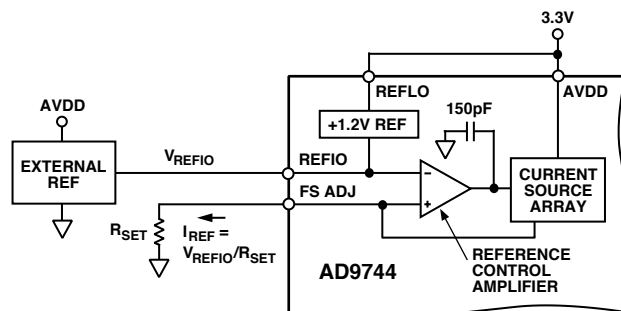

Figure 5. External Reference Configuration

REFERENCE CONTROL AMPLIFIER

The AD9744 contains a control amplifier that is used to regulate the full-scale output current, I_{OUTFS}. The control amplifier is configured as a V-I converter as shown in Figure 4, so that its current output, I_{REF}, is determined by the ratio of the V_{REFIO} and an external resistor, R_{SET}, as stated in Equation 4. I_{REF} is copied to the segmented current sources with the proper scale factor to set I_{OUTFS} as stated in Equation 3.

The control amplifier allows a wide (10:1) adjustment span of I_{OUTFS} over a 2 mA to 20 mA range by setting I_{REF} between 62.5 μA and 625 μA. The wide adjustment span of I_{OUTFS} provides several benefits. The first relates directly to the power dissipation of the AD9744, which is proportional to I_{OUTFS} (refer to the Power Dissipation section). The second relates to the 20 dB adjustment, which is useful for system gain control purposes.

The small signal bandwidth of the reference control amplifier is approximately 500 kHz and can be used for low-frequency small signal multiplying applications.

DAC TRANSFER FUNCTION

Both DACs in the AD9744 provide complementary current outputs, IOUTA and IOUTB. IOUTA will provide a near full-scale current output, I_{OUTFS}, when all bits are high (i.e., DAC CODE = 16383), while IOUTB, the complementary output, provides no current. The current output appearing at *IOUTA* and *IOUTB* is a function of both the input code and I_{OUTFS} and can be expressed as:

$$IOUTA = (DAC\ CODE\ /\ 16384) \times I_{OUTFS} \qquad (1)$$

$$IOUTB = (16383 - DAC\ CODE)\ /\ 16384 \times I_{OUTFS} \qquad (2)$$

where DAC CODE = 0 to 16383 (i.e., decimal representation).

As mentioned previously, I_{OUTFS} is a function of the reference current I_{REF}, which is nominally set by a reference voltage, V_{REFIO}, and external resistor, R_{SET}. It can be expressed as:

$$I_{OUTFS} = 32 \times I_{REF} \qquad (3)$$

where

$$I_{REF} = V_{REFIO}\ /\ R_{SET} \qquad (4)$$

The two current outputs will typically drive a resistive load directly or via a transformer. If dc coupling is required, IOUTA and IOUTB should be directly connected to matching resistive loads, R_{LOAD}, that are tied to analog common, ACOM. Note, R_{LOAD} may represent the equivalent load resistance seen by IOUTA or IOUTB as would be the case in a doubly terminated 50 Ω or 75 Ω cable. The single-ended voltage output appearing at the *IOUTA* and *IOUTB* nodes is simply:

$$V_{OUTA} = IOUTA \times R_{LOAD} \qquad (5)$$

$$V_{OUTB} = IOUTB \times R_{LOAD} \qquad (6)$$

Note the full-scale value of V_{OUTA} and V_{OUTB} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

$$V_{DIFF} = (IOUTA - IOUTB) \times R_{LOAD} \qquad (7)$$

Substituting the values of *IOUTA*, *IOUTB*, I_{REF}, and V_{DIFF} can be expressed as:

$$V_{DIFF} = \{(2 \times DAC\ CODE - 16383)\ /\ 16384\}$$
$$(32 \times R_{LOAD}\ /\ R_{SET}) \times V_{REFIO} \qquad (8)$$

These last two equations highlight some of the advantages of operating the AD9744 differentially. First, the differential operation will help cancel common-mode error sources associated with IOUTA and IOUTB, such as noise, distortion, and dc offsets. Second, the differential code dependent current and subsequent voltage, V_{DIFF}, is twice the value of the single-ended voltage output (i.e., V_{OUTA} or V_{OUTB}), thus providing twice the signal power to the load.

Note, the gain drift temperature performance for a single-ended (V_{OUTA} and V_{OUTB}) or differential output (V_{DIFF}) of the AD9744 can be enhanced by selecting temperature tracking resistors for R_{LOAD} and R_{SET} due to their ratiometric relationship as shown in Equation 8.

ANALOG OUTPUTS

The complementary current outputs in each DAC, IOUTA and IOUTB, may be configured for single-ended or differential operation. IOUTA and IOUTB can be converted into complementary single-ended voltage outputs, V_{OUTA} and V_{OUTB}, via a load resistor, R_{LOAD}, as described in the DAC Transfer Function section by Equations 5 through 8. The differential voltage, V_{DIFF}, existing between V_{OUTA} and V_{OUTB} can also be converted to a single-ended voltage via a transformer or differential amplifier configuration. The ac performance of the AD9744 is optimum and specified using a differential transformer coupled output in which the voltage swing at IOUTA and IOUTB is limited to ±0.5 V.

The distortion and noise performance of the AD9744 can be enhanced when it is configured for differential operation. The common-mode error sources of both IOUTA and IOUTB can be significantly reduced by the common-mode rejection of a transformer or differential amplifier. These common-mode error sources include even-order distortion products and noise. The enhancement in distortion performance becomes more significant as the frequency content of the reconstructed waveform increases and/or its amplitude decreases. This is due to the first order cancellation of various dynamic common-mode distortion mechanisms, digital feedthrough, and noise.

Performing a differential-to-single-ended conversion via a transformer also provides the ability to deliver twice the reconstructed signal power to the load (i.e., assuming no source termination). Since the output currents of IOUTA and IOUTB are complementary, they become additive when processed differentially. A properly selected transformer will allow the AD9744 to provide the required power and voltage levels to different loads.

The output impedance of IOUTA and IOUTB is determined by the equivalent parallel combination of the PMOS switches associated with the current sources and is typically 100 kΩ in parallel with 5 pF. It is also slightly dependent on the output voltage (i.e., V_{OUTA} and V_{OUTB}) due to the nature of a PMOS device. As a result, maintaining IOUTA and/or IOUTB at a virtual ground via an I-V op amp configuration will result in the optimum dc linearity. Note the INL/DNL specifications for the AD9744 are measured with IOUTA maintained at a virtual ground via an op amp.

IOUTA and IOUTB also have a negative and positive voltage compliance range that must be adhered to in order to achieve optimum performance. The negative output compliance range of –1.0 V is set by the breakdown limits of the CMOS process. Operation beyond this maximum limit may result in a breakdown of the output stage and affect the reliability of the AD9744.

The positive output compliance range is slightly dependent on the full-scale output current, I_{OUTFS}. It degrades slightly from its nominal 1.2 V for an I_{OUTFS} = 20 mA to 1.0 V for an I_{OUTFS} = 2 mA. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUTA and IOUTB does not exceed 0.5 V.

DIGITAL INPUTS
The AD9744's digital section consists of 14 input bit channel and a clock input. The 14-bit parallel data inputs follow standard positive binary coding where DB13 is the most significant bit (MSB) and DB0 is the least significant bit (LSB). IOUTA produces a full-scale output current when all data bits are at Logic 1. IOUTB produces a complementary output with the full-scale current split between the two outputs as a function of the input code.
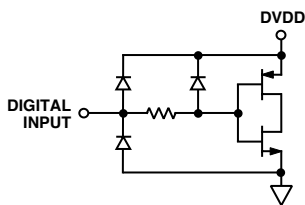

Figure 6. Equivalent Digital Input

The digital interface is implemented using an edge-triggered master/slave latch. The DAC output updates on the rising edge of the clock and is designed to support a clock rate as high as 165 MSPS. The clock can be operated at any duty cycle that meets the specified latch pulsewidth. The setup and hold times can also be varied within the clock cycle as long as the specified minimum times are met, although the location of these transition edges may affect digital feedthrough and distortion performance. Best performance is typically achieved when the input data transitions on the falling edge of a 50% duty cycle clock.

DAC TIMING
Input Clock and Data Timing Relationship
Dynamic performance in a DAC is dependent on the relationship between the position of the clock edges and the point in time at which the input data changes. The AD9744 is rising edge triggered, and so exhibits dynamic performance sensitivity when the data transition is close to this edge. In general, the goal when applying the AD9744 is to make the data transition close to the falling clock edge. This becomes more important as the sample rate increases. Figure 7 shows the relationship of SFDR to clock placement with different sample rates. Note that at the lower sample rates, more tolerance is allowed in clock placement, while at higher rates, more care must be taken.
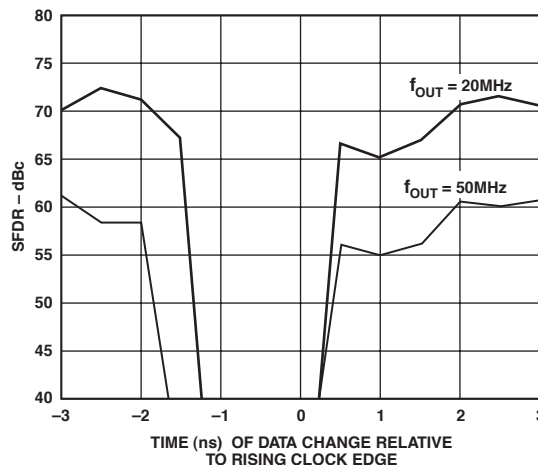

Figure 7. SFDR vs. Clock Placement @ f_{OUT} = 20 MHz and 50 MHz

Sleep Mode Operation
The AD9744 has a power-down function that turns off the output current and reduces the supply current to less than 4 mA over the specified supply range of 3.0 V to 3.6 V and temperature range. This mode can be activated by applying a logic level 1 to the SLEEP pin. The SLEEP pin logic threshold is equal to $0.5 \times AVDD$. This digital input also contains an active pull-down circuit that ensures the AD9744 remains enabled if this input is left disconnected. The AD9744 takes less than 50 ns to power down and approximately 5 µs to power back up.

POWER DISSIPATION
The power dissipation, P_D, of the AD9744 is dependent on several factors that include:

- The power supply voltages (AVDD and DVDD)
- The full-scale current output I_{OUTFS}
- The update rate f_{CLOCK}
- The reconstructed digital input waveform

The power dissipation is directly proportional to the analog supply current, I_{AVDD}, and the digital supply current, I_{DVDD}. I_{AVDD} is directly proportional to I_{OUTFS} as shown in Figure 8 and is insensitive to f_{CLOCK}. Conversely, I_{DVDD} is dependent on both the digital input waveform, f_{CLOCK}, and digital supply DVDD. Figure 9 shows I_{DVDD} as a function of full-scale sine wave output ratios (f_{OUT}/f_{CLOCK}) for various update rates with DVDD = 3.3 V.
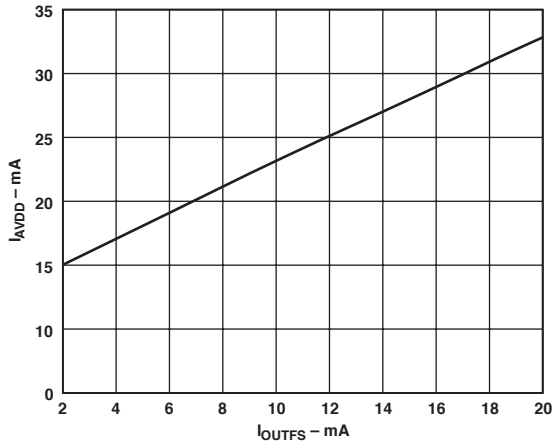
AD9744
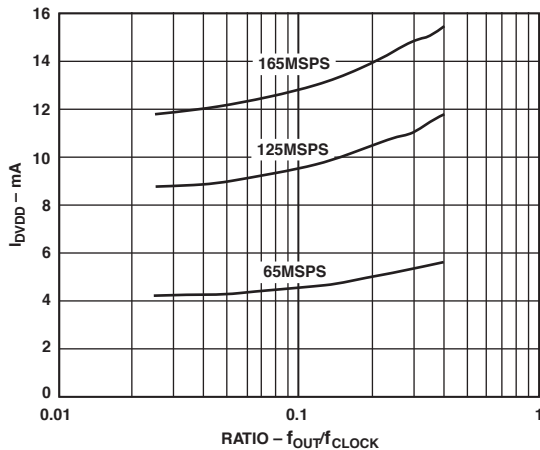

Figure 8. I_{AVDD} vs. I_{OUTFS}

Figure 9. I_{DVDD} vs. Ratio @ DVDD = 3.3 V

APPLYING THE AD9744

Output Configurations

The following sections illustrate some typical output configurations for the AD9744. Unless otherwise noted, it is assumed that I_{OUTFS} is set to a nominal 20 mA. For applications requiring the optimum dynamic performance, a differential output configuration is suggested. A differential output configuration may consist of either an RF transformer or a differential op amp configuration. The transformer configuration provides the optimum high-frequency performance and is recommended for any application that allows ac coupling. The differential op amp configuration is suitable for applications requiring dc coupling, a bipolar output, signal gain, and/or level shifting, within the bandwidth of the chosen op amp.

A single-ended output is suitable for applications requiring a unipolar voltage output. A positive unipolar output voltage will result if IOUTA and/or IOUTB is connected to an appropriately sized load resistor, R_{LOAD}, referred to ACOM. This configuration may be more suitable for a single-supply system requiring a dc-coupled, ground referred output voltage. Alternatively, an amplifier could be configured as an I-V converter, thus converting IOUTA or IOUTB into a negative unipolar voltage. This configuration provides the best dc linearity since IOUTA or IOUTB is maintained at a virtual ground.

DIFFERENTIAL COUPLING USING A TRANSFORMER

An RF transformer can be used to perform a differential-to-single-ended signal conversion as shown in Figure 10. A differentially coupled transformer output provides the optimum distortion performance for output signals whose spectral content lies within the transformer's passband. An RF transformer, such as the Mini-Circuits T1–1T, provides excellent rejection of common-mode distortion (i.e., even-order harmonics) and noise over a wide frequency range. It also provides electrical isolation and the ability to deliver twice the power to the load. Transformers with different impedance ratios may also be used for impedance matching purposes. Note that the transformer provides ac coupling only.
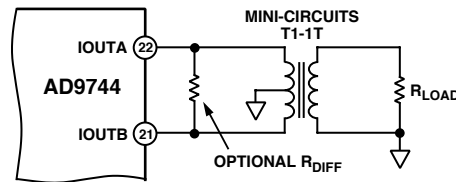

Figure 10. Differential Output Using a Transformer

The center tap on the primary side of the transformer must be connected to ACOM to provide the necessary dc current path for both IOUTA and IOUTB. The complementary voltages appearing at IOUTA and IOUTB (i.e., V_{OUTA} and V_{OUTB}) swing symmetrically around ACOM and should be maintained with the specified output compliance range of the AD9744. A differential resistor, R_{DIFF}, may be inserted in applications where the output of the transformer is connected to the load, R_{LOAD}, via a passive reconstruction filter or cable. R_{DIFF} is determined by the transformer's impedance ratio and provides the proper source termination that results in a low VSWR. Note that approximately half the signal power will be dissipated across R_{DIFF}.

DIFFERENTIAL COUPLING USING AN OP AMP

An op amp can also be used to perform a differential-to-single-ended conversion as shown in Figure 11. The AD9744 is configured with two equal load resistors, R_{LOAD}, of 25 Ω. The differential voltage developed across IOUTA and IOUTB is converted to a single-ended signal via the differential op amp configuration. An optional capacitor can be installed across IOUTA and IOUTB, forming a real pole in a low-pass filter. The addition of this capacitor also enhances the op amp's distortion performance by preventing the DACs high slewing output from overloading the op amp's input.
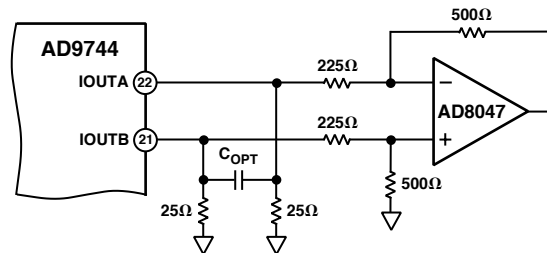

Figure 11. DC Differential Coupling Using an Op Amp

The common-mode rejection of this configuration is typically determined by the resistor matching. In this circuit, the differential op amp circuit using the AD8047 is configured to provide some additional signal gain. The op amp must operate off of a dual supply since its output is approximately ±1.0 V. A high-speed amplifier capable of preserving the differential performance

of the AD9744 while meeting other system level objectives (i.e., cost, power) should be selected. The op amp's differential gain, its gain setting resistor values, and full-scale output swing capabilities should all be considered when optimizing this circuit.

The differential circuit shown in Figure 12 provides the necessary level shifting required in a single-supply system. In this case, AVDD, which is the positive analog supply for both the AD9744 and the op amp, is also used to level-shift the differential output of the AD9744 to midsupply (i.e., AVDD/2). The AD8041 is a suitable op amp for this application.
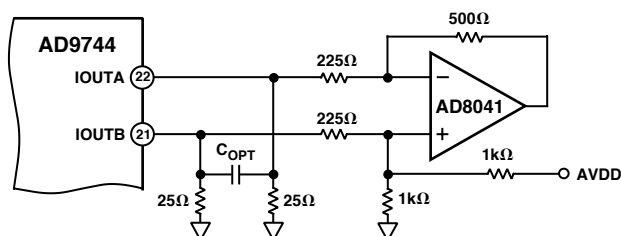

Figure 12. Single Supply DC Differential Coupled Circuit

SINGLE-ENDED UNBUFFERED VOLTAGE OUTPUT
Figure 13 shows the AD9744 configured to provide a unipolar output range of approximately 0 V to 0.5 V for a doubly terminated 50 Ω cable since the nominal full-scale current, I_{OUTFS}, of 20 mA flows through the equivalent R_{LOAD} of 25 Ω. In this case, R_{LOAD} represents the equivalent load resistance seen by IOUTA or IOUTB. The unused output (IOUTA or IOUTB) can be connected to ACOM directly or via a matching R_{LOAD}. Different values of I_{OUTFS} and R_{LOAD} can be selected as long as the positive compliance range is adhered to. One additional consideration in this mode is the integral nonlinearity (INL) as discussed in the Analog Output section of this data sheet. For optimum INL performance, the single-ended, buffered voltage output configuration is suggested.
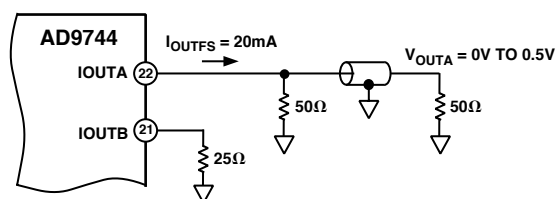

Figure 13. 0 V to 0.5 V Unbuffered Voltage Output

SINGLE-ENDED, BUFFERED VOLTAGE OUTPUT CONFIGURATION
Figure 14 shows a buffered single-ended output configuration in which the op amp U1 performs an I-V conversion on the AD9744 output current. U1 maintains IOUTA (or IOUTB) at a virtual ground, minimizing the nonlinear output impedance effect on the DAC's INL performance as discussed in the Analog Output section. Although this single-ended configuration typically provides the best dc linearity performance, its ac distortion performance at higher DAC update rates may be limited by U1's slew rate capabilities. U1 provides a negative unipolar output voltage and its full-scale output voltage is simply the product of R_{FB} and I_{OUTFS}. The full-scale output should be set within U1's voltage output swing capabilities by scaling I_{OUTFS} and/or R_{FB}. An improvement in ac distortion performance may result with a reduced I_{OUTFS} since the signal current U1 will be required to sink less signal current.
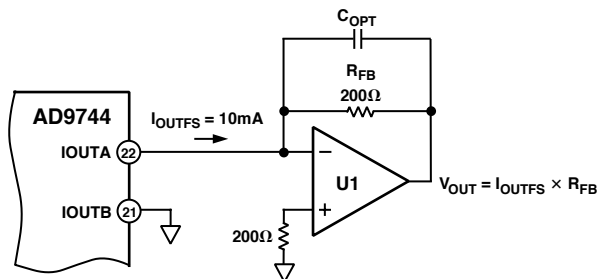

Figure 14. Unipolar Buffered Voltage Output

POWER AND GROUNDING CONSIDERATIONS, POWER SUPPLY REJECTION
Many applications seek high-speed and high-performance under less than ideal operating conditions. In these application circuits, the implementation and construction of the printed circuit board is as important as the circuit design. Proper RF techniques must be used for device selection, placement, and routing as well as power supply bypassing and grounding to ensure optimum performance. Figures 19 to 22 illustrate the recommended printed circuit board ground, power, and signal plane layouts that are implemented on the AD9744 evaluation board.

One factor that can measurably affect system performance is the ability of the DAC output to reject dc variations or ac noise superimposed on the analog or digital dc power distribution. This is referred to as the power supply rejection ratio. For dc variations of the power supply, the resulting performance of the DAC directly corresponds to a gain error associated with the DAC's full-scale current, I_{OUTFS}. AC noise on the dc supplies is common in applications where the power distribution is generated by a switching power supply. Typically, switching power supply noise will occur over the spectrum from tens of kHz to several MHz. The PSRR vs frequency of the AD9744 AVDD supply over this frequency range is shown in Figure 15.
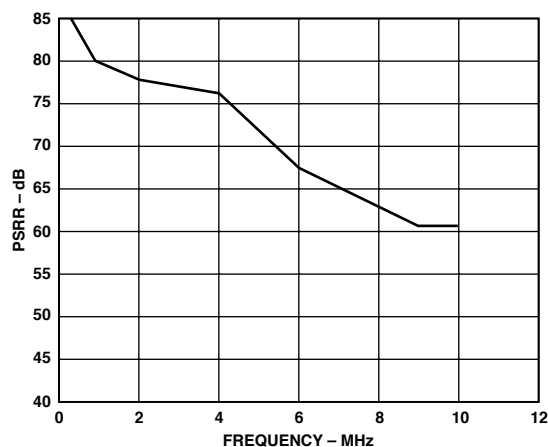

Figure 15. Power Supply Rejection Ratio

Note that the units in Figure 15 are given in units of (amps out/ volts in). Noise on the analog power supply has the effect of modulating the internal switches, and therefore the output current. The voltage noise on AVDD, therefore, will be added in a nonlinear manner to the desired IOUT. Due to the relative different size of these switches, PSRR is very code dependent. This can produce a mixing effect that can modulate low-frequency power supply noise to higher frequencies. Worst-case PSRR for

AD9744

either one of the differential DAC outputs will occur when the full-scale current is directed toward that output. As a result, the PSRR measurement in Figure 15 represents a worst-case condition in which the digital inputs remain static and the full-scale output current of 20 mA is directed to the DAC output being measured.

An example serves to illustrate the effect of supply noise on the analog supply. Suppose a switching regulator with a switching frequency of 250 kHz produces 10 mV of noise and, for simplicity sake (i.e., ignore harmonics), all of this noise is concentrated at 250 kHz. To calculate how much of this undesired noise will appear as current noise superimposed on the DAC's full-scale current, I_{OUTFS}, one must determine the PSRR in dB using Figure 15 at 250 kHz. To calculate the PSRR for a given R_{LOAD}, such that the units of PSRR are converted from A/V to V/V, adjust the curve in Figure 15 by the scaling factor $20 \times \log(R_{LOAD})$. For instance, if R_{LOAD} is 50 Ω, the PSRR is reduced by 34 dB (i.e., PSRR of the DAC at 250 kHz which is 85 dB in Figure 15 becomes 51 dB V_{OUT}/V_{IN}).

Proper grounding and decoupling should be a primary objective in any high-speed, high resolution system. The AD9744 features separate analog and digital supply and ground pins to optimize the management of analog and digital ground currents in a system. In general, AVDD, the analog supply, should be decoupled to ACOM, the analog common, as close to the chip as physically possible. Similarly, DVDD, the digital supply, should be decoupled to DCOM as close to the chip as physically possible.

For those applications that require a single 3.3 V supply for both the analog and digital supplies, a clean analog supply may be generated using the circuit shown in Figure 16. The circuit consists of a differential LC filter with separate power supply and return lines. Lower noise can be attained by using low ESR type electrolytic and tantalum capacitors.
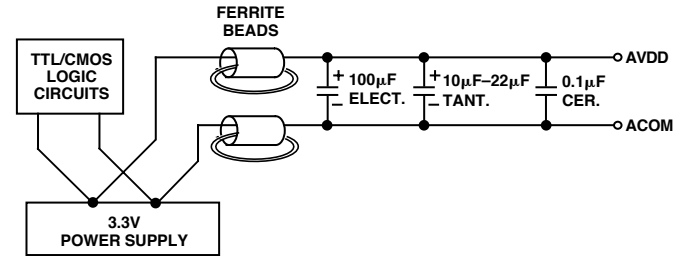

Figure 16. Differential LC Filter for Single 3.3 V Applications

EVALUATION BOARD
General Description
The TxDAC Family Evaluation Board allows for easy set up and testing of any TxDAC product in the 28-lead SOIC package. Careful attention to layout and circuit design combined with a prototyping area allow the user to evaluate the AD9744 easily and effectively in any application where high resolution, high-speed conversion is required.

This board allows the user the flexibility to operate the AD9744 in various configurations. Possible output configurations include transformer coupled, resistor terminated, and single and differential outputs. The digital inputs are designed to be driven from various word generators, with the on-board option to add a resistor network for proper load termination. Provisions are also made to operate the AD9744 with either the internal or external reference or to exercise the power-down feature.
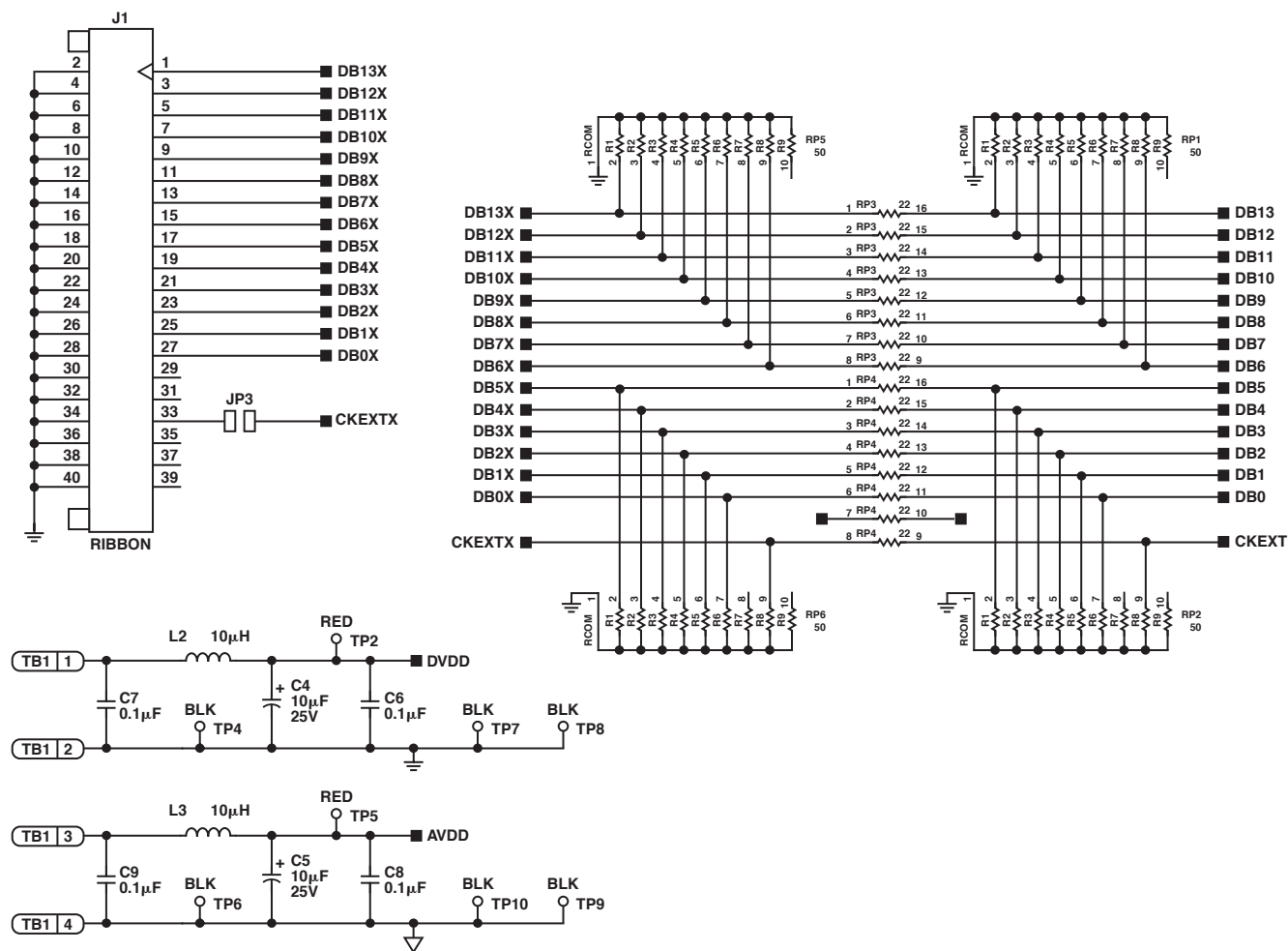
Figure 17. Evaluation Board: Power Supply and Digital Inputs
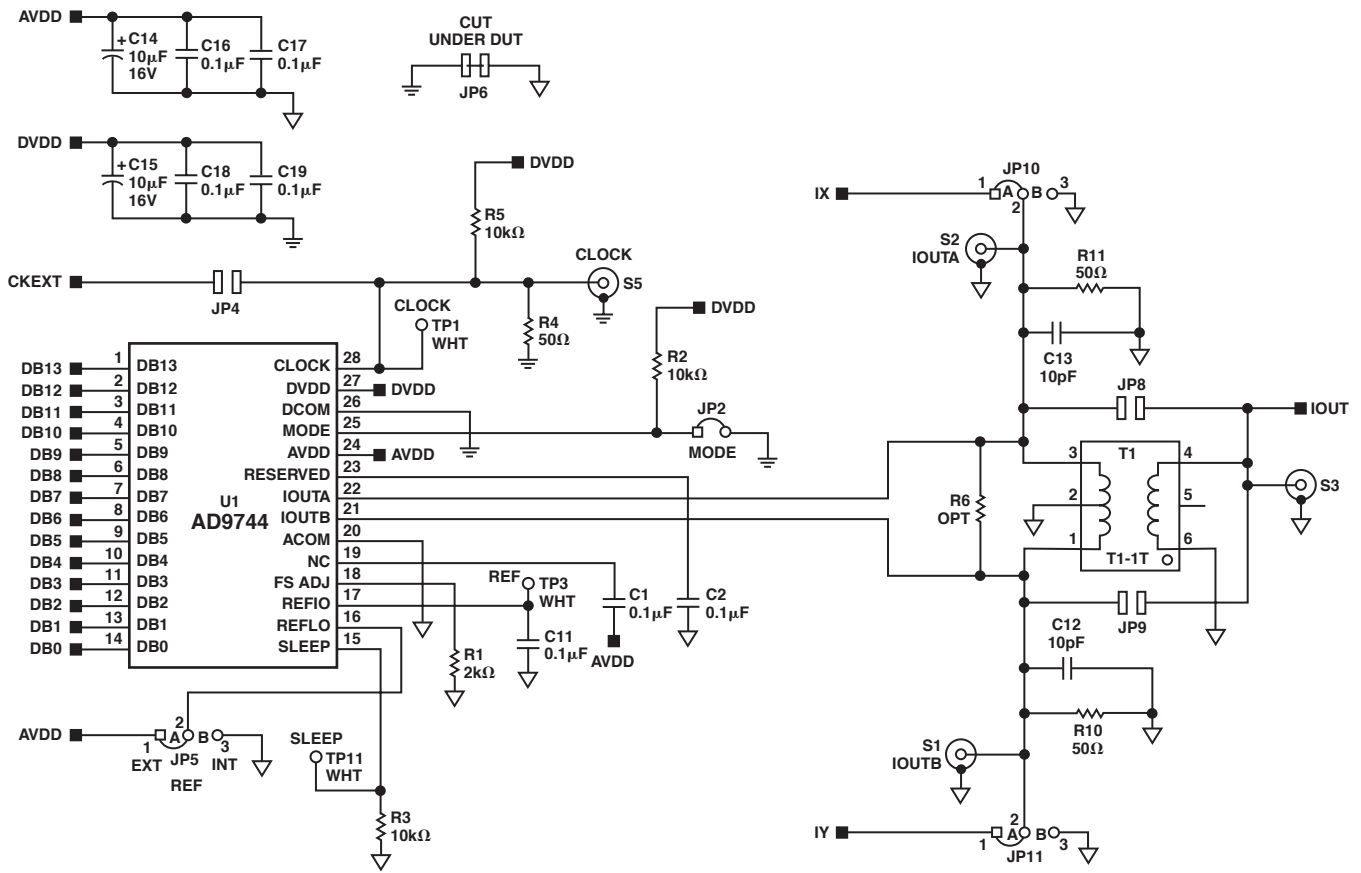
AD9744
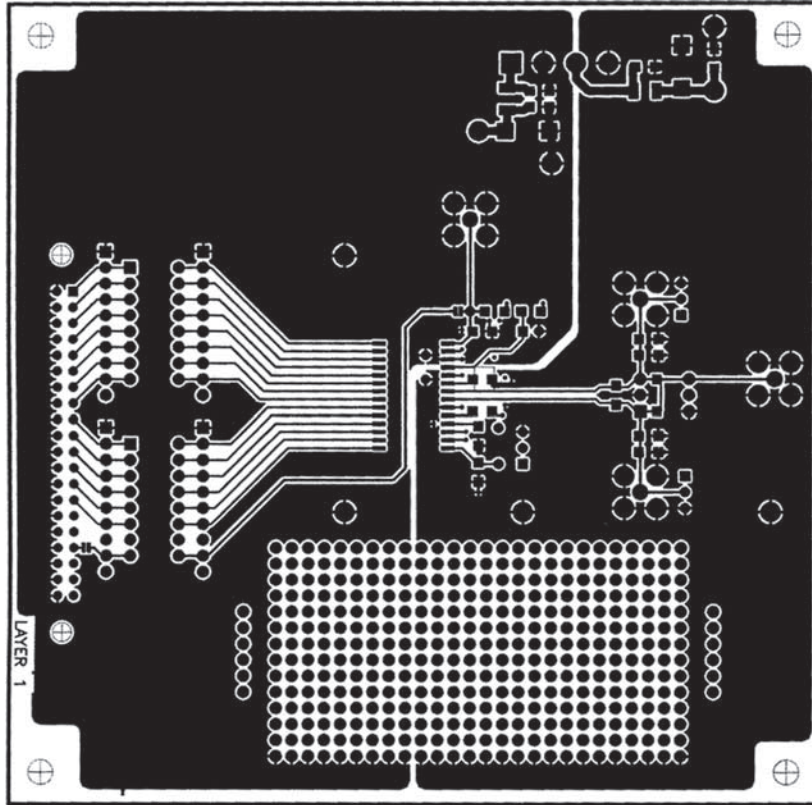

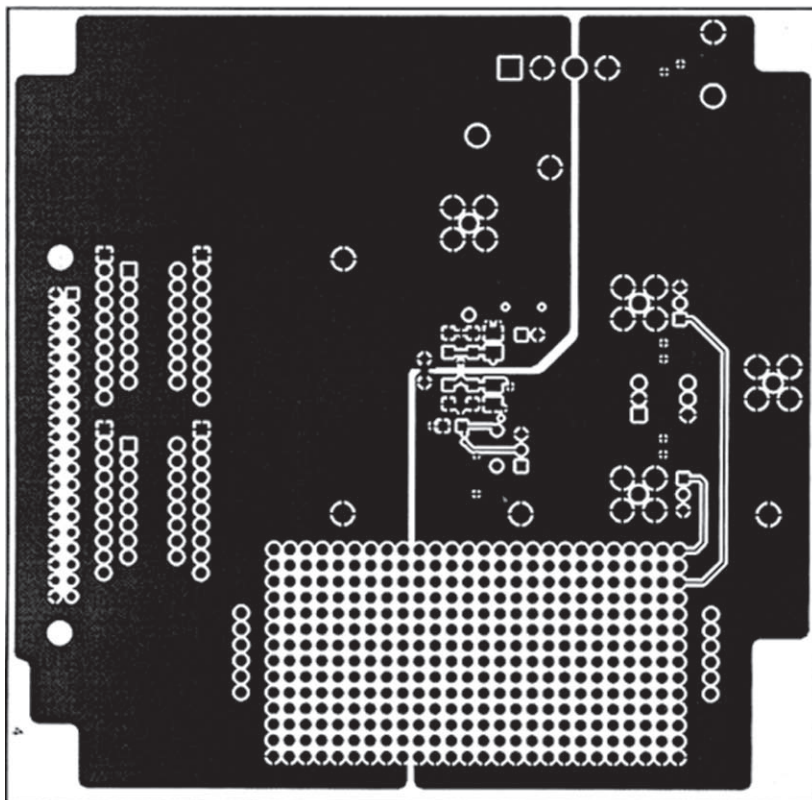Figure 18. Evaluation Board: Output Signal Conditioning

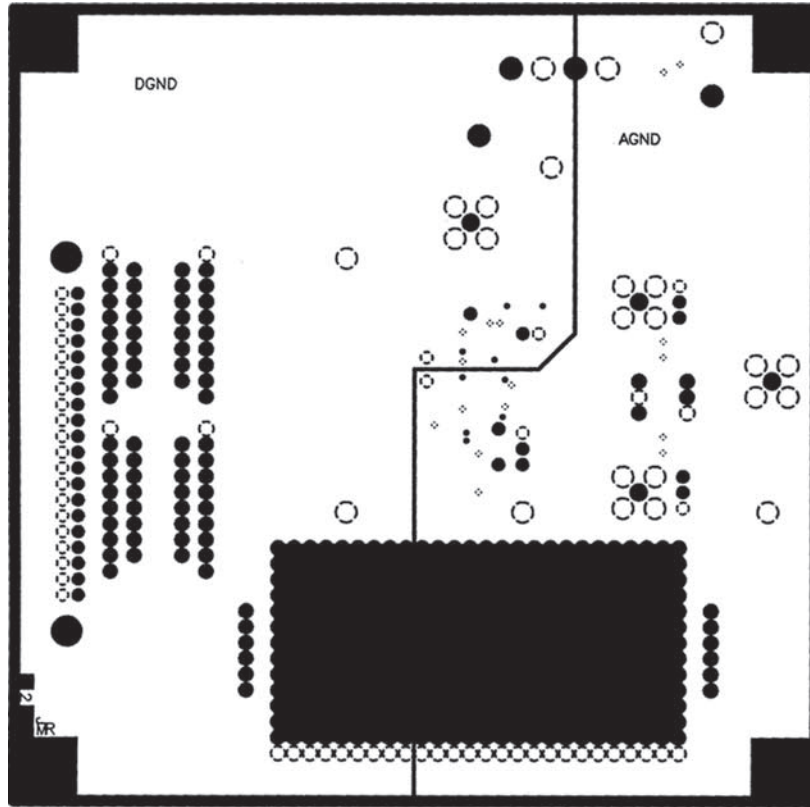Figure 19. Primary Side
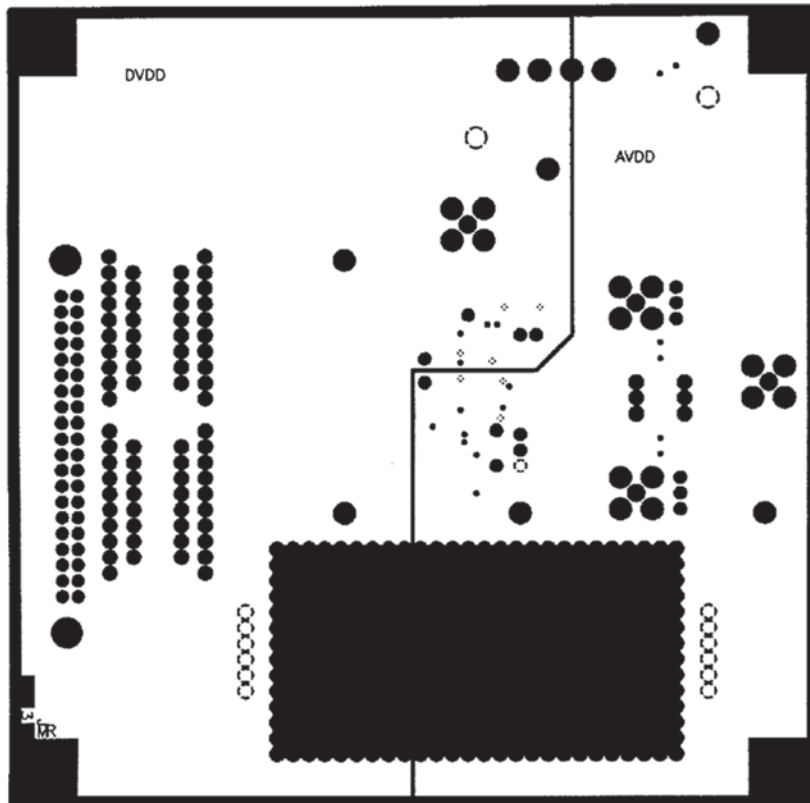

Figure 20. Secondary Side
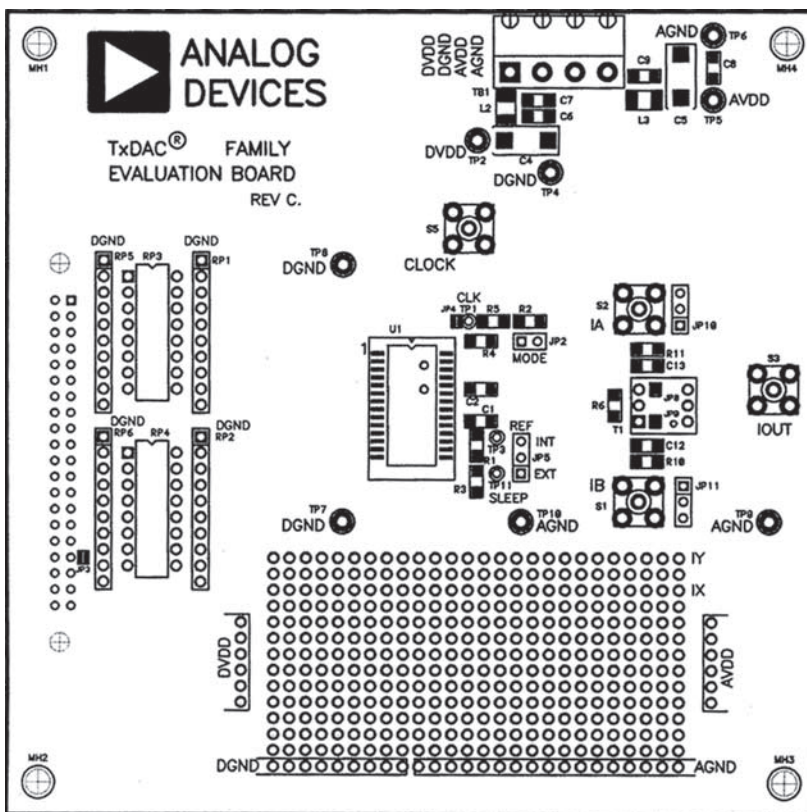
Figure 21. Ground Plane

Figure 22. Power Plane

REV. 0

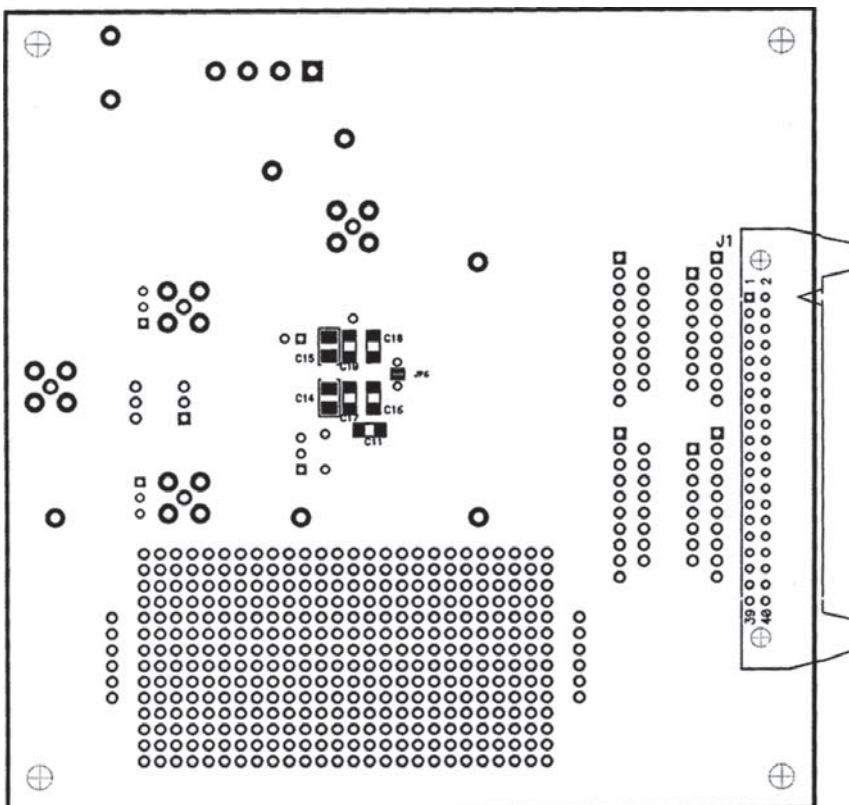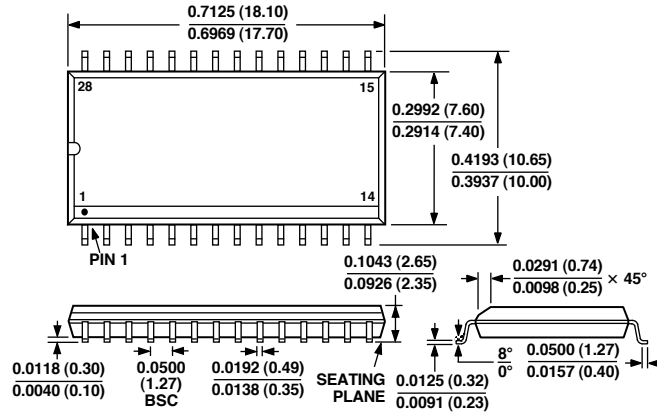Figure 23. Assembly – Primary Side

Figure 24. Assembly – Secondary Side

AD9744

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm)

28-Lead Standard Small Outline Package (SOIC)
(R-28)

0.7125 (18.10)
0.6969 (17.70)

28   15

0.2992 (7.60)
0.2914 (7.40)

0.4193 (10.65)
0.3937 (10.00)

1   14

PIN 1

0.1043 (2.65)
0.0926 (2.35)

0.0291 (0.74)
0.0098 (0.25) × 45°

0.0118 (0.30)
0.0040 (0.10)

0.0500
(1.27)
BSC

0.0192 (0.49)
0.0138 (0.35)

SEATING
PLANE

0.0125 (0.32)
0.0091 (0.23)

8°
0°

0.0500 (1.27)
0.0157 (0.40)

28-Lead Thin Shrink SO Package (TSSOP)
(RU-28)

0.386 (9.80)
0.378 (9.60)

28   15

0.177 (4.50)
0.169 (4.30)

0.256 (6.50)
0.246 (6.25)

1   14

PIN 1

0.006 (0.15)
0.002 (0.05)

0.0433
(1.10)
MAX

SEATING
PLANE

0.0256 (0.65)
BSC

0.0118 (0.30)
0.0075 (0.19)

0.0079 (0.20)
0.0035 (0.090)

8°
0°

0.028 (0.70)
0.020 (0.50)

REV. 0