Precision Low Noise, Low Input Bias Current Operational Amplifiers

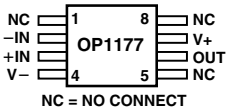
OP1177/OP2177/OP4177

FEATURES
Low Offset Voltage: 60 μV Max
Very Low Offset Voltage Drift: 0.7 μV/°C Max
Low Input Bias Current: 2 nA Max
Low Noise: 8 nV/√Hz
CMRR, PSRR, and A_{VO} > 120 dB Min
Low Supply Current: 400 μA/Amp
Dual Supply Operation: ±2.5 V to ±15 V
Unity Gain Stable
No Phase Reversal
Inputs Internally Protected Beyond Supply Voltage

APPLICATIONS
Wireless Base Station Control Circuits
Optical Network Control Circuits
Instrumentation
Sensors and Controls
Thermocouples
RTDs
Strain Bridges
Shunt Current Measurements
Precision Filters

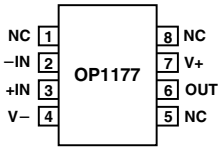
FUNCTIONAL BLOCK DIAGRAM

8-Lead MSOP (RM-Suffix)



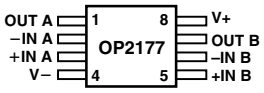
NC = NO CONNECT

8-Lead SOIC (R-Suffix)

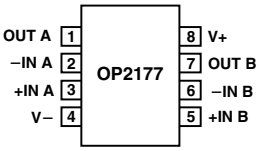


NC = NO CONNECT

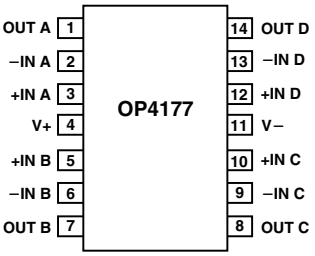
8-Lead MSOP (RM-Suffix)



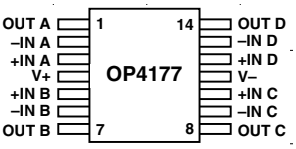
8-Lead SOIC (R-Suffix)



14-Lead SOIC (R-Suffix)



14-Lead TSSOP (RU-Suffix)



GENERAL DESCRIPTION

The OPx177 family consists of very high-precision, single, dual, and quad amplifiers featuring extremely low offset voltage and drift, low input bias current, low noise, and low power consumption. Outputs are stable with capacitive loads of over 1,000 pF with no external compensation. Supply current is less than 500 μA per amplifier at 30 V. Internal 500 Ω series resistors protect the inputs, allowing input signal levels several volts beyond either supply without phase reversal.

Unlike previous high-voltage amplifiers with very low offset voltages, the OP1177 and OP2177 are available in the tiny MSOP 8-lead surface-mount package, while the OP4177 is available in TSSOP14. Moreover, specified performance in the MSOP/TSSOP package is identical to performance in the SOIC package.

OPx177 family offers the widest specified temperature range of any high-precision amplifier in surface-mount packaging. All versions are fully specified for operation from –40°C to +125°C for the most demanding operating environments.

Applications for these amplifiers include precision diode power measurement, voltage and current level setting, and level detection in optical and wireless transmission systems. Additional applications include line powered and portable instrumentation and controls—thermocouple, RTD, strain-bridge, and other sensor signal conditioning—and precision filters.

The OP1177 (single) and the OP2177 (dual) amplifiers are available in the 8-lead MSOP and 8-lead SOIC packages. The OP4177 (quad) is available in 14-lead narrow SOIC and 14-lead TSSOP packages. MSOP and TSSOP packages are available in tape and reel only.

REV. B

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OP1177/OP2177/OP4177–SPECIFICATIONS (@ V_S = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ*	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
OP1177	V_{OS}			15	60	µV
OP2177/4177	V_{OS}			15	75	µV
OP1177/2177	V_{OS}	–40°C < T_A < +125°C		25	100	µV
OP4177	V_{OS}	–40°C < T_A < +125°C		25	120	µV
Input Bias Current	I_B	–40°C < T_A < +125°C	–2	+0.5	+2	nA
Input Offset Current	I_{OS}	–40°C < T_A < +125°C	–1	+0.2	+1	nA
Input Voltage Range			–3.5		+3.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –3.5 V to +3.5 V	120	126		dB
		–40°C < T_A < +125°C	118	125		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ , V_O = –3.5 V to +3.5 V	1,000	2,000		V/mV
Offset Voltage Drift						
OP1177/OP2177	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		0.2	0.7	µV/°C
OP4177	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		0.3	0.9	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA, –40°C < T_A < +125°C	+4	+4.1		V
Output Voltage Low	V_{OL}	I_L = 1 mA, –40°C < T_A < +125°C		–4.1	–4	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1.2 V		±10		mA
POWER SUPPLY						
Power Supply Rejection Ratio						
OP1177	PSRR	V_S = ±2.5 V to ±15 V,	120	130		dB
		–40°C < T_A < +125°C	115	125		dB
OP2177/OP4177	PSRR	V_S = ±2.5 V to ±15 V,	118	121		dB
		–40°C < T_A < +125°C	114	120		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		400	500	µA
		–40°C < T_A < +125°C		500	600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.7		V/µs
Gain Bandwidth Product	GBP			1.3		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.4		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		7.9	8.5	nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS						
CHANNEL SEPARATION	C_S	DC		0.01		µV/V
		f = 100 kHz		–120		dB

*Typical values cover all parts within one standard deviation of the average value. Average values, given in many competitors' data sheets as "typical," give unrealistically low estimates for parameters that can have both positive and negative values.

Specifications subject to change without notice.

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ*	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage						
OP1177	V_{OS}			15	60	µV
OP2177/OP4177	V_{OS}			15	75	µV
OP1177/OP2177	V_{OS}	–40°C < T_A < +125°C		25	100	µV
OP4177	V_{OS}	–40°C < T_A < +125°C		25	120	µV
Input Bias Current	I_B	–40°C < T_A < +125°C	–2	+0.5	+2	nA
Input Offset Current	I_{OS}	–40°C < T_A < +125°C	–1	+0.2	+1	nA
Input Voltage Range			–13.5		+13.5	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = –13.5 V to +13.5 V				
		–40°C < T_A < +125°C	120	125		dB
Large Signal Voltage Gain	A_{VO}	R_L = 2 kΩ , V_O = –13.5 V to +13.5 V	1,000	3,000		V/mV
Offset Voltage Drift						
OP1177/OP2177	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		0.2	0.7	µV/°C
OP4177	$\Delta V_{OS}/\Delta T$	–40°C < T_A < +125°C		0.3	0.9	µV/°C
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	I_L = 1 mA, –40°C < T_A < +125°C	+14	+14.1		V
Output Voltage Low	V_{OL}	I_L = 1 mA, –40°C < T_A < +125°C		–14.1	–14	V
Output Current	I_{OUT}	$V_{DROPOUT}$ < 1.2 V		±10		mA
Short Circuit Current	I_{SC}			±35		mA
POWER SUPPLY						
Power Supply Rejection Ratio						
OP1177	PSRR	V_S = ±2.5 V to ±15 V,	120	130		dB
		–40°C < T_A < +125°C	115	125		dB
OP2177/OP4177	PSRR	V_S = ±2.5 V to ±15 V,	118	121		dB
		–40°C < T_A < +125°C	114	120		dB
Supply Current/Amplifier	I_{SY}	V_O = 0 V		400	500	µA
		–40°C < T_A < +125°C		500	600	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 2 kΩ		0.7		V/µs
Gain Bandwidth Product	GBP			1.3		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.4		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		7.9	8.5	nV/√Hz
Current Noise Density	i_n	f = 1 kHz		0.2		pA/√Hz
MULTIPLE AMPLIFIERS						
CHANNEL SEPARATION	C_S	DC		0.01		µV/V
		f = 100 kHz		–120		dB

*Typical values cover all parts within one standard deviation of the average value. Average values, given in many competitors' data sheets as "typical," give unrealistically low estimates for parameters that can have both positive and negative values.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

Supply Voltage . . . . . 36 V
Input Voltage . . . . . V_{S-} to V_{S+}
Differential Input Voltage . . . . . ±Supply Voltage
Storage Temperature Range
R, RM, and RU Packages . . . . . –65°C to +150°C
Operating Temperature Range
OP1177/OP2177/OP4177 . . . . . –40°C to +125°C
Junction Temperature Range
R, RM, and RU Packages . . . . . –65°C to +150°C
Lead Temperature Range (Soldering, 10 sec) . . . . . 300°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Type	θ_{JA}[1]	θ_{JC}	Unit
8-Lead MSOP (RM)[2]	190	44	°C/W
8-Lead SOIC (R)	158	43	°C/W
14-Lead SOIC (R)	120	36	°C/W
14-Lead TSSOP (RU)	240	43	°C/W

NOTES
[1]θ_{JA} is specified for worst-case conditions, i.e., θ_{JA} is specified for device soldered in circuit board for surface-mount packages.
[2]MSOP is only available in tape and reel.

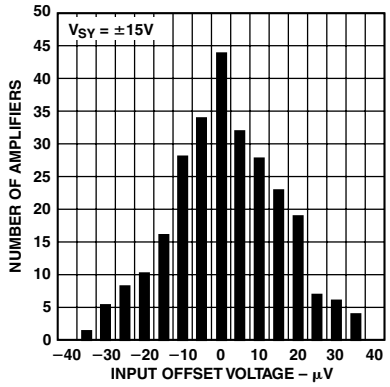
ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding Information
OP1177ARM	–40°C to +125°C	8-Lead MINI_SOIC	RM-8	AZA
OP1177AR	–40°C to +125°C	8-Lead SOIC	SO-8	
OP2177ARM	–40°C to +125°C	8-Lead MINI_SOIC	RM-8	B2A
OP2177AR	–40°C to +125°C	8-Lead SOIC	SO-8	
OP4177AR	–40°C to +125°C	14-Lead SOIC	R-14	
OP4177ARU	–40°C to +125°C	14-Lead TSSOP	RU-14	

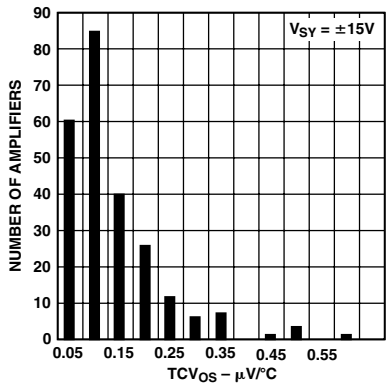
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP1177/OP2177/OP4177 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

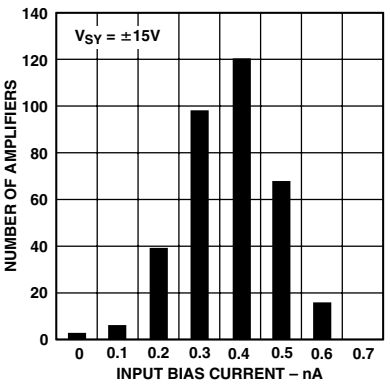
Typical Performance Characteristics–OP1177/OP2177/OP4177



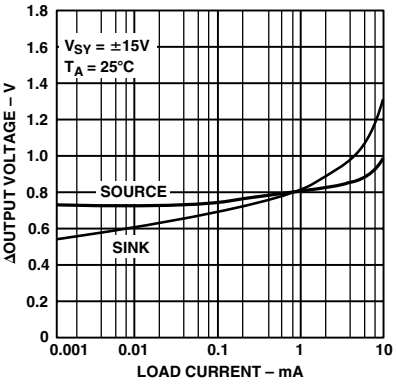
TPC 1. Input Offset Voltage Distribution



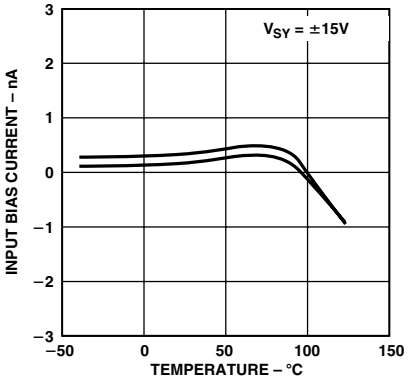
TPC 2. Input Offset Voltage Drift Distribution



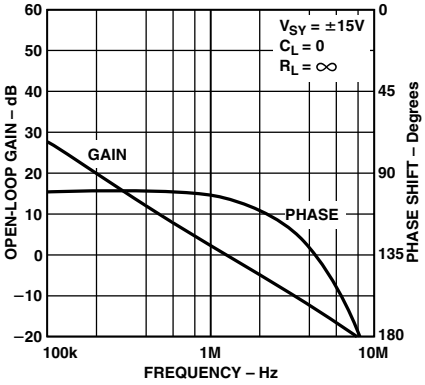
TPC 3. Input Bias Current Distribution



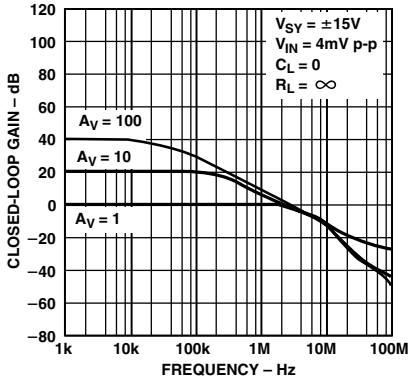
TPC 4. Output Voltage to Supply Rail vs. Load Current



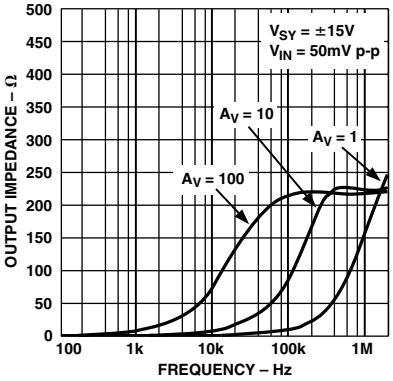
TPC 5. Input Bias Current vs. Temperature



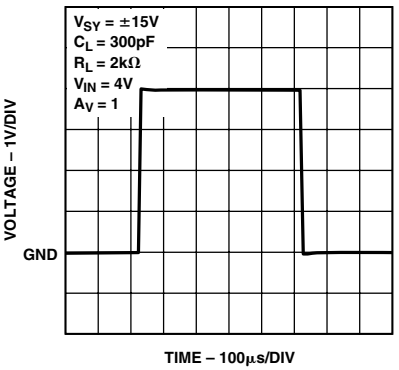
TPC 6. Open-Loop Gain and Phase Shift vs. Frequency



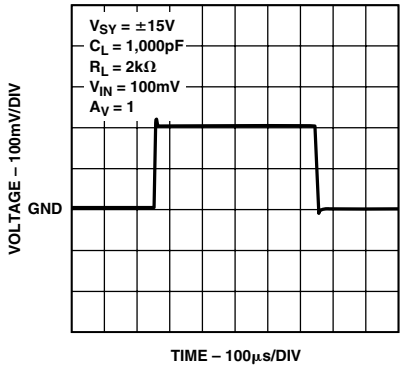
TPC 7. Closed-Loop Gain vs. Frequency



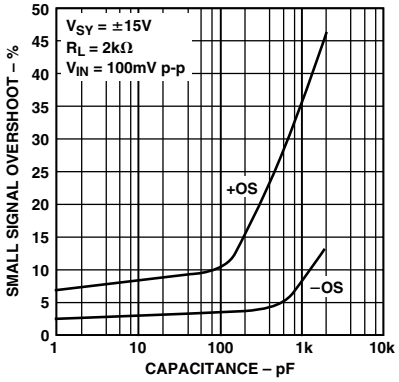
TPC 8. Output Impedance vs. Frequency



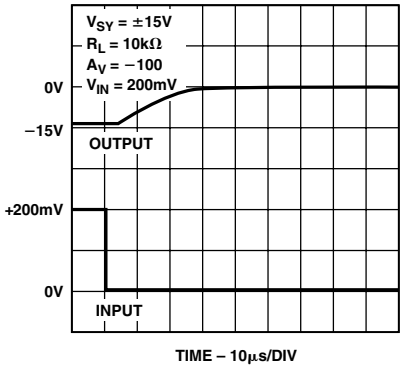
TPC 9. Large Signal Transient Response



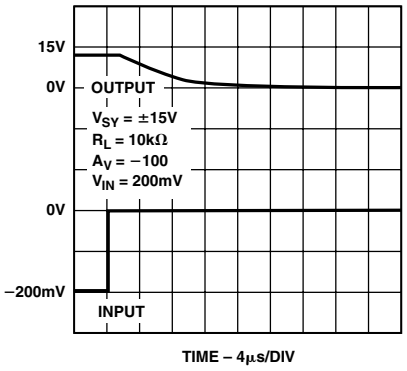
TPC 10. Small Signal Transient Response



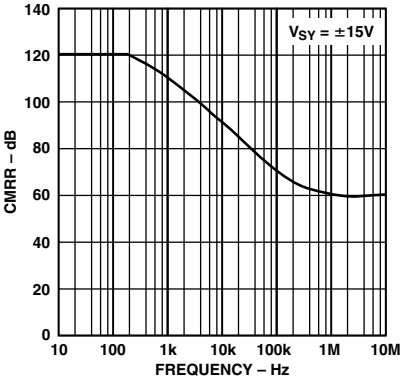
TPC 11. Small Signal Overshoot vs. Load Capacitance



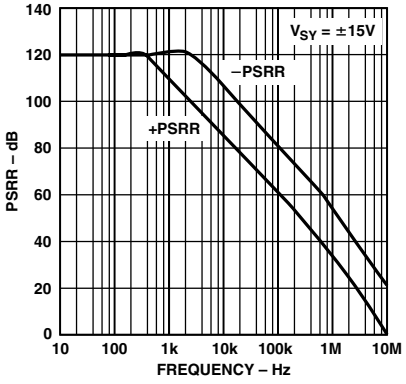
TPC 12. Positive Overvoltage Recovery



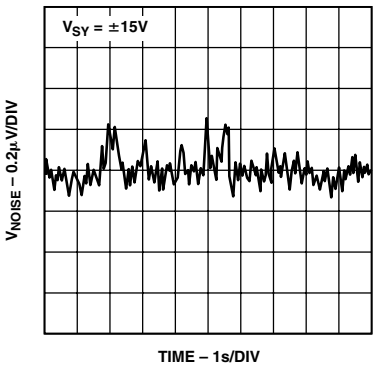
TPC 13. Negative Overvoltage Recovery



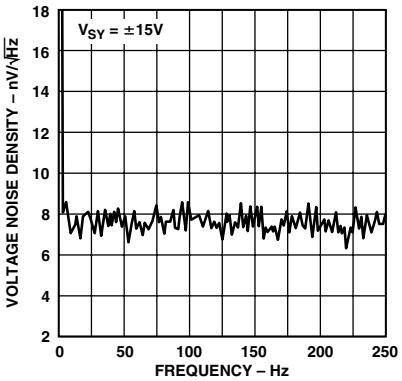
TPC 14. CMRR vs. Frequency



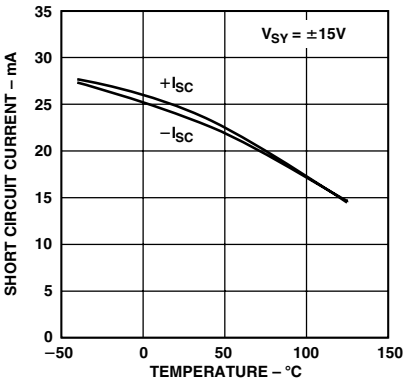
TPC 15. PSRR vs. Frequency



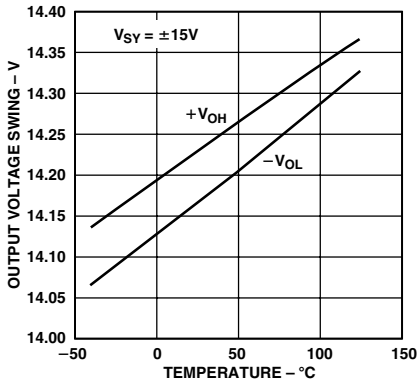
TPC 16. 0.1 Hz to 10 Hz Input Voltage Noise



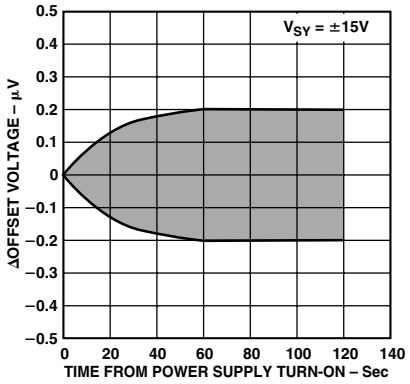
TPC 17. Voltage Noise Density



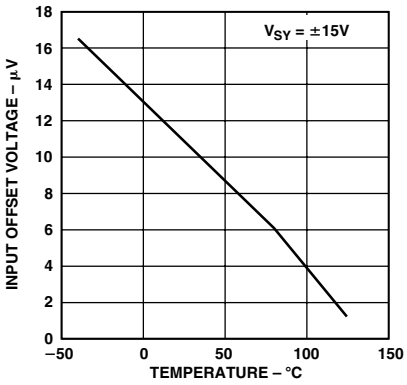
TPC 18. Short Circuit Current vs. Temperature



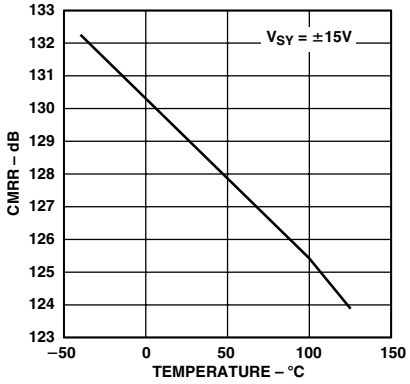
TPC 19. Output Voltage Swing vs. Temperature



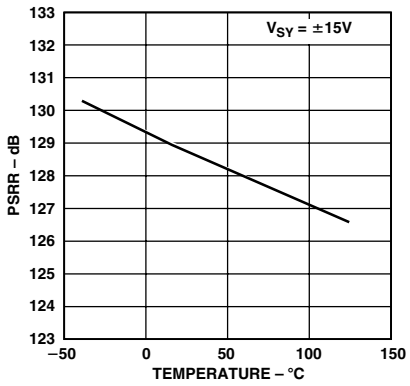
TPC 20. Warm-Up Drift



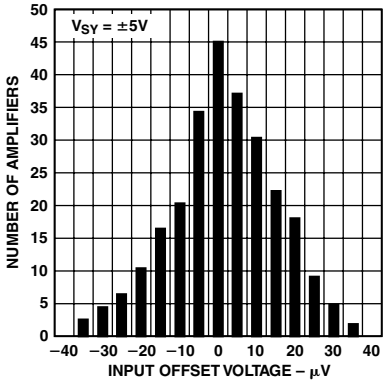
TPC 21. $|V_{OS}|$ vs. Temperature



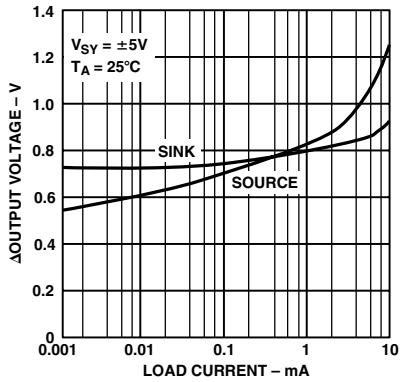
TPC 22. CMRR vs. Temperature



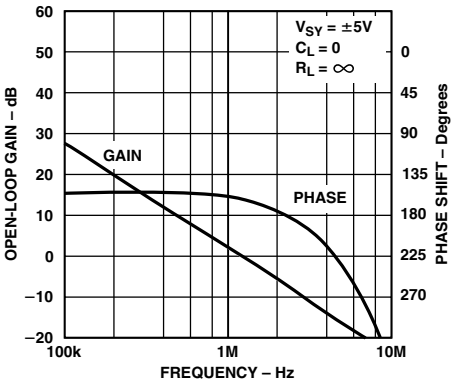
TPC 23. PSRR vs. Temperature



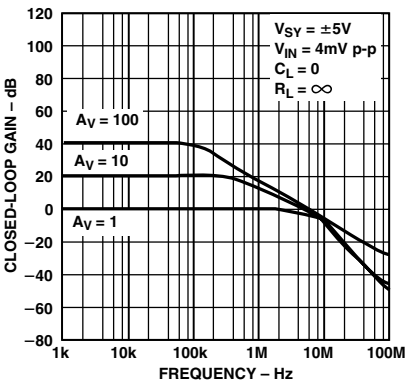
TPC 24. Input Offset Voltage Distribution



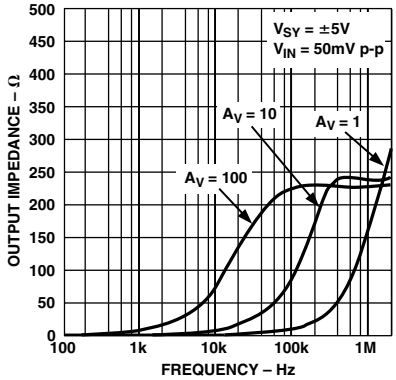
TPC 25. Output Voltage to Supply Rail vs. Load Current



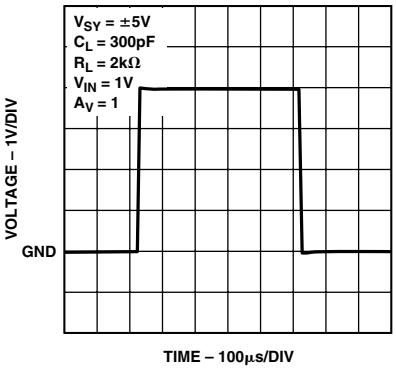
TPC 26. Open-Loop Gain and Phase Shift vs. Frequency



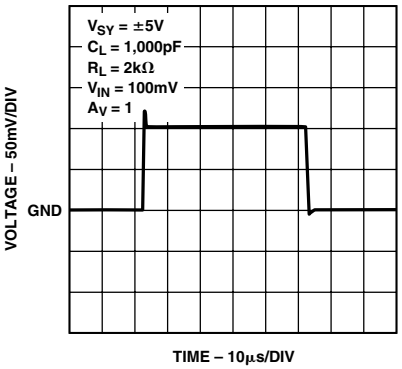
TPC 27. Closed-Loop Gain vs. Frequency



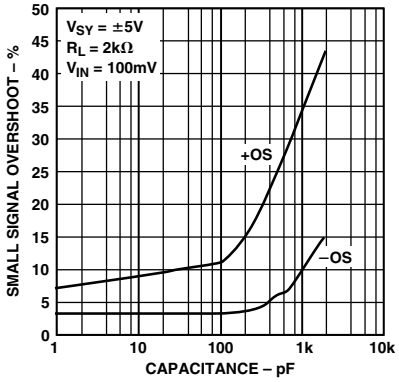
TPC 28. Output Impedance vs. Frequency



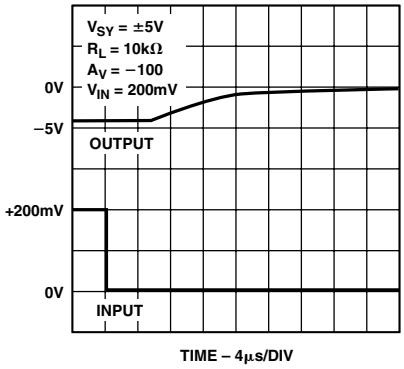
TPC 29. Large Signal Transient Response



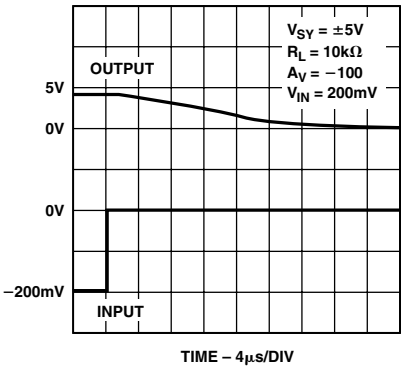
TPC 30. Small Signal Transient Response



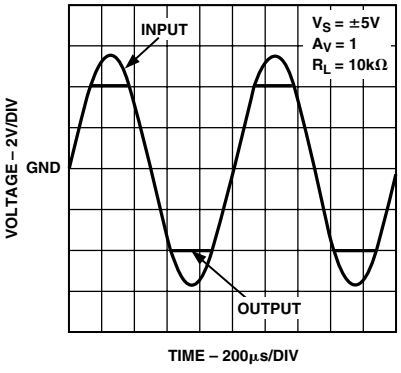
TPC 31. Small Signal Overshoot vs. Load Capacitance



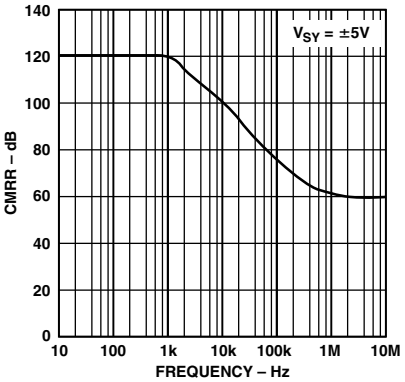
TPC 32. Positive Overvoltage Recovery



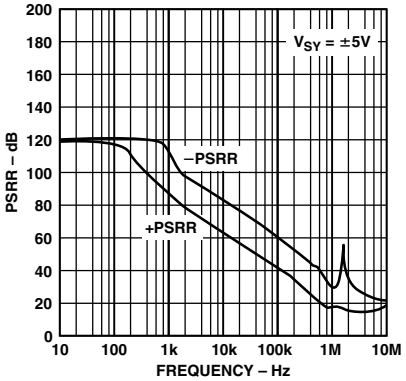
TPC 33. Negative Overvoltage Recovery



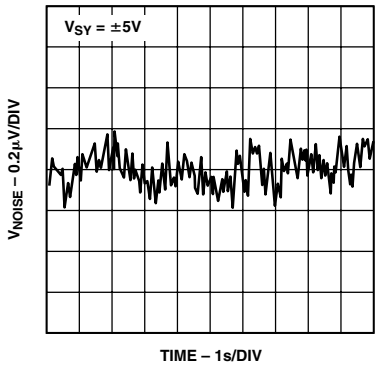
TPC 34. No Phase Reversal



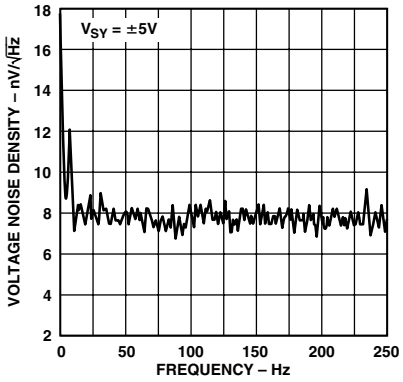
TPC 35. CMRR vs. Frequency



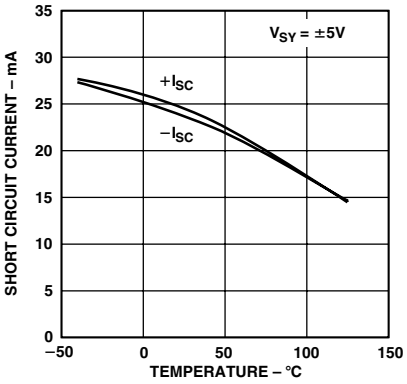
TPC 36. PSRR vs. Frequency



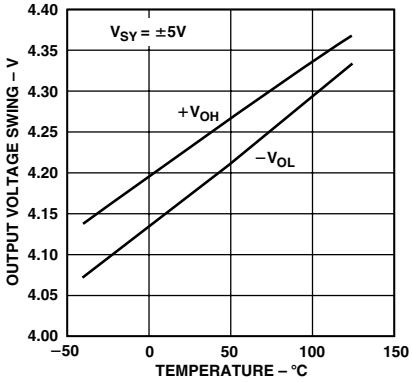
TPC 37. 0.1 Hz to 10 Hz Input Voltage Noise



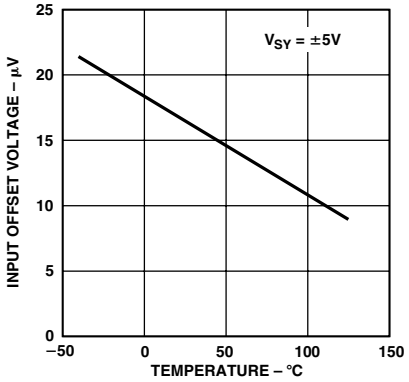
TPC 38. Voltage Noise Density



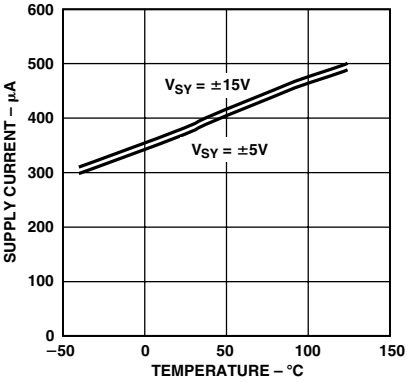
TPC 39. Short Circuit Current vs. Temperature



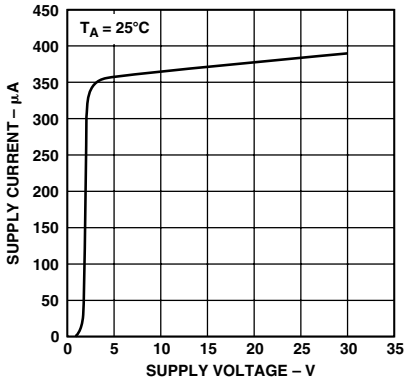
TPC 40. Output Voltage Swing vs. Temperature



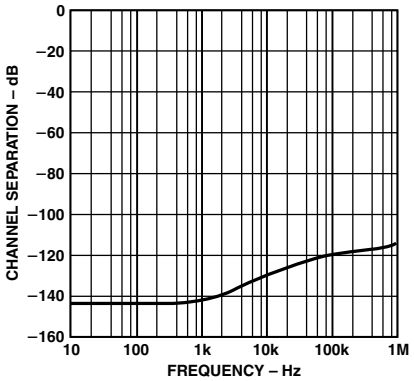
TPC 41. $|V_{OS}|$ vs. Temperature



TPC 42. Supply Current vs. Temperature



TPC 43. Supply Current vs. Supply Voltage



TPC 44. Channel Separation vs. Frequency

FUNCTIONAL DESCRIPTION

OP1177 is the fourth generation of ADI's industry standard OP07 amplifier family. OP1177 is a very high-precision, low-noise operational amplifier with the highly desirable combination of extremely low offset voltage and very low input bias currents. Unlike JFET amplifiers, the low bias and offset currents are relatively insensitive to ambient temperatures, even up to 125°C.

For the first time, Analog Devices' proprietary process technology and linear design expertise have produced a high-voltage amplifier with superior performance to the OP07, OP77, and OP177 in a tiny MSOP 8-lead package. Despite its small size the OP1177 offers numerous improvements including low wideband noise, very wide input and output voltage range, lower input bias current, and complete freedom from phase inversion.

OP1177 has the widest specified operating temperature range of any similar device in a plastic surface-mount package. This is increasingly important as PC board and overall system sizes continue to shrink, causing internal system temperatures to rise. Power consumption is reduced by a factor of four from the OP177 while bandwidth and slew rate increase by a factor of two. The low power dissipation and very stable performance versus temperature also act to reduce warm-up drift errors to insignificant levels.

Open-loop gain linearity under heavy loads is superior to competitive parts like OPA277, improving dc accuracy and reducing distortion in circuits with high closed-loop gains. Inputs are internally protected from overvoltage conditions referenced to either supply rail.

Like any high-performance amplifier, maximum performance is achieved by following appropriate circuit and PC board guidelines. The following sections provide practical advice on getting the most out of the OP1177 under a variety of application conditions.

Total Noise Including Source Resistors

The low input current noise and input bias current of the OP1177 make it useful for circuits with substantial input source resistance. Input offset voltage increases by less than 1 μV max per 500 Ω of source resistance.

The total noise density of the OP1177 is:

$$e_{n,\,TOTAL} = \sqrt{e_n^{\,2} + \left(i_n R_S\right)^2 + 4kTR_S}$$

Where, e_n is the input voltage noise density
i_n is the input current noise density
R_S is the source resistance at the noninverting terminal
k is Boltzman's constant (1.38×10^{-23} J/K)
T is the ambient temperature in Kelvin (T = 273 + °C)

For R_S < 3.9 kΩ, e_n dominates and

$$e_{n,\,TOTAL} \approx e_n$$

For 3.9 kΩ < R_S < 412 kΩ, voltage noise of the amplifier, current noise of the amplifier translated through the source resistor, and thermal noise from the source resistor all contribute to the total noise.

For R_S > 412 kΩ, the current noise dominates and

$$e_{n,\,TOTAL} \approx i_n R_S$$

The total equivalent rms noise over a specific bandwidth is expressed as:

$$E_n = \left(e_{n,\,TOTAL}\right)\sqrt{BW}$$

Where BW is the bandwidth in Hertz.

NOTE: The above analysis is valid for frequencies larger than 50 Hz. When considering lower frequencies, flicker noise (also known as 1/f noise) must be taken into account.

For a reference on noise calculations refer to Bandpass KRC or Sallen-Key Filter section.

Gain Linearity

Gain linearity reduces errors in closed-loop configurations. The straighter the gain curve, the lower the maximum error over the input signal range will be. This is especially true for circuits with high closed-loop gains.

The OP1177 has excellent gain linearity even with heavy loads, shown in Figure 1. Compare its performance to the OPA277, shown in Figure 2. Both devices were measured under identical conditions with R_L = 2 kΩ. The OP2177 (dual) has virtually no distortion at lower voltages. It was compared to the OPA277 at several supply voltages and various loads. Its performance exceeded that of its counterpart by far.

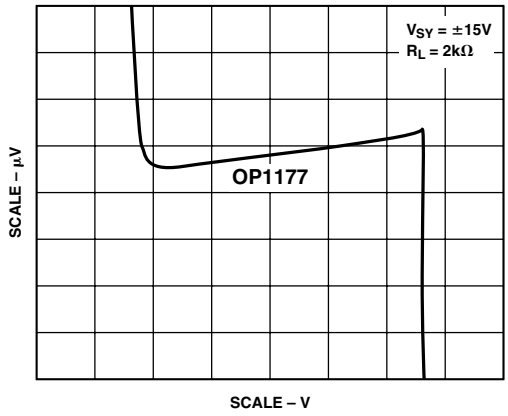


Figure 1. Gain Linearity

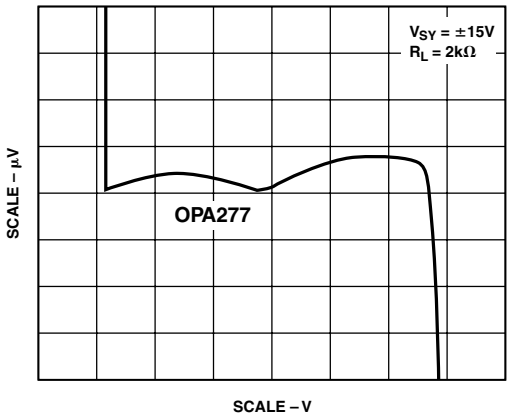


Figure 2. Gain Linearity

Input Overvoltage Protection

When their input voltage exceeds the positive or negative supply voltage, most amplifiers require external resistors to protect them from damage.

The OP1177 has internal protective circuitry that allows voltages as high as 2.5 V beyond the supplies to be applied at the input of either terminal without any harmful effects.

Use an additional resistor in series with the inputs if the voltage will exceed the supplies by more than 2.5 V. The value of the resistor can be determined from the formula:

$$\frac{(V_{IN} - V_S)}{R_S + 500\ \Omega} \leq 5\ mA$$

With the OP1177's low input offset current of <1 nA max, placing a 5 kΩ resistor in series with both inputs adds less than 5 μV to input offset voltage and has a negligible impact on the overall noise performance of the circuit.

5 kΩ will protect the inputs to more than 27 V beyond either supply. Refer to the THD + N section for additional information on noise versus source resistance.

Output Phase Reversal

Phase reversal is defined as a change of polarity in the amplifier transfer function. Many operational amplifiers exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances this can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The OP1177 is immune to phase reversal problems even at input voltages beyond the supplies.

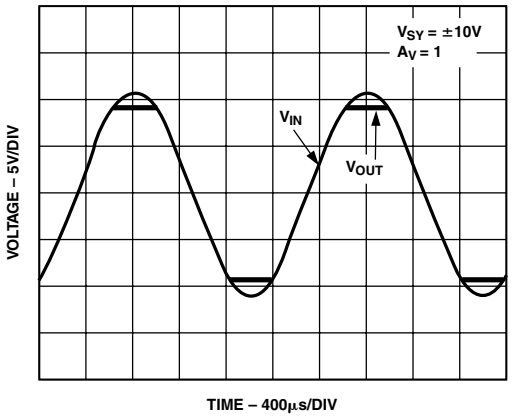


Figure 3. No Phase Reversal

Settling Time

Settling time is defined as the time it takes an amplifier output to reach and remain within a percentage of its final value after application of an input pulse. It is especially important in measurement and control circuits where amplifiers buffer A/D inputs or DAC outputs.

To minimize settling time in amplifier circuits, use proper bypassing of power supplies and an appropriate choice of circuit components. Resistors should be metal film types as these have less stray capacitance and inductance than their wire-wound counterparts. Capacitors should be polystyrene or polycarbonate types to minimize dielectric absorption.

The leads from the power supply should be kept as short as possible to minimize capacitance and inductance. The OP1177 has a settling time of about 45 μs to 0.01% (1 mV) with a 10 V step applied to the input in a noninverting unity gain.

Overload Recovery Time

Overload recovery is defined as the time it takes the output voltage of an amplifier to recover from a saturated condition to its linear response region. A common example is where the output voltage demanded by the circuit's transfer function lies beyond the maximum output voltage capability of the amplifier. A 10 V input applied to an amplifier in a closed-loop gain of 2 will demand an output voltage of 20 V. This is beyond the output voltage range of the OP1177 when operating at ±15 V supplies and will force the output into saturation.

Recovery time is important in many applications, particularly where the op amp must amplify small signals in the presence of large transient voltages.

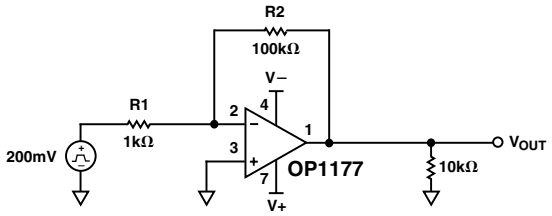


Figure 4. Test Circuit for Overload Recovery Time

TPC 12 shows the positive overload recovery time of the OP1177. The output recovers in less than 4 μs after being overdriven by more than 100%.

The negative overload recovery of the OP1177 is 1.4 μs as seen in TPC 13.

THD + Noise

The OP1177 has very low total harmonic distortion. This indicates excellent gain linearity and makes the OP1177 a great choice for high closed-loop gain precision circuits.

Figure 5 shows that the OP1177 has approximately 0.00025% distortion in unity gain, the worst-case configuration for distortion.

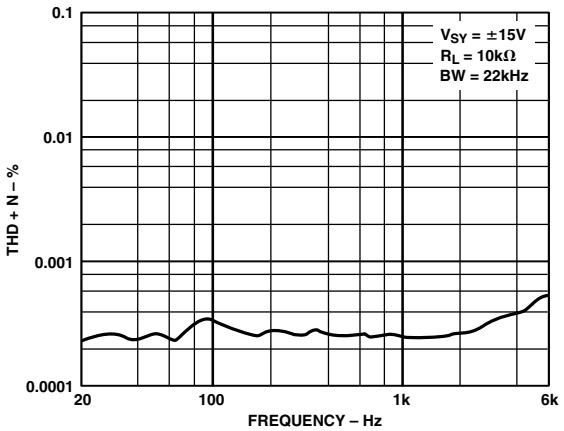


Figure 5. THD + N vs. Frequency

Capacitive Load Drive

OP1177 is inherently stable at all gains and capable of driving large capacitive loads without oscillation. With no external compensation, the OP1177 will safely drive capacitive loads up to 1000 pF in any configuration. As with virtually any amplifier, driving larger capacitive loads in unity gain requires additional circuitry to assure stability.

In this case, a "snubber network" is used to prevent oscillation and reduce the amount of overshoot. A significant advantage of this method is that it does not reduce the output swing because the resistor R_S is not inside the feedback loop.

Figure 6 is a scope photograph of the output of the OP1177 in response to a 400 mV pulse. The load capacitance is 2 nF. The circuit is configured in positive unity gain, the worst-case condition for stability.

Placing an R-C network, as shown in Figure 8, parallel to the load capacitance C_L will allow the amplifier to drive higher values of C_L without causing oscillation or excessive overshoot.

There is no ringing and overshoot is reduced from 27% to 5% using the snubber network.

Optimum values for R_S and C_S are tabulated in Table I for several capacitive loads up to 200 nF. Values for other capacitive loads can be determined experimentally.

Table I. Optimum Values for Capacitive Loads

C_L (nF)	R_S (Ω)	C_S
10	20	0.33 µF
50	30	6.8 nF
200	200	0.47 µF

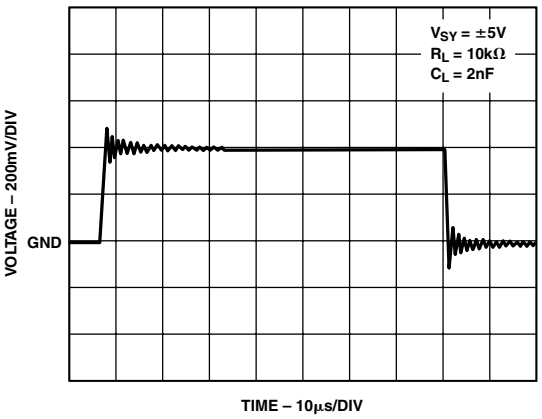


Figure 6. Capacitive Load Drive without Snubber

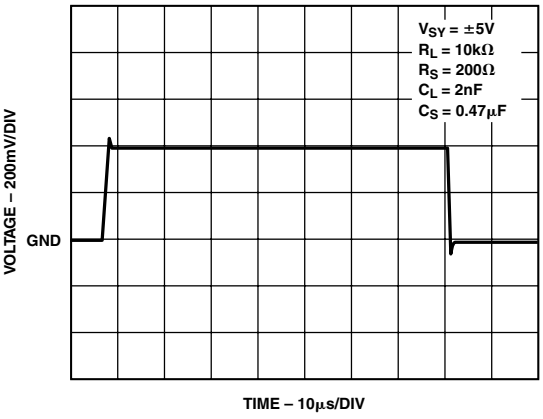


Figure 7. Capacitive Load Drive with Snubber

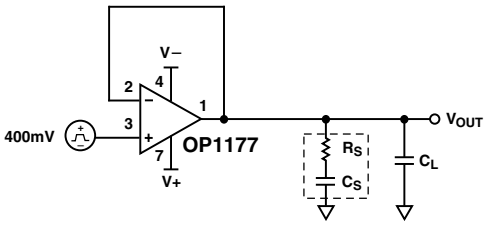


Figure 8. Snubber Network Configuration

CAUTION: The snubber technique cannot recover the loss of bandwidth induced by large capacitive loads.

Stray Input Capacitance Compensation

The effective input capacitance in an op amp circuit, C_t, consists of three components. These are: the internal differential capacitance between the input terminals, the internal common mode capacitance of each input to ground, and the external capacitance including parasitic capacitance. In the circuit of Figure 9, the closed-loop gain increases as the signal frequency increases.

The transfer function of the circuit is:

$$1+\frac{R2}{R1}\left(1+sC_tR1\right)$$

indicating a zero at:

$$s=\frac{R2+R1}{R2R1C_t}=\frac{1}{2\pi\left(R1//R2\right)C_t}$$

Depending on the value of $R1$ and $R2$, the cutoff frequency of the closed-loop gain may be well below the crossover frequency. In this case, the phase margin, Φ_m, can be severely degraded resulting in excessive ringing or even oscillation.

A simple way to overcome this problem is to insert a capacitor in the feedback path as shown in Figure 10.

The resulting pole can be positioned to adjust the phase margin.

Setting $C_f = (R1/R2)C_t$, achieves a phase margin of 90°.

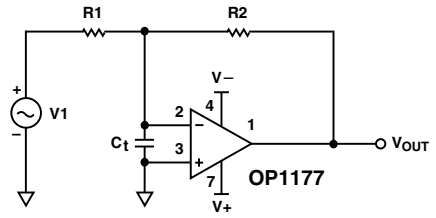


Figure 9. Stray Input Capacitance

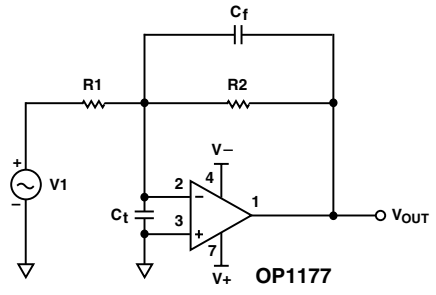


Figure 10. Compensation Using Feedback Capacitor

Reducing Electromagnetic Interference
A number of methods can be utilized to reduce the effects of EMI on amplifier circuits.

In one method, stray signals on either input are coupled to the opposite input of the amplifier. The result is that the signal is rejected according to the amplifier's CMRR.

This is usually achieved by inserting a capacitor between the inputs of the amplifier as shown in Figure 11. However, this method may also cause instability depending on the value of capacitance.

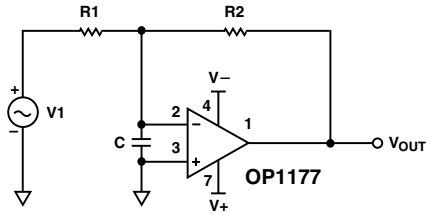


Figure 11. EMI Reduction

Placing a resistor in series with the capacitor (Figure 12) increases the dc loop gain and reduces the output error. Positioning the breakpoint (introduced by R-C) below the secondary pole of the op amp improves the phase margin and hence stability.

R can be chosen independently of C for a specific phase margin according to the formula

$$R = \frac{R2}{ajf_2} - \left(1 + \frac{R2}{R1}\right)$$

where a is the open-loop gain of the amplifier and f_2 is the frequency at which the phase of a = Φ_m – 180°.

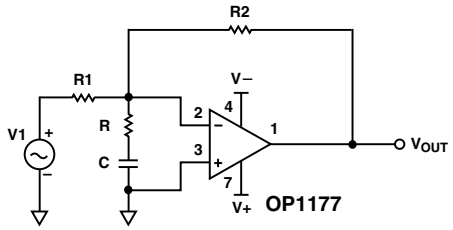


Figure 12. Compensation Using Input RC Network

Proper Board Layout
The OP1177 is a high-precision device. In order to ensure optimum performance at the PC board level, care must be taken in the design of the board layout.

To avoid leakage currents, the surface of the board should be kept clean and free of moisture. Coating the surface creates a barrier to moisture accumulation and helps reduce parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies will minimize power supply disturbances due to output current variation, such as when driving an ac signal into a heavy load. Bypass capacitors should be connected as closely as possible to the device supply pins. Stray capacitances are a concern at the output and the inputs of the amplifier. It is recommended that signal traces be kept at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PC board can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, resistors should be oriented so heat sources warm both ends equally. Input signal paths should contain matching numbers and types of components where possible in order to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Matching components should be located in close proximity and should be oriented in the same manner. Leads should be of equal length so that thermal conduction is in equilibrium. Heat sources on the PC board should be kept as far away from amplifier input circuitry as practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and also helps to maintain a constant temperature across the circuit board.

Difference Amplifiers
Difference amplifiers are used in high-accuracy circuits to improve the common-mode rejection ratio (CMRR).

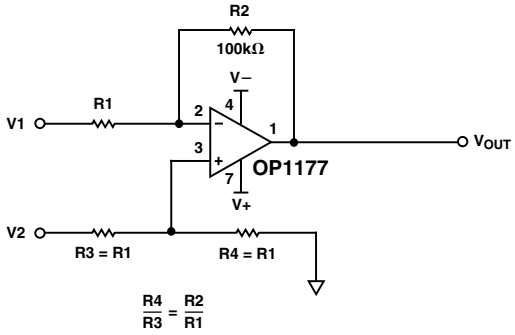


Figure 13. Difference Amplifier

In the single amplifier instrumentation amplifier (circuit of Figure 13), where:

$$\frac{R4}{R3} = \frac{R2}{R1}$$

$$V_O = \frac{R2}{R1}(V_2 - V_1)$$

a mismatch between the ratio $R2/R1$ and $R4/R3$ will cause the common-mode rejection ratio to be reduced. To better understand this effect, consider the following:

By definition:

$$CMRR = \frac{A_{DM}}{A_{CM}}$$

where A_{DM} is the differential gain and A_{CM} is the common-mode gain.

$$A_{DM} = \frac{V_O}{V_{DIFF}} \text{ and } A_{CM} = \frac{V_O}{V_{CM}}$$

$$V_{DIFF} = V_1 - V_2 \text{ and } V_{CM} = \frac{1}{2}(V_1 + V_2)$$

In order for this circuit to act as a difference amplifier, its output must be proportional to the differential input signal.

From Figure 13,

$$V_O = -\left(\frac{R2}{R1}\right)V_1 + \left[\frac{\left(1+\frac{R2}{R1}\right)}{\left(1+\frac{R3}{R4}\right)}\right]V_2$$

Arranging terms and combining the equations above yields:

$$CMRR = \frac{R4R1 + R3R2 + 2R4R2}{2R4R1 - 2R2R3} \quad (1)$$

The sensitivity of CMRR with respect to the $R1$ is obtained by taking the derivative of CMRR, in Equation 1, with respect to $R1$.

$$\frac{\delta CMRR}{\delta R1} = \frac{\delta}{\delta R1}\left(\frac{R1R4}{2R1R4 - 2R2R3} + \frac{2R2R4 + R2R3}{2R1R4 - 2R2R3}\right)$$

$$\frac{\delta CMRR}{\delta R1} = \frac{1}{2 - \frac{(2R2R3)}{R1R4}}$$

Assuming that: $R1 \approx R2 \approx R3 \approx R4 \approx R$ and

$R(1 - \delta) < R1, R2, R3, R4 < R(1 + \delta)$.

The worst-case CMRR error arises when:

$R1 = R4 = R(1 + \delta)$ and $R2 = R3 = R(1 - \delta)$. Plugging these values into Equation 1 yields:

$$CMRR_{MIN} \cong \left|\frac{1}{2\delta}\right|$$

where δ is the tolerance of the resistors.

Lower tolerance value resistors result in higher common-mode rejection (up to the CMRR of the op amp).

Using 5% tolerance resistors, the highest CMRR that can be guaranteed is 20 dB. On the other hand, using 0.1% tolerance resistors would result in a common-mode rejection ratio of at least 54 dB (assuming that the op amp CMRR × 54 dB).

With the CMRR of OP1177 at 120 dB minimum, the resistor match will be the limiting factor in most circuits. A trimming resistor can be used to further improve resistor matching and CMRR of the difference amp circuit.

A High-Accuracy Thermocouple Amplifier

A thermocouple consists of two dissimilar metal wires placed in contact. The dissimilar metals produce a voltage

$$V_{TC} = \alpha(T_J - T_R)$$

where T_J is the temperature at the measurement of the hot junction, T_R is the one at the cold junction, and α is the Seebeck coefficient specific to the dissimilar metals used in the thermocouple. V_{TC} is the thermocouple voltage. V_{TC} becomes larger with increasing temperature.

Maximum measurement accuracy requires cold junction compensation of the thermocouple as described below.

To perform the cold junction compensation, apply a copper wire short across the terminating junctions (inside the isothermal block) simulating a 0°C point. Adjust the output voltage to zero using the trimming resistor R5 and then remove the copper wire.

The OP1177 is an ideal amplifier for thermocouple circuits since it has a very low offset voltage, excellent PSSR and CMRR, and low noise at low frequencies.

It can be used to create a thermocouple circuit with great linearity. Resistors R1 and R2 and diode D1 shown in Figure 14 are mounted in an isothermal block.

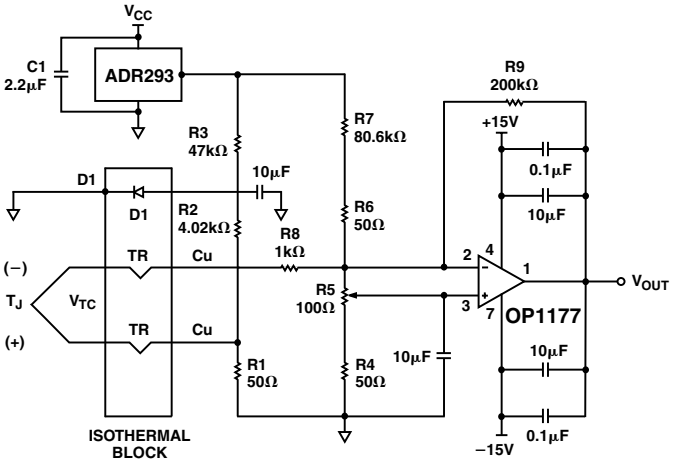


Figure 14. Type K Thermocouple Amplifier Circuit

Low Power Linearized RTD

A common application for a single element varying bridge is an RTD thermometer amplifier as shown in Figure 15. The excitation is delivered to the bridge by a 2.5 V reference applied at the top of the bridge.

RTDs may have thermal resistance as high as 0.5°C to 0.8°C per mW. In order to minimize errors due to resistor drift, the current through each leg of the bridge must be kept low. In this circuit, the amplifier supply current flows through the bridge.

However, at the OP1177 maximum supply current of 600 µA, the RTD dissipates less than 0.1 mW of power even at the highest resistance. Errors due to power dissipation in the bridge are kept under 0.1°C.

Calibration of the bridge can be made at the minimum value of temperature to be measured by adjusting R_P until the output is zero.

To calibrate the output span, set the full-scale and linearity pots to midpoint and apply a 500°C temperature to the sensor or substitute the equivalent 500°C RTD resistance.

Adjust the full-scale pot for a 5 V output. Finally, apply 250°C or the equivalent RTD resistance and adjust the linearity pot for 2.5 V output.

The circuit achieves better than ±0.5°C accuracy after adjustment.

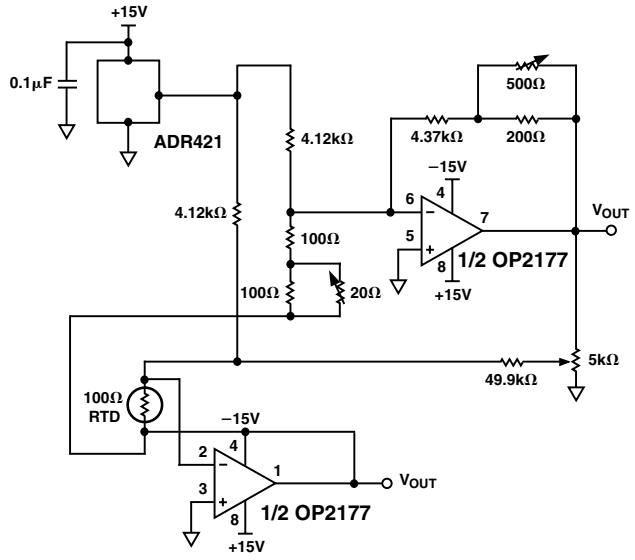


Figure 15. Low Power Linearized RTD Circuit

Single Op Amp Bridge

The low input offset voltage drift of the OP1177 makes it very effective for bridge amplifier circuits used in RTD signal conditioning. It is often more economical to use a single bridge op amp as opposed to an instrumentation amplifier.

In the circuit of Figure 16, the output voltage at the op amp is:

$$V_O = \frac{R2}{R}\left[V_{REF}\left(\frac{\delta}{\frac{R1}{R}+\left(1+\frac{R1}{R2}\right)(1+\delta)}\right)\right]$$

where δ = ΔR/R is the fractional deviation of the RTD resistance with respect to the bridge resistance due to the change in temperature at the RTD.

For $\delta << 1$, the expression above becomes:

$$V_O \cong \left(\frac{R2}{R}\right)V_{REF}\left(\frac{\delta}{1+\frac{R1}{R}+\frac{R1}{R2}}\right) = \left[\left(\frac{R2}{R}\right)\left(1+\frac{R1}{R2}\right)+\left(\frac{R1}{R2}\right)\right]V_{REF}\,\delta$$

With V_{REF} constant, the output voltage is linearly proportional to δ with a gain factor of:

$$V_{REF}\left(\frac{R2}{R}\right)\left[\left(1+\frac{R1}{R2}\right)+\left(\frac{R1}{R2}\right)\right]$$

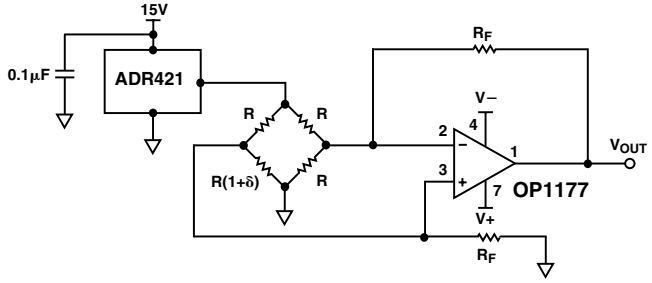


Figure 16. Single Bridge Amplifier

REALIZATION OF ACTIVE FILTERS

Bandpass KRC or Sallen-Key Filter

The low offset voltage and the high CMRR of the OP1177 make it an excellent choice for precision filters such as the KRC filter shown in Figure 17. This filter type offers the capability to tune the gain and the cutoff frequency independently.

Since the common-mode voltage into the amplifier varies with the input signal in the KRC filter circuit, a high CMRR is required to minimize distortion. Also, the low offset voltage of the OP1177 allows a wider dynamic range when the circuit gain is chosen to be high.

The circuit of Figure 17 consists of two stages. The first stage is a simple high-pass filter whose corner frequency f_C is:

$$\frac{1}{2\pi\sqrt{C1C2R1R2}} \quad (2)$$

and whose

$$Q = K\sqrt{\frac{R1}{R2}} \quad (3)$$

where K is the dc gain.

Choosing equal capacitor values minimizes the sensitivity and simplifies Equation 2 to:

$$\frac{1}{2\pi C\sqrt{R1R2}}$$

The value of Q determines the peaking of the gain versus frequency (ringing in transient response). Commonly chosen values for Q are generally near unity.

Setting $Q = \frac{1}{\sqrt{2}}$,

yields minimum gain peaking and minimum ringing.

Determine values for $R1$ and $R2$ by use of Equation 3.

For $Q = \frac{1}{\sqrt{2}}$, R1/R2 = 2 in the circuit example. Pick R1 = 5 kΩ and R2 = 10 kΩ for simplicity.

The second stage is a low-pass filter whose corner frequency can be determined in a similar fashion. For $R3 = R4 = R$.

$$f_C = \frac{1}{2\pi R\sqrt{\frac{C3}{C4}}} \text{ and } Q = \frac{1}{2}\sqrt{\frac{C3}{C4}}$$

Channel Separation

Multiple amplifiers on a single die are often required to reject any signals originating from the inputs or outputs of adjacent channels. OP2177 input and bias circuitry is designed to prevent feedthrough of signals from one amplifier channel to the other. As a result the OP2177 has an impressive channel separation of greater than –120 dB for frequencies up to 100 kHz and greater than –115 dB for signals up to 1 MHz.

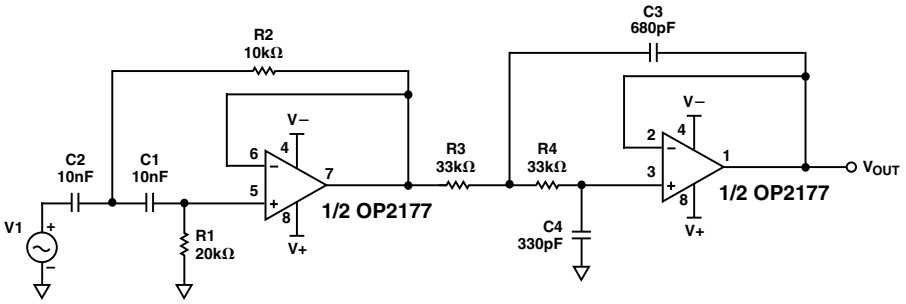


Figure 17. Two-Stage Band-Pass Filter

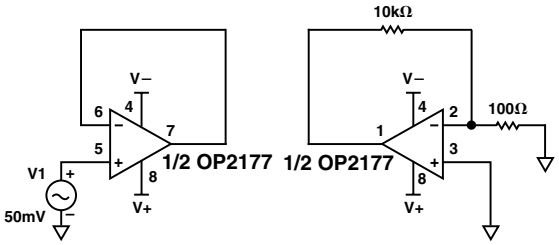


Figure 18. Channel Separation Test Circuit

SPICE Model

The spice macro-model for the OP1177 can be downloaded from the Analog Devices web site at www.analog.com. This model will accurately simulate a number of parameters, both dc and ac.

References on Noise Dynamics and Flicker Noise

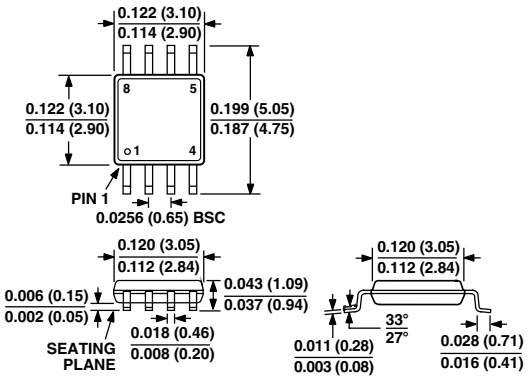
S. Franco, *Design with Operational Amplifiers and Analog Integrated Circuits, McGraw-Hill 1998.*

The Best of Analog Dialogue, from Analog Devices.

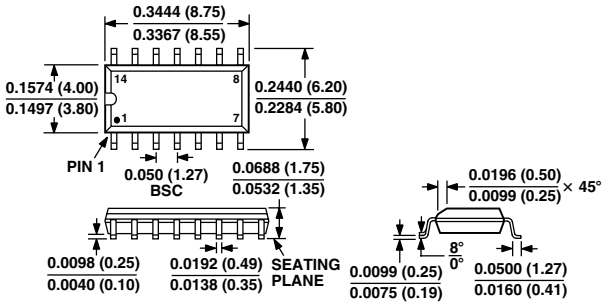
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead MINI_SOIC
(RM-8)



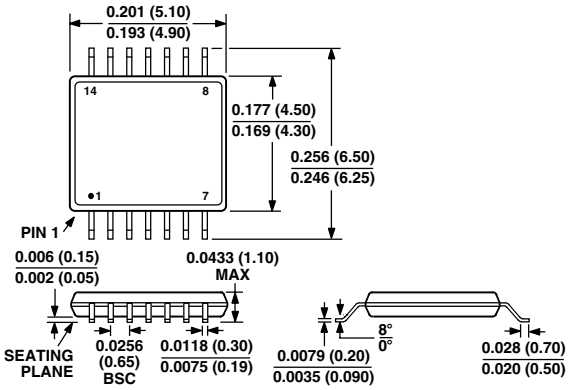
14-Lead SOIC
(R-14)



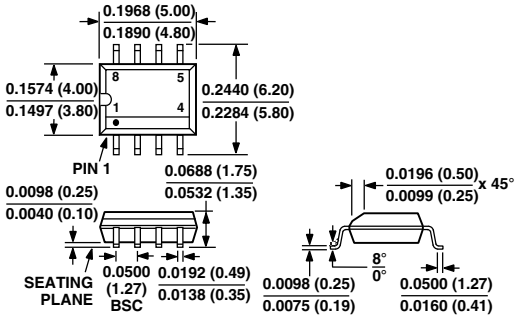
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

14-Lead TSSOP
(RU-14)



8-Lead SOIC
(R-8)



Revision History

Location	Page
Data Sheet changed from REV. A to REV. B.	
Added OP4177	Global
Edits to SPECIFICATIONS	2
Edits to ELECTRICAL CHARACTERISTICS headings	4
Edits to ORDERING GUIDE	4
11/01—Data Sheet changed from REV. 0 to REV. A.	
Edit to FEATURES	1
Edits to TPC 6	5

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