PLL Frequency Synthesizer

ADF4106

FEATURES

6.0 GHz Bandwidth
2.7 V to 3.3 V Power Supply
Separate Charge Pump Supply (V_P) Allows Extended Tuning Voltage in 3 V Systems
Programmable Dual Modulus Prescaler 8/9, 16/17, 32/33, 64/65
Programmable Charge Pump Currents
Programmable Anti-Backlash Pulsewidth
3-Wire Serial Interface
Analog and Digital Lock Detect
Hardware and Software Power-Down Mode

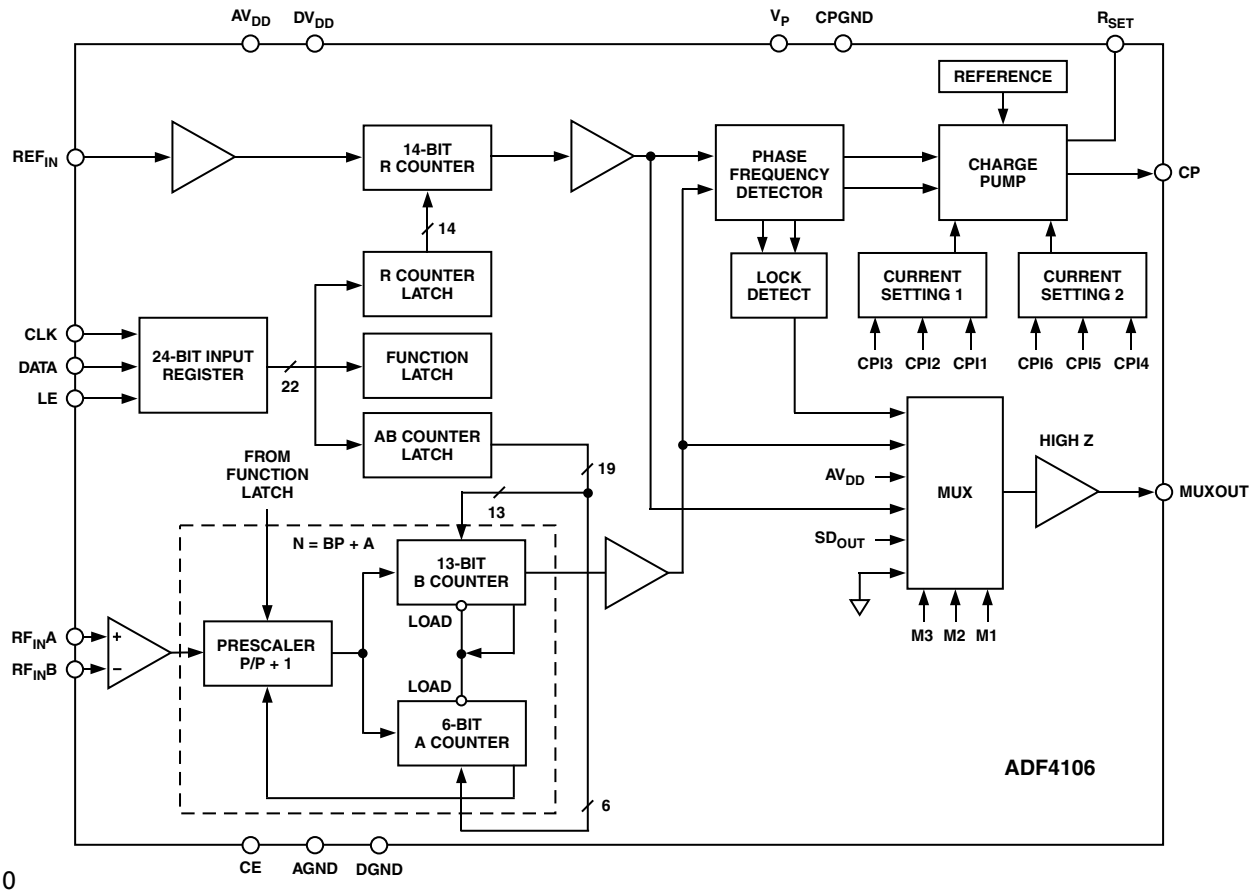
APPLICATIONS

Broadband Wireless Access
Instrumentation
Wireless LANS
Base Stations For Wireless Radio

GENERAL DESCRIPTION

The ADF4106 frequency synthesizer can be used to implement local oscillators in the up-conversion and down-conversion sections of wireless receivers and transmitters. It consists of a low-noise digital PFD (Phase Frequency Detector), a precision charge pump, a programmable reference divider, programmable A and B counters and a dual-modulus prescaler (P/P + 1). The A (6-bit) and B (13-bit) counters, in conjunction with the dual modulus prescaler (P/P + 1), implement an N divider (N = BP + A). In addition, the 14-bit reference counter (R Counter), allows selectable REFIN frequencies at the PFD input. A complete PLL (Phase-Locked Loop) can be implemented if the synthesizer is used with an external loop filter and VCO (Voltage Controlled Oscillator). Its very high bandwidth means that frequency doublers can be eliminated in many high-frequency systems, simplifying system architecture and lowering cost.

FUNCTIONAL BLOCK DIAGRAM



REV. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 **www.analog.com**
Fax: 781/326-8703

ADF4106–SPECIFICATIONS[1] ($AV_{DD} = DV_{DD} = 3$ V ± 10%; $AV_{DD} \le V_P \le 5.5$ V; AGND = DGND = CPGND = 0 V; $R_{SET} = 5.1$ kΩ; dBm referred to 50 Ω; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

Parameter	B Version[1]	BChips[2] (typ)	Unit	Test Conditions/Comments
RF CHARACTERISTICS				See Figure 3 for Input Circuit
RF Input Frequency (RF_{IN})[3]	0.5/6.0	0.5/6.0	GHz min/max	
RF Input Sensitivity	–10/0	–10/0	dBm min/max	
Maximum Allowable Prescaler Output Frequency[4]	300	300	MHz max	
REFIN CHARACTERISTICS				
REFIN Input Frequency	20/250	20/250	MHz min/max	For f < 20 MHz, Use DC-Coupled Square Wave, (0 to V_{DD})
REFIN Input Sensitivity[5]	0.8/AV_{DD}	0.8/AV_{DD}	V p-p min/max	AC-Coupled; When DC-Coupled, 0 to V_{DD} max (CMOS Compatible)
REFIN Input Capacitance	10	10	pF max	
REFIN Input Current	±100	±100	µA max	
PHASE DETECTOR				
Phase Detector Frequency[6]	56	56	MHz max	
CHARGE PUMP				
I_{CP} Sink/Source				Programmable, See Table V
High Value	5	5	mA typ	With $R_{SET} = 5.1$ kΩ
Low Value	625	625	µA typ	
Absolute Accuracy	2.5	2.5	% typ	With $R_{SET} = 5.1$ kΩ
R_{SET} Range	2.7/10	2.7/10	kΩ typ	See Table V
I_{CP} Three-State Leakage Current	1	1	nA typ	
Sink and Source Current Matching	2	2	% typ	$0.5 \text{ V} \le V_{CP} \le V_P - 0.5$ V
I_{CP} vs. V_{CP}	1.5	1.5	% typ	$0.5 \text{ V} \le V_{CP} \le V_P - 0.5$ V
I_{CP} vs. Temperature	2	2	% typ	$V_{CP} = V_P/2$
LOGIC INPUTS				
V_{INH}, Input High Voltage	1.4	1.4	V min	
V_{INL}, Input Low Voltage	0.6	0.6	V max	
I_{INH}/I_{INL}, Input Current	±1	±1	µA max	
C_{IN}, Input Capacitance	10	10	pF max	
LOGIC OUTPUTS				
V_{OH}, Output High Voltage	1.4	1.4	V min	Open Drain Output Chosen 1 kΩ Pull-up to 1.8 V
V_{OH}, Output High Voltage	1.4	1.4	V min	CMOS Output Chosen
I_{OH}	100	100	µA max	
V_{OL}, Output Low Voltage	0.4	0.4	V max	$I_{OL} = 500$ µA
POWER SUPPLIES				
AV_{DD}	2.7/3.3	2.7/3.3	V min/V max	
DV_{DD}	AV_{DD}	AV_{DD}		
V_P	AV_{DD}/5.5	AV_{DD}/5.5	V min/V max	$AV_{DD} \le V_P \le 5.5$ V
I_{DD}[7] ($AI_{DD} + DI_{DD}$)	15	13	mA max	13 mA typ
I_P	0.4	0.4	mA max	$T_A = 25°C$
Power-Down Mode[8] ($AI_{DD} + DI_{DD}$)	10	10	µA typ	

Parameter	B Version[1]	BChips[2] (typ)	Unit	Test Conditions/Comments
NOISE CHARACTERISTICS				
ADF4106 Phase Noise Floor[9]	–174	–174	dBc/Hz typ	@ 25 kHz PFD Frequency
	–166	–166	dBc/Hz typ	@ 200 kHz PFD Frequency
	–159	–159	dBc/Hz typ	@ 1 MHz PFD Frequency
Phase Noise Performance[10]				@ VCO Output
900 MHz Output[11]	–93	–93	dBc/Hz typ	@ 1 kHz Offset and 200 kHz PFD Frequency
5800 MHz Output[12]	–74	–74	dBc/Hz typ	@ 1 kHz Offset and 200 kHz PFD Frequency
5800 MHz Output[13]	–84	–84	dBc/Hz typ	@ 1 kHz Offset and 1 MHz PFD Frequency
Spurious Signals				
900 MHz Output[11]	–90/–92	–90/–92	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD Frequency
5800 MHz Output[12]	–65/–70	–65/–70	dBc typ	@ 200 kHz/400 kHz and 200 kHz PFD Frequency
5800 MHz Output[13]	–70/–75	–70/–75	dBc typ	@ 1 MHz/2 MHz and 1 MHz PFD Frequency

NOTES
[1]Operating temperature range (B Version) is –40°C to +85°C.
[2]The BChip specifications are given as typical values.
[3]Use a square wave for lower frequencies, below the mimimum stated.
[4]This is the maximum operating frequency of the CMOS counters. The prescaler value should be chosen to ensure that the RF input is divided down to a frequency that is less than this value.
[5]$AV_{DD} = DV_{DD} = 3$ V
[6]Guaranteed by design. Sample tested to ensure compliance.
[7]$T_A = 25°C$; $AV_{DD} = DV_{DD} = 3$ V; P = 16; $RF_{IN} = 6.0$ GHz
[8]$T_A = 25°C$; $AV_{DD} = DV_{DD} = 3.3$ V; R = 16383; A = 63; B = 891; P = 32; $RF_{IN} = 6.0$ GHz
[9]The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20logN (where N is the N divider value).
[10]The phase noise is measured with the EVAL-ADF4106EB1 Evaluation Board and the HP8562E Spectrum Analyzer. The spectrum analyzer provides the REFIN for the synthesizer (f_{REFOUT} = 10 MHz @ 0 dBm).
[11]$f_{REFIN} = 10$ MHz; $f_{PFD} = 200$ kHz; Offset Frequency = 1 kHz; $f_{RF} = 900$ MHz; N = 4500; Loop B/W = 20 kHz
[12]$f_{REFIN} = 10$ MHz; $f_{PFD} = 200$ kHz; Offset Frequency = 1 kHz; $f_{RF} = 5800$ MHz; N = 29000; Loop B/W = 20 kHz
[13]$f_{REFIN} = 10$ MHz; $f_{PFD} = 1$ MHz; Offset Frequency = 1 kHz; $f_{RF} = 5800$ MHz; N = 5800; Loop B/W = 100 kHz

Specifications subject to change without notice.

TIMING CHARACTERISTICS

($AV_{DD} = DV_{DD} = 3$ V = 10%; $AV_{DD} \le V_P \le 5.5$ V; AGND = DGND = CPGND = 0 V; $R_{SET} = 5.1$ kΩ; $T_A = T_{MIN}$ to T_{MAX} unless otherwise noted.)

Parameter	Limit at T_{MIN} to T_{MAX} (B Version)	Unit	Test Conditions/Comments
t_1	10	ns min	DATA to CLOCK Setup Time
t_2	10	ns min	DATA to CLOCK Hold Time
t_3	25	ns min	CLOCK High Duration
t_4	25	ns min	CLOCK Low Duration
t_5	10	ns min	CLOCK to LE Setup Time
t_6	20	ns min	LE Pulsewidth

Guaranteed by design but not production tested.

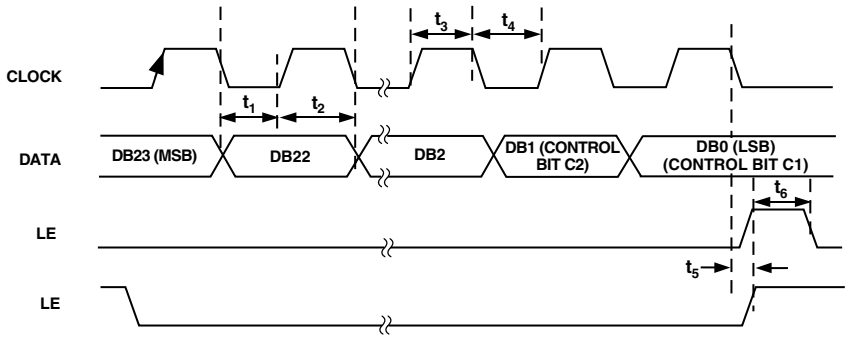


Figure 1. Timing Diagram

ABSOLUTE MAXIMUM RATINGS[1, 2]

(T_A = 25°C unless otherwise noted.)

AV_{DD} to GND[3]	–0.3 V to +3.6 V
AV_{DD} to DV_{DD}	–0.3 V to +0.3 V
V_P to GND	–0.3 V to +5.3 V
V_P to AV_{DD}	–0.3 V to +5.5 V
Digital I/O Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Analog I/O Voltage to GND	–0.3 V to V_P + 0.3 V
REF_{IN}, $RF_{IN}A$, $RF_{IN}B$ to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Maximum Junction Temperature	150°C
TSSOP θ_{JA} Thermal Impedance	150.4°C/W
CSP θ_{JA} Thermal Impedance	122°C/W
Lead Temperature, Soldering	
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

NOTES

[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

[2]This device is a high-performance RF integrated circuit with an ESD rating of <2 kV and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

[3]GND = AGND = DGND = 0 V

ORDERING GUIDE

Model	Temperature Range	Package Option*
ADF4106BRU	–40°C to +85°C	RU-16
ADF4106BCP	–40°C to +85°C	CP-20

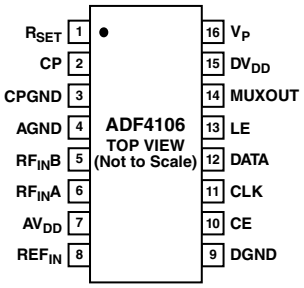
*RU = Thin Shrink Small Outline Package (TSSOP)
CP = Chip Scale Package
Contact the factory for chip availability.
Note that aluminum bond wire should not be used with the ADF4106 die.

CAUTION

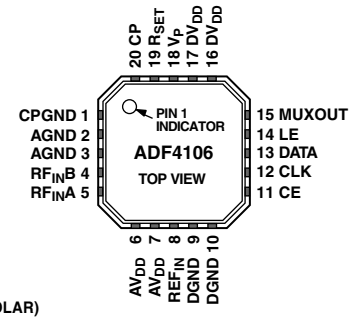
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADF4106 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS

TSSOP



Chip Scale Package



NOTE: TRANSISTOR COUNT 6425 (CMOS), 303 (BIPOLAR)

PIN FUNCTION DESCRIPTIONS

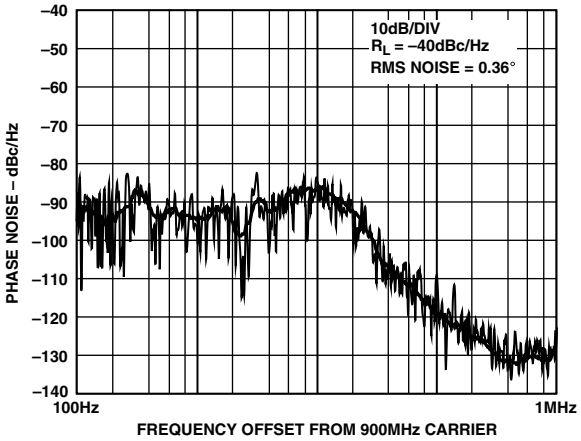
Mnemonic	Function
R_{SET}	Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the R_{SET} pin is 0.6 V. The relationship between I_{CP} and R_{SET} is $$I_{CP\,MAX} = \frac{25.5}{R_{SET}}$$ So, with R_{SET} = 5.1 kΩ, I_{CPMAX} = 5 mA.
CP	Charge Pump Output. When enabled this provides $\pm I_{CP}$ to the external loop filter, which in turn drives the external VCO.
CPGND	Charge Pump Ground. This is the ground return path for the charge pump.
AGND	Analog Ground. This is the ground return path of the prescaler.
$RF_{IN}B$	Complementary Input to the RF Prescaler. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 3.
$RF_{IN}A$	Input to the RF Prescaler. This small signal input is ac coupled to the external VCO.
AV_{DD}	Analog Power Supply. This may range from 2.7 V to 3.3 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. AV_{DD} must be the same value as DV_{DD}.
REF_{IN}	Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100 kΩ. See Figure 2. This input can be driven from a TTL or CMOS crystal oscillator or it can be ac coupled.
DGND	Digital Ground
CE	Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high will power up the device depending on the status of the power-down bit F2.
CLK	Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input.
DATA	Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input.
LE	Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected using the control bits.
MUXOUT	This multiplexer output allows either the Lock Detect, the scaled RF or the scaled Reference Frequency to be accessed externally.
DV_{DD}	Digital Power Supply. This may range from 2.7 V to 3.3 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. DV_{DD} must be the same value as AV_{DD}.
V_P	Charge Pump Power Supply. This should be greater than or equal to V_{DD}. In systems where V_{DD} is 3 V, it can be set to 5 V and used to drive a VCO with a tuning range of up to 5 V.

ADF4106–Typical Performance Characteristics

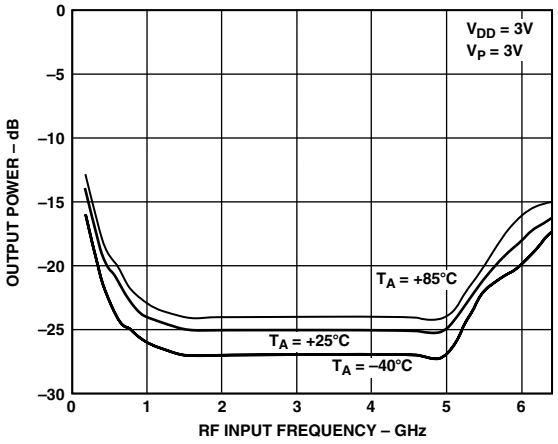
FREQ UNIT – GHz KEYWORD – R
PARAM TYPE – S IMPEDANCE Ω – 50
DATA FORMAT – MA

FREQ	MAGS11	ANGS11	FREQ	MAGS11	ANGS11
0.500	0.89148	–17.2820	3.300	0.42777	–102.748
0.600	0.88133	–20.6919	3.400	0.42859	–107.167
0.700	0.87152	–24.5386	3.500	0.43365	–111.883
0.800	0.85855	–27.3228	3.600	0.43849	–117.548
0.900	0.84911	–31.0698	3.700	0.44475	–123.856
1.000	0.83512	–34.8623	3.800	0.44800	–130.399
1.100	0.82374	–38.5574	3.900	0.45223	–136.744
1.200	0.80871	–41.9093	4.000	0.45555	–142.766
1.300	0.79176	–45.6990	4.100	0.45313	–149.269
1.400	0.77205	–49.4185	4.200	0.45622	–154.884
1.500	0.75696	–52.8898	4.300	0.45555	–159.680
1.600	0.74234	–56.2923	4.400	0.46108	–164.916
1.700	0.72239	–60.2584	4.500	0.45325	–168.452
1.800	0.69419	–63.1446	4.600	0.45054	–173.462
1.900	0.67288	–65.6464	4.700	0.45200	–176.697
2.000	0.66227	–68.0742	4.800	0.45043	178.824
2.100	0.64758	–71.3530	4.900	0.45282	174.947
2.200	0.62454	–75.5658	5.000	0.44287	170.237
2.300	0.59466	–79.6404	5.100	0.44909	166.617
2.400	0.55932	–82.8246	5.200	0.44294	162.786
2.500	0.52256	–85.2795	5.300	0.44558	158.766
2.600	0.48754	–85.6298	5.400	0.45417	153.195
2.700	0.46411	–86.1854	5.500	0.46038	147.721
2.800	0.45776	–86.4997	5.600	0.47128	139.760
2.900	0.44859	–88.8080	5.700	0.47439	132.657
3.000	0.44588	–91.9737	5.800	0.48604	125.782
3.100	0.43810	–95.4087	5.900	0.50637	121.110
3.200	0.43269	–99.1282	6.000	0.52172	115.400

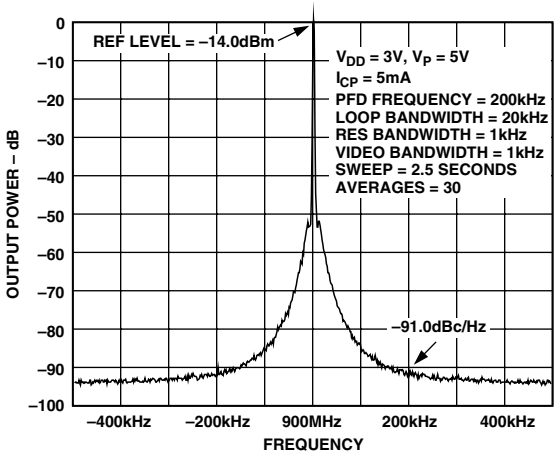
TPC 1. S-Parameter Data for the RF Input



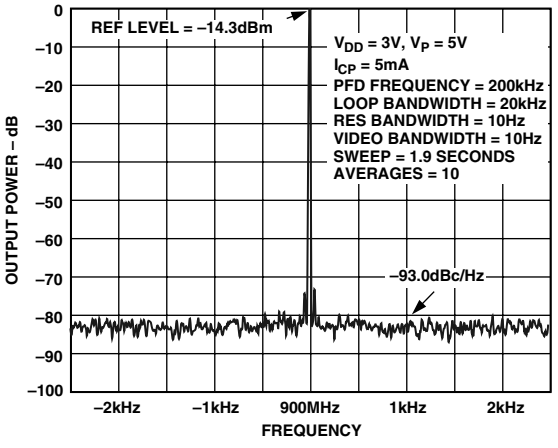
TPC 4. Integrated Phase Noise (900 MHz, 200 kHz, and 20 kHz)



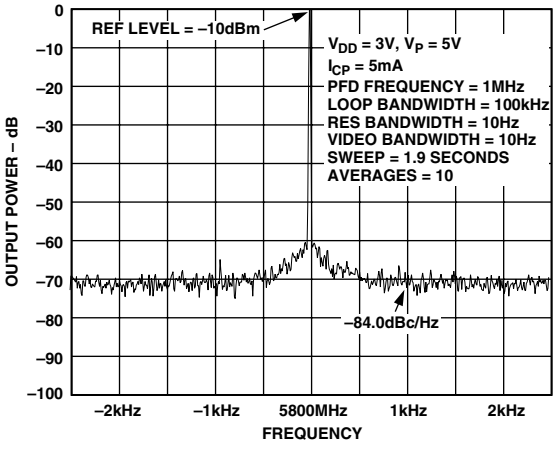
TPC 2. Input Sensitivity



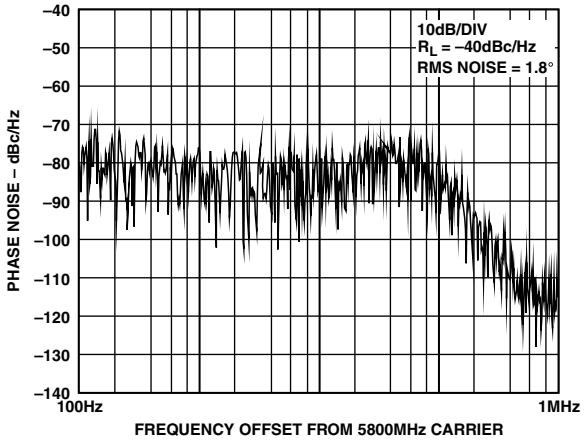
TPC 5. Reference Spurs (900 MHz, 200 kHz, and 20 kHz)



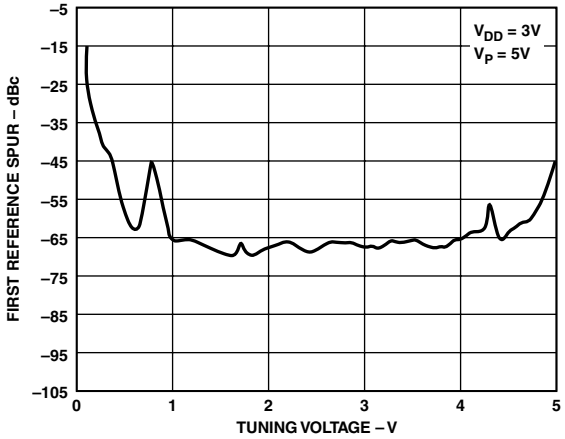
TPC 3. Phase Noise (900 MHz, 200 kHz, and 20 kHz)



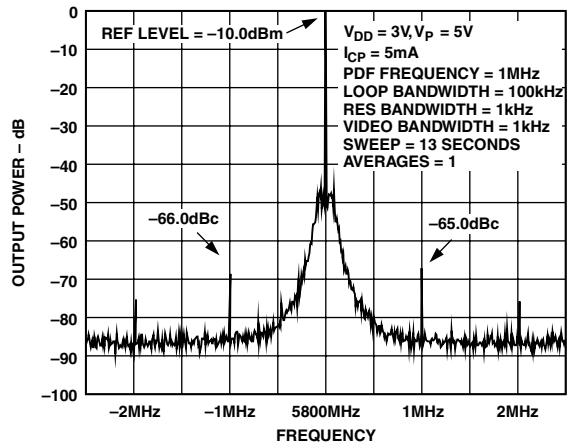
TPC 6. Phase Noise (5.8 GHz, 1 MHz, and 100 kHz)



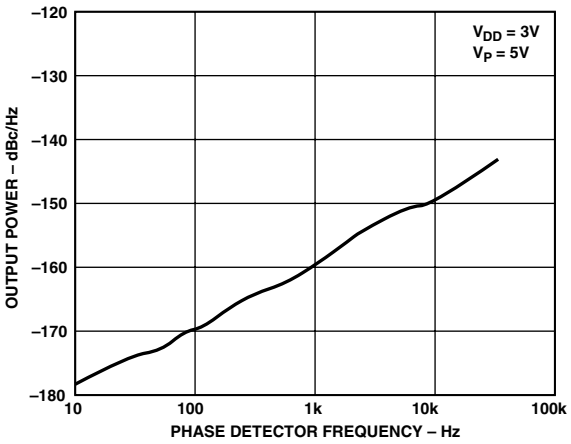
TPC 7. Integrated Phase Noise (5.8 GHz, 1 MHz, and 100 kHz)



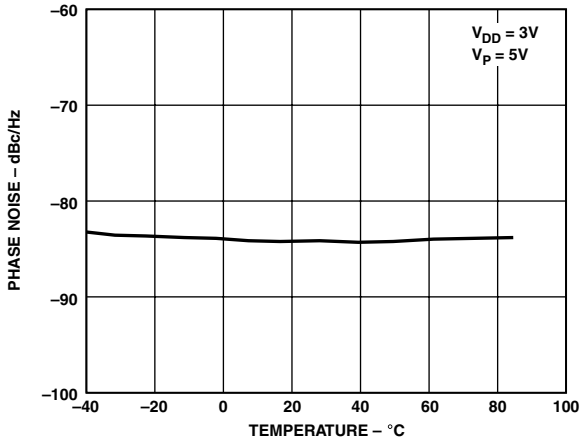
TPC 10. Reference Spurs vs. V_{TUNE} (5.8 GHz, 1 MHz, and 100 kHz)



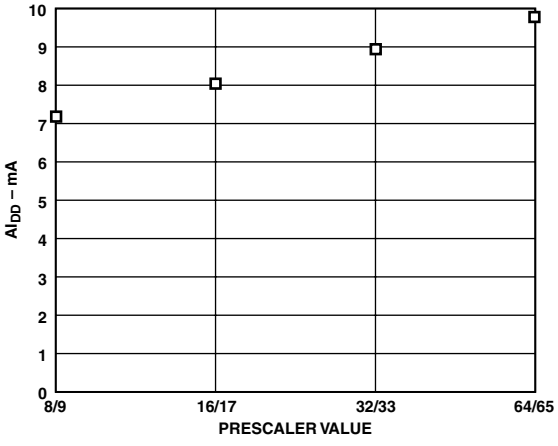
TPC 8. Reference Spurs (5.8 GHz, 1 MHz, and 100 kHz)



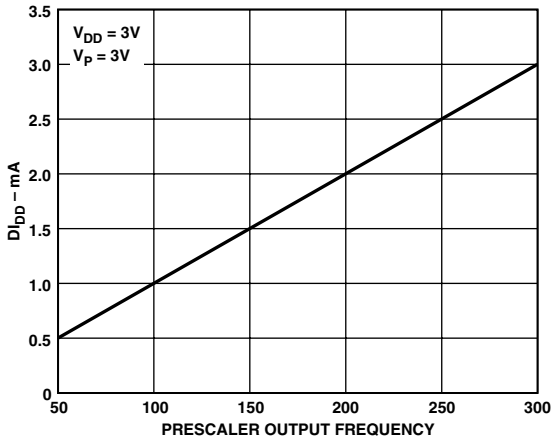
TPC 11. Phase Noise (referred to CP output) vs. PFD Frequency



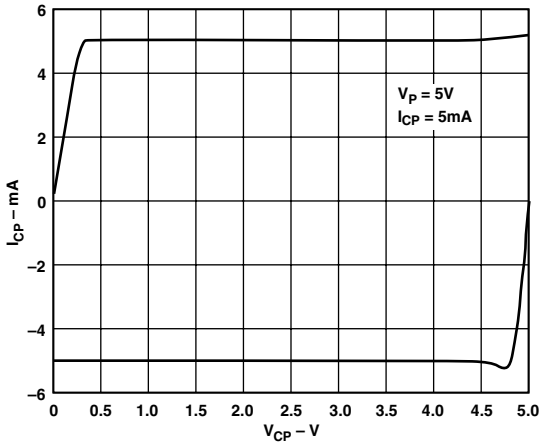
TPC 9. Phase Noise (5.8 GHz, 1 MHz, and 100 kHz) vs. Temperature



TPC 12. AI_{DD} vs. Prescaler Value



TPC 13. DI_{DD} vs. Prescaler Output Frequency



TPC 14. Charge Pump Output Characteristics

CIRCUIT DESCRIPTION

REFERENCE INPUT SECTION

The Reference Input stage is shown in Figure 2. SW1 and SW2 are normally-closed switches. SW3 is normally-open. When Powerdown is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the REF_{IN} pin on power-down.

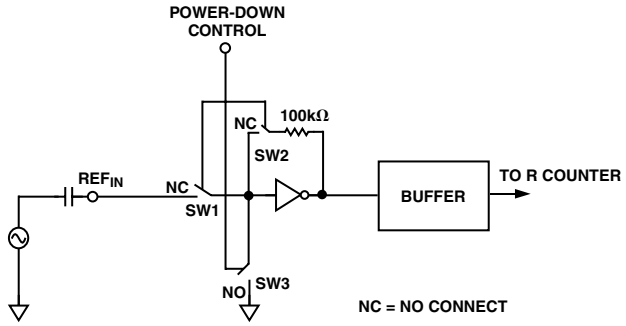


Figure 2. Reference Input Stage

RF INPUT STAGE

The RF input stage is shown in Figure 3. It is followed by a 2-stage limiting amplifier to generate the CML clock levels needed for the prescaler.

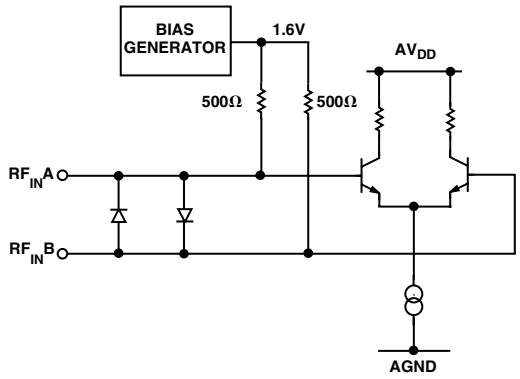


Figure 3. RF Input Stage

PRESCALER (P/P + 1)

The dual modulus prescaler (P/P + 1), along with the A and B counters, enables the large division ratio, N, to be realized (N = BP + A). The dual-modulus prescaler, operating at CML levels, takes the clock from the RF input stage and divides it down to a manageable frequency for the CMOS A and B counters. The prescaler is programmable. It can be set in software to 8/9, 16/17, 32/33 or 64/65. It is based on a synchronous 4/5 core. There is a minimum divide ratio possible for fully contiguous output frequencies. This minimum is determined by P, the prescaler value and is given by: $(P^2 – P)$.

A AND B COUNTERS

The A and B CMOS counters combine with the dual modulus prescaler to allow a wide ranging division ratio in the PLL feedback counter. The counters are specified to work when the prescaler output is 300 MHz or less. Thus, with an RF input frequency of 4.0 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

Pulse Swallow Function

The A and B counters, in conjunction with the dual modulus prescaler make it possible to generate output frequencies which are spaced only by the Reference Frequency divided by R. The equation for the VCO frequency is as follows:

$$f_{VCO} = [(P \times B) + A] \times \frac{f_{REFIN}}{R}$$

f_{VCO} Output Frequency of external voltage controlled oscillator (VCO).

P Preset modulus of dual modulus prescaler (8/9, 16/17, etc.,).

B Preset Divide Ratio of binary 13-bit counter (3 to 8191).

A Preset Divide Ratio of binary 6-bit swallow counter (0 to 63).

f_{REFIN} External reference frequency oscillator.

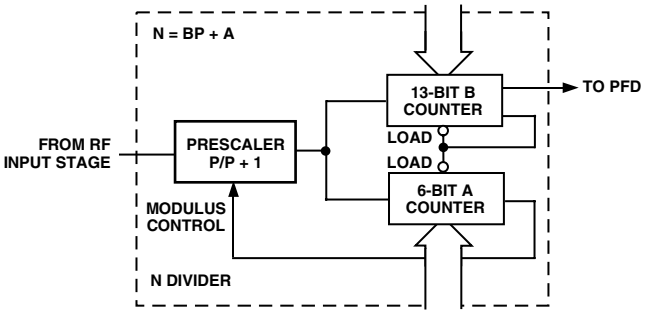


Figure 4. A and B Counters

R COUNTER

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter (N = BP + A) and produces an output proportional to the phase and frequency difference between them. Figure 5 is a simplified schematic. The PFD includes a programmable delay element which controls the width of the anti-backlash pulse. This pulse ensures that there is no deadzone in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the Reference Counter Latch, ABP2 and ABP1 control the width of the pulse. See Table III.

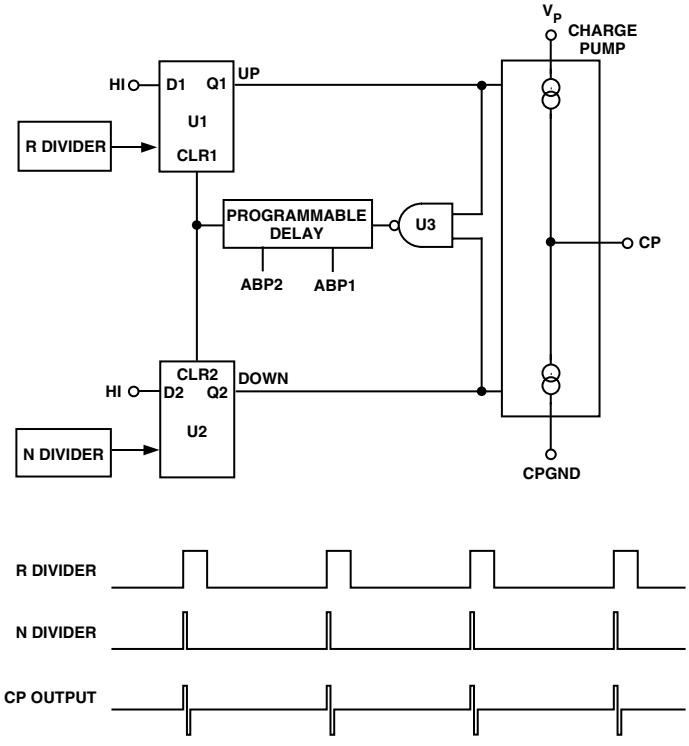


Figure 5. PFD Simplified Schematic and Timing (In Lock)

MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4110 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the Function Latch. Table V shows the full truth table. Figure 6 shows the MUXOUT section in block diagram form.

Lock Detect

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect.

Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive Phase Detector cycles is less than 15 ns. With LDP set to "1," five consecutive cycles of less than 15 ns are required to set the lock detect. It will stay set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle.

The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected this output will be high with narrow low-going pulses.

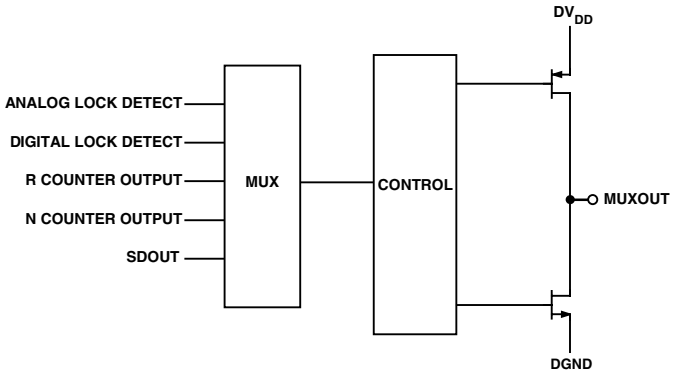


Figure 6. MUXOUT Circuit

INPUT SHIFT REGISTER

The ADF4110 family digital section includes a 24-bit input shift register, a 14-bit R counter and a 19-bit N counter, comprising a 6-bit A counter and a 13-bit B counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table VI. Table I shows a summary of how the latches are programmed.

Table I. C2, C1 Truth Table

Control Bits C2	C1	Data Latch
0	0	R Counter
0	1	N Counter (A and B)
1	0	Function Latch (Including Prescaler)
1	1	Initialization Latch

Table II. Latch Summary

REFERENCE COUNTER LATCH

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER													CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

N COUNTER LATCH

RESERVED		CP GAIN	13-BIT B COUNTER													6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
		G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

FUNCTION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

INITIALIZATION LATCH

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)

Table III. Reference Counter Latch Map

RESERVED			LOCK DETECT PRECISION	TEST MODE BITS		ANTI-BACKLASH WIDTH		14-BIT REFERENCE COUNTER												CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	0	0	LDP	T2	T1	ABP2	ABP1	R14	R13	R12	R11	R10	R9	R8	R7	R6	R5	R4	R3	R2	R1	C2 (0)	C1 (0)

X = DON'T CARE

R14	R13	R12	.....	R3	R2	R1	DIVIDE RATIO
0	0	0	.....	0	0	1	1
0	0	0	.....	0	1	0	2
0	0	0	.....	0	1	1	3
0	0	0	.....	1	0	0	4
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	16380
1	1	1	.....	1	0	1	16381
1	1	1	.....	1	1	0	16382
1	1	1	.....	1	1	1	16383

ABP2	ABP1	ANTIBACKLASH PULSEWIDTH
0	0	2.9ns
0	1	1.3ns
1	0	6.0ns
1	1	2.9ns

TEST MODE BITS SHOULD BE SET TO 00 FOR NORMAL OPERATION

LDP	OPERATION
0	THREE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.
1	FIVE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET.

BOTH OF THESE BITS MUST BE SET TO 0 FOR NORMAL OPERATION

Table IV. AB Counter Latch Map

RESERVED		CP GAIN	13-BIT B COUNTER												6-BIT A COUNTER						CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
X	X	G1	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	A6	A5	A4	A3	A2	A1	C2 (0)	C1 (1)

X = DON'T CARE

A6	A5	.....	A2	A1	A COUNTER DIVIDE RATIO
0	0	.....	0	0	0
0	0	.....	0	1	1
0	0	.....	1	0	2
0	0	.....	1	1	3
.	.	.....	.	.	.
.	.	.....	.	.	.
.	.	.....	.	.	.
1	1	.....	0	0	60
1	1	.....	0	1	61
1	1	.....	1	0	62
1	1	.....	1	1	63

B13	B12	B11		B3	B2	B1	B COUNTER DIVIDE RATIO
0	0	0	.....	0	0	0	NOT ALLOWED
0	0	0	.....	0	0	1	NOT ALLOWED
0	0	0	.....	0	1	0	NOT ALLOWED
0	0	0	.....	1	1	1	3
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
.	.	.	.....	.	.	.	.
1	1	1	.....	1	0	0	8188
1	1	1	.....	1	0	1	8189
1	1	1	.....	1	1	0	8190
1	1	1	.....	1	1	1	8191

F4 (FUNCTION LATCH) FASTLOCK ENABLE	CP GAIN	OPERATION
0	0	CHARGE PUMP CURRENT SETTING
	1	IS PERMANENTLY USED
0	1	CHARGE PUMP CURRENT SETTING
	2	IS PERMANENTLY USED
1	0	CHARGE PUMP CURRENT SETTING
	1	IS USED
1	1	CHARGE PUMP CURRENT IS SWITCHED TO SETTING 2. THE TIME SPENT IN SETTING 2 IS DEPENDENT ON WHICH FASTLOCK MODE IS USED. SEE FUNCTION LATCH DESCRIPTION

N = BP + A, P IS PRESCALER VALUE SET IN THE FUNCTION LATCH. B MUST BE GREATER THAN OR EQUAL TO A. FOR CONTINUOUSLY ADJACENT VALUES OF ($N \times F_{REF}$), AT THE OUTPUT, N_{MIN} IS ($P^2 - P$)

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.

Table V. Function Latch Map

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (0)

F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN LOCK DETECT
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

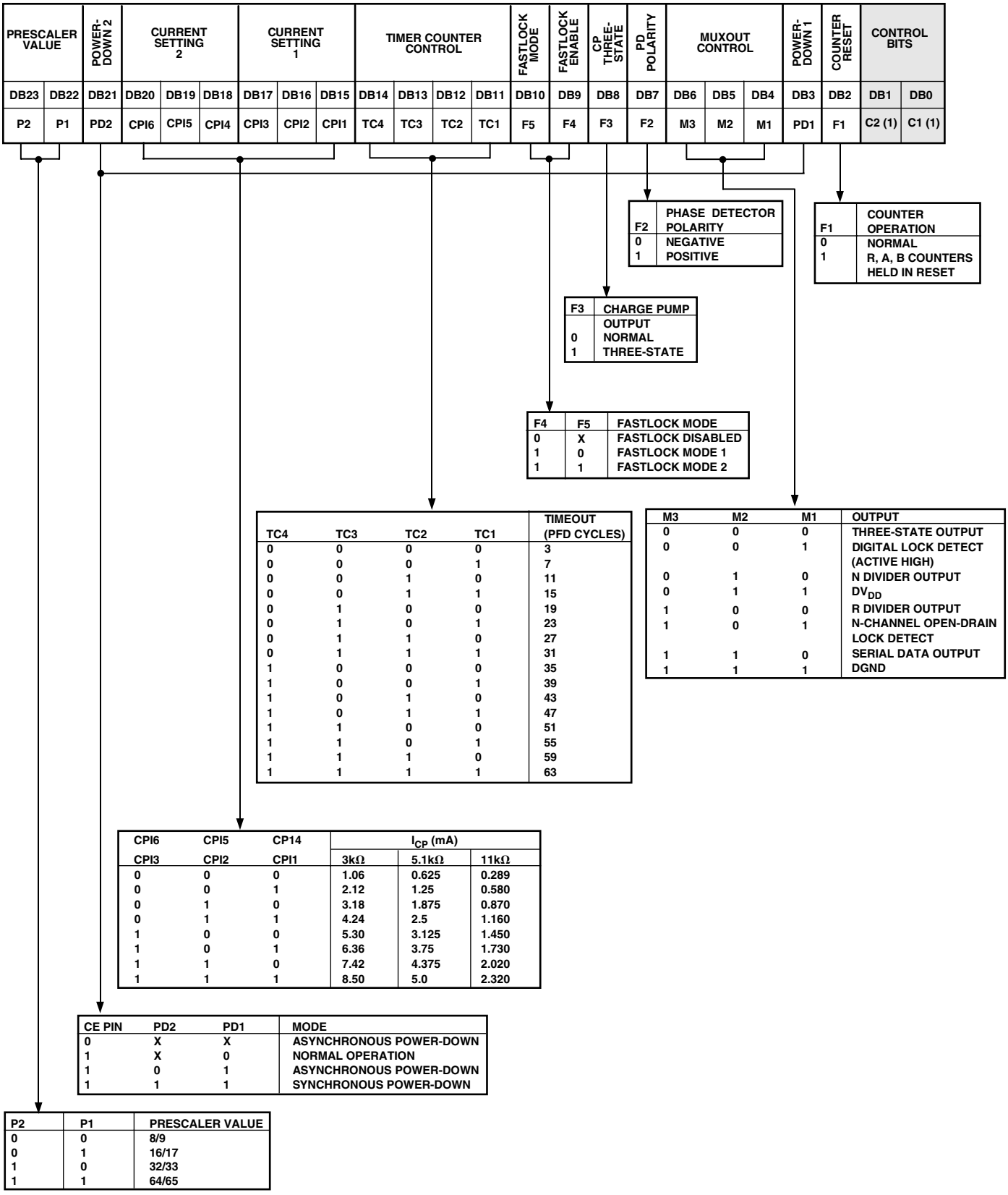
CPI6	CPI5	CP14	I_{CP} (mA)		
CPI3	CPI2	CPI1	3kΩ	5.1kΩ	11kΩ
0	0	0	1.06	0.625	0.289
0	0	1	2.12	1.25	0.580
0	1	0	3.18	1.875	0.870
0	1	1	4.24	2.5	1.160
1	0	0	5.30	3.125	1.450
1	0	1	6.36	3.75	1.730
1	1	0	7.42	4.375	2.020
1	1	1	8.50	5.0	2.320

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

Table VI. Initialization Latch Map

PRESCALER VALUE		POWER-DOWN 2	CURRENT SETTING 2			CURRENT SETTING 1			TIMER COUNTER CONTROL				FASTLOCK MODE	FASTLOCK ENABLE	CP THREE-STATE	PD POLARITY	MUXOUT CONTROL			POWER-DOWN 1	COUNTER RESET	CONTROL BITS	
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
P2	P1	PD2	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	TC4	TC3	TC2	TC1	F5	F4	F3	F2	M3	M2	M1	PD1	F1	C2 (1)	C1 (1)



F2	PHASE DETECTOR POLARITY
0	NEGATIVE
1	POSITIVE

F1	COUNTER OPERATION
0	NORMAL
1	R, A, B COUNTERS HELD IN RESET

F3	CHARGE PUMP OUTPUT
0	NORMAL
1	THREE-STATE

F4	F5	FASTLOCK MODE
0	X	FASTLOCK DISABLED
1	0	FASTLOCK MODE 1
1	1	FASTLOCK MODE 2

TC4	TC3	TC2	TC1	TIMEOUT (PFD CYCLES)
0	0	0	0	3
0	0	0	1	7
0	0	1	0	11
0	0	1	1	15
0	1	0	0	19
0	1	0	1	23
0	1	1	0	27
0	1	1	1	31
1	0	0	0	35
1	0	0	1	39
1	0	1	0	43
1	0	1	1	47
1	1	0	0	51
1	1	0	1	55
1	1	1	0	59
1	1	1	1	63

M3	M2	M1	OUTPUT
0	0	0	THREE-STATE OUTPUT
0	0	1	DIGITAL LOCK DETECT (ACTIVE HIGH)
0	1	0	N DIVIDER OUTPUT
0	1	1	DV_{DD}
1	0	0	R DIVIDER OUTPUT
1	0	1	N-CHANNEL OPEN-DRAIN LOCK DETECT
1	1	0	SERIAL DATA OUTPUT
1	1	1	DGND

CPI6	CPI5	CP14	I_{CP} (mA)		
CPI3	CPI2	CPI1	3kΩ	5.1kΩ	11kΩ
0	0	0	1.06	0.625	0.289
0	0	1	2.12	1.25	0.580
0	1	0	3.18	1.875	0.870
0	1	1	4.24	2.5	1.160
1	0	0	5.30	3.125	1.450
1	0	1	6.36	3.75	1.730
1	1	0	7.42	4.375	2.020
1	1	1	8.50	5.0	2.320

CE PIN	PD2	PD1	MODE
0	X	X	ASYNCHRONOUS POWER-DOWN
1	X	0	NORMAL OPERATION
1	0	1	ASYNCHRONOUS POWER-DOWN
1	1	1	SYNCHRONOUS POWER-DOWN

P2	P1	PRESCALER VALUE
0	0	8/9
0	1	16/17
1	0	32/33
1	1	64/65

THE FUNCTION LATCH

With C2, C1 set to 1,0, the on-chip function latch will be programmed. Table V shows the input data format for programming the Function Latch.

Counter Reset

DB2 (F1) is the counter reset bit. When this is "1," the R counter and the A,B counters are reset. For normal operation this bit should be "0." *Upon powering up, the F1 bit needs to be disabled (set to "0"). The N counter then resumes counting in "close" alignment with the R counter. (The maximum error is one prescaler cycle).*

Power-Down

DB3 (PD1) and DB21 (PD2) on the ADF4110 Family, provide programmable power-down modes. They are enabled by the CE pin. When the CE pin is low, the device is immediately disabled regardless of the states of PD2, PD1. In the programmed asynchronous power-down, the device powers down immediately after latching a "1" into bit PD1, with the condition that PD2 has been loaded with a "0." In the programmed synchronous power-down, the device power down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a "1" into bit PD1 (on condition that a "1" has also been loaded to PD2), then the device will go into power-down on the occurrence of the next charge pump event. When a power down is activated (either synchronous or asynchronous mode including CE-pin-activated power down), the following events occur:

All active dc current paths are removed.
The R, N, and timeout counters are forced to their load state conditions.
The charge pump is forced into three-state mode.
The digital clock detect circuitry is reset.
The RF_{IN} input is debiased.
The reference input buffer circuitry is disabled.
The input register remains active and capable of loading and latching data.

MUXOUT Control

The on-chip multiplexer is controlled by M3, M2, M1 on the ADF4110 Family. Table V shows the truth table.

Fastlock Enable Bit

DB9 of the Function Latch is the Fastlock Enable Bit. Only when this is "1" is Fastlock enabled.

Fastlock Mode Bit

DB10 of the Function Latch is the Fastlock Mode bit. When Fastlock is enabled, this bit determines which Fastlock Mode is used. If the Fastlock Mode bit is "0," Fastlock Mode 1 is selected and if the Fastlock Mode bit is "1," Fastlock Mode 2 is selected.

Fastlock Mode 1

The charge pump current is switched to the contents of Current Setting 2. The device enters Fastlock by having a "1" written to the CP Gain bit in the AB counter latch. The device exits Fastlock by having a "0" written to the CP Gain bit in the AB counter latch.

Fastlock Mode 2

The charge pump current is switched to the contents of Current Setting 2. The device enters Fastlock by having a "1" written to the CP Gain bit in the AB counter latch. The device exits Fastlock under the control of the Timer Counter. After the timeout period determined by the value in TC4–TC1, the CP Gain bit in the AB counter latch is automatically reset to "0" and the device reverts to normal mode instead of Fastlock. See Table V for the timeout periods.

Timer Counter Control

The user has the option of programming two charge pump currents. The intent is that the Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change (i.e., when a new output frequency is programmed). The normal sequence of events is as follows:

Users initially decide what the preferred charge pump currents are will be. For example, they may choose 2.5 mA as Current Setting 1 and 5 mA as the Current Setting 2. At the same time they must also decide how long they want the secondary current to stay active before reverting to the primary current. This is controlled by the Timer Counter Control Bits DB14 to DB11 (TC4–TC1) in the Function Latch. The truth table is given in Table V.

Now, when users wish to program a new output frequency, they can simply program the AB counter latch with new values for A and B. At the same time they can set the CP Gain bit to a "1," which sets the charge pump with the value in CPI6–CPI4 for a period of time determined by TC4–TC1. When this time is up, the charge pump current reverts to the value set by CPI3–CPI1. At the same time the CP Gain bit in the A, B Counter latch is reset to 0 and is now ready for the next time that the user wishes to change the frequency again.

Note that there is an enable feature on the Timer Counter. It is enabled when Fastlock Mode 2 is chosen by setting the Fastlock Mode bit (DB10) in the Function Latch to "1."

Charge Pump Currents

CPI3, CPI2, CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, CPI4 program Current Setting 2 for the charge pump. The truth table is given in Table V.

Prescaler Value

P2 and P1 in the Function Latch set the prescaler values. The prescaler value should be chosen so that the prescaler output frequency is always less than or equal to 300 MHz. Thus, with an RF frequency of 4 GHz, a prescaler value of 16/17 is valid but a value of 8/9 is not valid.

PD Polarity

This bit sets the Phase Detector Polarity Bit. See Table V.

CP Three-State

This bit controls the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

THE INITIALIZATION LATCH

When C2, C1 = 1, 1, the Initialization Latch is programmed. This is essentially the same as the Function Latch (programmed when C2, C1 = 1, 0).

However, when the Initialization Latch is programmed there is an additional internal reset pulse applied to the R and AB counters. This pulse ensures that the AB counter is at load point when the AB counter data is latched and the device will begin counting in close phase alignment.

If the Latch is programmed for synchronous power-down (CE pin is High; PD1 bit is High; PD2 bit is Low), the internal pulse also triggers this powerdown. The prescaler reference and the oscillator input buffer are unaffected by the internal reset pulse and so close phase alignment is maintained when counting resumes.

When the first AB counter data is latched after initialization, the internal reset pulse is again activated. However, successive AB counter loads after this will not trigger the internal reset pulse.

DEVICE PROGRAMMING AFTER INITIAL POWER-UP

After initially powering up the device, there are three ways to program the device.

Initialization Latch Method

- Apply V_{DD}.
- Program the Initialization Latch ("11" in two LSBs of input word). Make sure that F1 bit is programmed to "0."
- Do a Function Latch load ("10" in two LSBs of the control word), making sure that the F1 bit is programmed to a "0."
- Do an R load ("00" in two LSBs).
- Do an AB load ("01" in two LSBs).

When the Initialization Latch is loaded, the following occurs:

1. The function latch contents are loaded.
2. An internal pulse resets the R, A, B and timeout counters to load state conditions and also three-states the charge pump. Note that the prescaler bandgap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
3. Latching the first AB counter data after the initialization word will activate the same internal reset pulse. Successive AB loads will not trigger the internal reset pulse unless there is another initialization.

CE Pin Method

- Apply V_{DD}.
- Bring CE low to put the device into power-down. This is an asynchronous power-down in that it happens immediately.
- Program the Function Latch (10).
- Program the R Counter Latch (00).
- Program the AB Counter Latch (01).
- Bring CE high to take the device out of power-down.

The R and AB counters will now resume counting in close alignment. Note that after CE goes high, a duration of 1 µs may be required for the prescaler bandgap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down in order to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it has been programmed at least once after V_{DD} was initially applied.

Counter Reset Method

- Apply V_{DD}.
- Do a Function Latch Load ("10" in two LSBs). As part of this, load "1" to the F1 bit. This enables the counter reset.
- Do an R Counter Load ("00" in two LSBs).
- Do an AB Counter Load ("01" in two LSBs).
- Do a Function Latch Load ("10" in two LSBs). As part of this, load "0" to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump, but does not trigger synchronous power-down.

APPLICATION SECTION

Local Oscillator for LMDS Base Station Transmitter

Figure 7 shows the ADF4106 being used with a VCO to produce the LO for an LMDS base station operation in the 5.4 GHz to 5.8 GHz band.

The reference input signal is applied to the circuit at $FREF_{IN}$ and, in this case, is terminated in 50 Ω. A typical base station system would have either a TCXO or an OCXO driving the Reference Input without any 50 Ω termination.

In order to have a channel spacing of 1 MHz at the output, the 10 MHz reference input must be divided by 10, using the on-chip reference divider of the ADF4106.

The charge pump output of the ADF4106 (Pin 2) drives the loop filter. In calculating the loop filter component values, a number of items need to be considered. In this example, the loop filter was designed so that the overall phase margin for the system would be 45 degrees. Other PLL system specifications are given below:

K_D = 2.5 mA
K_V = 80 MHz/V
Loop Bandwidth = 50 kHz
F_{REF} = 1 MHz
N = 5800
Extra Reference Spur Attenuation = 10 dB

All of these specifications are needed and used to come up with the loop filter component values shown in Figure 7.

Figure 7 gives a typical phase noise performance of –83 dBc/Hz at 1 kHz offset from the carrier. Spurs are better than –62 dBc.

The loop filter output drives the VCO, which, in turn, is fed back to the RF input of the PLL synthesizer and also drives the RF Output terminal. A T-circuit configuration provides 50 Ω matching between the VCO output, the RF output and the RF_{IN} terminal of the synthesizer. Note that the ADF4106 RF input looks like 50 Ω at 5.8 GHz and so no terminating resistor is needed. When operating at lower frequencies however, this is not the case.

In a PLL system, it is important to know when the system is in lock. In Figure 7, this is accomplished by using the MUXOUT signal from the synthesizer. The MUXOUT pin can be programmed to monitor various internal signals in the synthesizer. One of these is the LD or lock-detect signal.

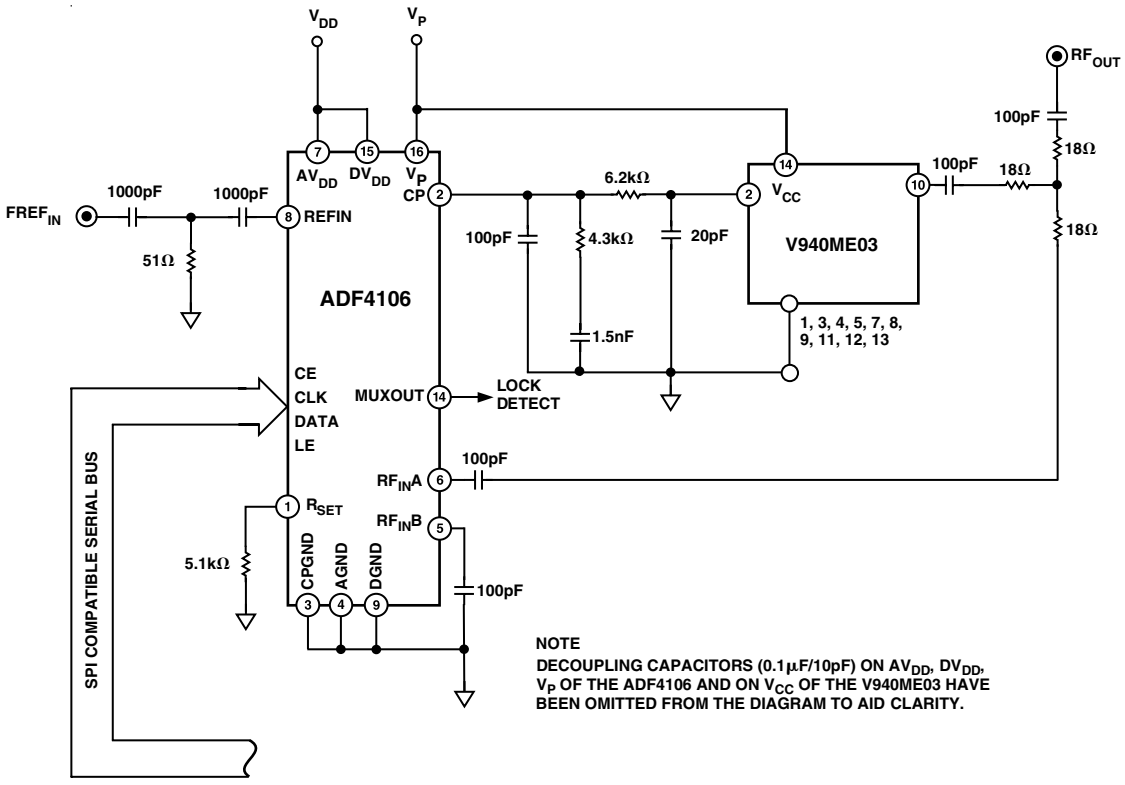


Figure 7. Local Oscillator for LMDS Base Station

INTERFACING

The ADF4106 has a simple SPI-compatible serial interface for writing to the device. SCLK, SDATA and LE control the data transfer. When LE (Latch Enable) goes high, the 24 bits which have been clocked into the input register on each rising edge of SCLK will get transferred to the appropriate latch. See Figure 1 for the Timing Diagram and Table I for the Latch Truth Table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 μs. This is certainly more than adequate for systems which will have typical lock times in hundreds of microseconds.

ADuC812 Interface

Figure 8 shows the interface between the ADF4106 and the ADuC812 microconverter. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The microconverter is set up for SPI Master Mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4106 needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the microconverter to the device. When the third byte has been written the LE input should be brought high to complete the transfer.

On first applying power to the ADF4106, it needs at three writes (one each to the R counter latch, the N counter latch and the function latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed will be 166 kHz.

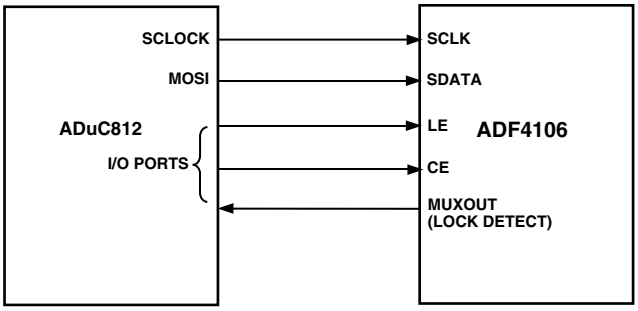


Figure 8. ADuC812 to ADF4106 Interface

ADSP-2181 Interface

Figure 9 shows the interface between the ADF4106 and the ADSP-21xx Digital Signal Processor. The ADF4106 needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the Autobuffered Transmit Mode of operation with Alternate Framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the Autobuffered mode and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

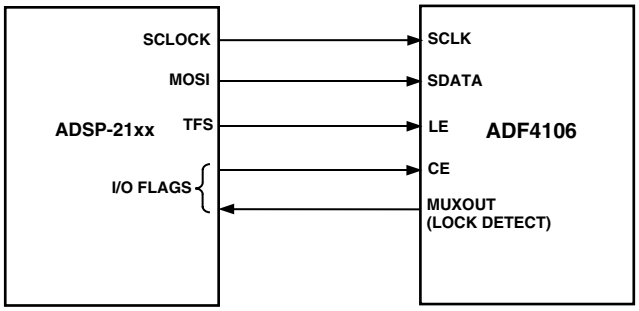
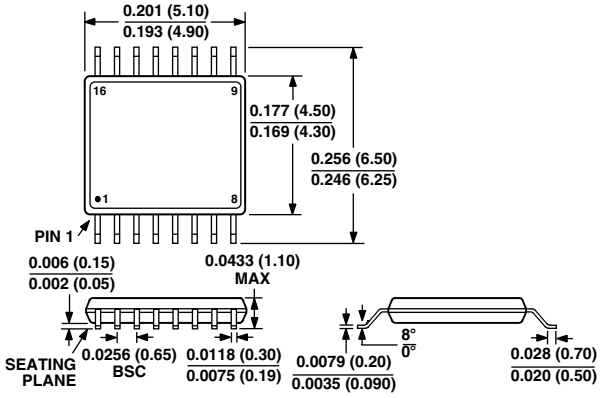


Figure 9. ADSP-21xx to ADF4106 Interface

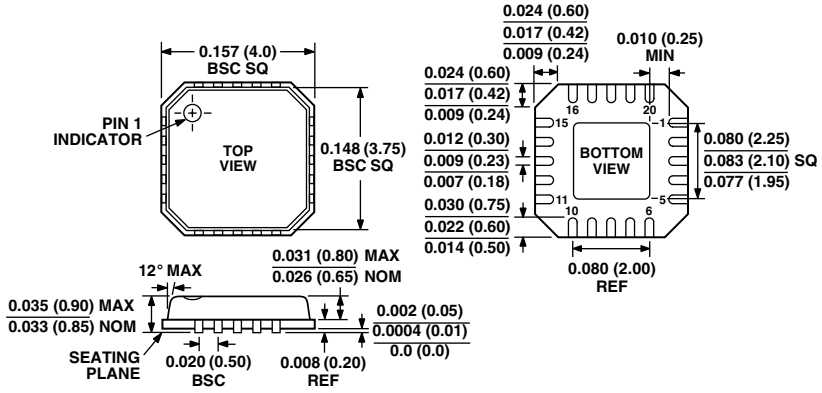
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

16-Lead Thin Shrink SO Package (TSSOP)
(RU-16)



20-Leadless Frame Chip Scale Package (LFCSP)
(CP-20)



CONTROLLING DIMENSIONS ARE IN MILLIMETERS

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