



# Evaluation Board for the ADV7192 Digital Video Encoder

## Eval-ADV7192EB

### FEATURES

**On-Board Reference**

**On-Board Clock**

**External PLL**

**8 or 16 bit Pixel Data Input**

**3x10bit Progressive Scan input**

**ADuC812 Microconverter + Switch Control**

**Direct Hook-Up to Printer Port of PC**

**PC Software for Control of ADV7192 modes**

### INTRODUCTION

This Application Note describes the ADV7192EB evaluation board which supports the ADV7192 Digital Video Encoder. The device accepts CCIR601 data and converts into analog Composite, Y/C, RGB or YUV video signals in

PAL or NTSC format. Full data on the ADV7192 is available in the ADV7192 data sheet, available from Analog Devices and should be consulted in conjunction with this note when using the Evaluation Board.

### REQUIREMENTS

The ADV7192 requires a DC power supply which is able to deliver a minimum of 3.3V. Ideal operating voltage for the ADV7192EB is 5V. Current requirements are approx. 0.5 A. To run the software which is supplied with the ADV7192 it is necessary to connect the printer port LPT1 of the PC to the boards 36pin

Centronics connector.

In order to run the software on a PC the operating system needs to be Windows 95 or Windows 98. The system requirements ask for any Pentium I, PMMx or Pentium II PC.

### GENERAL DESCRIPTION

The ADV7192EB provides a 25-pin input port over which pixel data in CCIR601 format can be input. Test pattern generators providing these standards are the Tektronix TSG601 handheld signal generator or the Tektronix TPG20. The input pixel data is converted from ECL level to TTL level via the MC10125TTLS.

It is also possible to input data in 16-Bit format or in progressive scan *YPrPb* format using P6, P14, P15 and P16.

If a different clock source as that provided by the pixel data is required, the ADV7192EB features a 27Mhz Oscillator (Y1) which can be connected over jumper J8.

The ADV7192 contains an internal PLL which synchronizes 27MHz operation with 54 MHz operation. IC570 (U10) should be used if an external PLL is required.

Two on-board push-buttons provide control over the SCRESET/RTC/TR pin and the RESET pin. According to the settings in Mode Register 4, whenever PB2 is pressed, a timing reset or a

SCreset is applied.

When RESET (PB1) is pressed the internal registers of the ADV7192 reset to default register settings (see following page).

The ADV7192EB also features an external Voltage Reference (U19) which provides 1.235V Output Voltage.

The DAC outputs are fed to an AD847 buffer op-amp (U1-U6) followed by a passive low-pass filter before being output over the BNC connection. The DAC outputs can be directly accessed at test points T1-T6.

The ADV7192EB is fitted with the ADuC812 Microconverter. With the supplied ADV7192 software, there is an additional 8051 .asm Code. This code contains demo settings for the ADV7192. According to the switch setting of SW1 the individual demos can be displayed.

The ADuC812 is optional and is not required to make full use of the ADV7192EB.

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## REGISTER SETTINGS ON POWER-UP AND ON RESET

The following register settings will correspond to the above settings:

After pressing the reset button PB1 on the evaluation board, the register settings of the ADV7192 will set up as follows:

NTSC Video Standard.  
2xOversampling Mode  
DAC A, B, C off  
DAC D, E, F on

### Disabled:

MR2: Sleep Mode Control,- Pixel Data Valid,  
Standard I2C, Square Pixel, SCART  
MR3: Closed Captioning, TTX Bit Request,  
Teletext, VBI  
MR4: Color Bars, VSYNC\_3H  
MR5: CLAMP, RGB Sync, Y-Level Control  
MR7: Sharpness Filter, Brightness Control, Hue  
Adjust, Luma Saturation, Color Control  
MR8: Gamma Control, DNR, Double Buffering,  
Progressive Scan input, 10-Bit input  
MR9: Undershoot Limiter  
OCR: CLKOUT Pin

### Enabled:

MR2: Pedestal,  
MR4: Burst, Chrominance,  
MR6: PLL, Power-Up Sleep Mode,

### Output Configuration:

DAC A: G  
DAC B: B  
DAC C: R  
DAC D: CVBS  
DAC E: LUMA  
DAC F: CHROMA

Timing Mode 0, Slave, Blank Disabled  
Interlaced Mode, 720 active pixel line duration,  
normal operating mode (no genlock), UV default  
levels, TTX input, HSO Out, 8-bit Pixel Port,  
no Chroma Delay

Subcarrier Frequency Register 0: CB  
Subcarrier Frequency Register 1: 8A  
Subcarrier Frequency Register 2: 09  
Subcarrier Frequency Register 3: 2A

MR0	00hex
MR1	07hex
MR2	08hex
MR3	00hex
MR4	00hex
MR5	00hex
MR6	00hex
MR7	00hex
MR8	00hex
MR9	00hex
OCR	72hex
TR0	08hex
TR1	00hex
SFR0	CBhex
SFR1	8Ahex
SFR2	09hex
SFR3	2Ahex
SPR	00hex

all other registers : 00hex

After powering up the ADV7192EB a hardware reset should be applied (PB1).

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## EVALUATION SOFTWARE

In order to give the user complete control over the ADV7192, a computer program is supplied with the board.

### Setting Up:

Insert DISK 1 into the floppy drive and double click on "SETUP.EXE" and you will be prompted for all other necessary information.

### Running the Software:

Double clicking the ADV7192 icon will run the software for the evaluation board.

### Initialisation:

After starting the software you will be asked to load a preset.

If you are not familiar with the software it is recommended to o.k. this message.

You will have the ADV7192 immediately configured in such a way that it will output a color bar signal when the DAC A BNC output is connected to a NTSC monitor.

For this configuration it is not necessary to provide an input signal because the internal color bars are enabled. The register settings for this preset can be checked in clicking on the READ ALL REGISTERS in the main window.

Otherwise it is recommended to consult the datasheet for information about each control.

## IMPORTANT THINGS TO KNOW:

### Validity of Settings:

The evaluation software can automatically check for an acknowledge or, when any register is changed can automatically read-back the new value stored in that register. The "ACKcheck" function is in the "Options" menu. The "Continuous Read" function may be enabled in the "Register Access" menu.

### PC Compatible Programming:

This version of software does not take into account the ability of the ADV7192 to accept continuous streams of data. Instead, for every register write or read, it completely re-initiates a start sequence (see the ADV7192 Data sheet for information on different ways registers can be written to). This means that more information has to be written to the MPU port extending the time required to program the ADV7192. This, while being a valid way of writing to the ADV7192 is not the optimum method of writing to the ADV7192.

### Dynamically Linked Menu System:

All menus in this software are interactive, so when (for example) you change the value of a register all switch settings relevant to that register change will automatically change to the correct state, the inverse is also correct.

## LINK HEADERS

### ADV7192 LINKS

These links are used for operating the ADV7192 encoder:

- J1** Ground link
- J2** Link clock signal to header P2.
- J3** Ground link
- J4, J6** Link Pull-Down Resistors (2K2) of 8/10-bit pixel input to Ground.
- J8** Clock Mode  
J8A: ADV7192 is clocked from the on-board 27Mhz clock.  
J8B : ADV7192 is clocked from the clock contained in the pixel input.
- J9, J12**  
If U10 (IC570) is used as an external PLL (as an alternative to the internal PLL)  
J12A provides the 27Mhz input clock and  
J9A provides the 54Mhz clock to the ADV7192.
- J10** Link clock signal to CLKIN pin of the ADV7192 and bypass the external PLL circuitry.
- J19** Link ALSB pin to Ground. This jumper should be inserted when ALSB is chosen to be set low.
- J20** Link BLANK pin to Ground. This allows control over the BLANK pin functionality over the software. If unconnected the BLANK pin is disabled permanently and the software can not control the BLANK pin functionality.
- J21** Link PAL\_NTSC pin to Ground. Inserting this jumper will configure the ADV7192 to run in NTSC mode regardless of the settings in Mode Register 0. The settings in Mode Register 2 can however override this pin (Standard I2C Control).
- J22** Timing Reset or SCReset / PB2  
J22A: The SCRESET/RTC/TR pin and PB2 are configured as a Timing Reset.  
J22B: The SCRESET/RTC pin is configured as a subcarrier phase reset input pin or as a RTC input pin, according to the settings in Mode Register 4. When Mode Register 4 is configured in Subcarrier Reset mode, PB2 will initiate a Subcarrier Phase reset and the Subcarrier Phase will reset to Field 0 at the start of the next Field.

## MICROCONVERTER ADuC812 LINKS

These links are required in conjunction with the ADuC812 Microconverter:

- J11** Link Vertical Sync signals to Interrupt.
  - J11A: the vertical sync signal VSO initiates an interrupt.
  - J11B: the vertical sync signal VSYNC initiates an interrupt.
  
- J13** Link Horizontal Sync signal to Interrupt.
  - J13A: the horizontal sync signal HSO initiates an interrupt.
  - J13B: the horizontal sync signal HSYNC initiates an interrupt.
  
- J14** Link TTX signal to Interrupt.
  
- J15** Link TTXRQ signal to Interrupt.
  
- J16** If the Microconverter is to be used with the ADV7192 this link sets the SCL of the I2C interface. This link must be set whenever the Microconverter is to be used with the ADV7192.
  
- J17** If the Microconverter is to be used with the ADV7192 this link sets the SDA of the I2C interface. This link must be set whenever the Microconverter is to be used with the ADV7192.
  
- J18** When this link is set, serial download on power-up or external Reset is enabled. After downloading the program this jumper must never be inserted, otherwise the ADuC program will be lost forever.

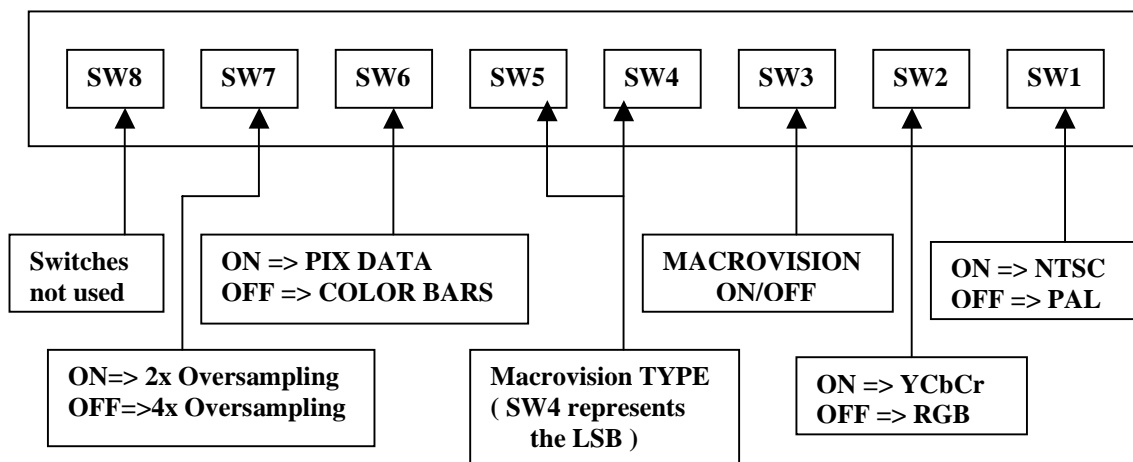
## ADuC812 MICROCONVERTER

To make most efficient use of the ADuC812's capacities, it is recommended to consult the datasheet for the ADuC812 and the 'Get Started Guide' for the

QuickStart™ Development System V1.1 which is the software to interface the PC and the Microconverter. All can be obtained from Analog Devices.

In this application the ADuC812 is used to load some presets, which are controlled over the Mode Control switch SW1:

## ADV719 :SWITCHES FUNCTIONALITIES



In order to make use of this facility the following instructions should be followed:

1. The ADV7192EB has to be connected over the 25pin pixel port to a signal generator supplying valid CCIR601 data.  
Jumper J8 has to be set to J8B.
2. The disks supplied with the ADV7192EB contain a file called '92dem.asm'.  
Double click on ASM51.exe and name the path and filename of the .asm file. A message should come up which reads:  
'ASSEMBLY COMPLETE, 0 ERRORS FOUND'
3. Connect the 5pin connector to P3 (N.C. on pin 5). Insert jumper J18.  
Power-up the board.  
This special cable can be provided or requested from Analog Devices.
4. Double click on DEBUG812.exe. Under SESSION, click on DEMO.SES. In the CONFIGURATION window, click on FILES and

load the compiled .lst and .hex files for 92dem.asm, that is 92dem.lst and 92dem.hex.

5. Press the RESET button on the board. Click on RESET in the CONFIGURATION window. The data will be uploaded and the status bar should read: 'Data uploaded successfully'.
6. Click on the PROG icon in the ADuC812 Debugger. The status bar should read: 'Data uploaded successfully'.
7. Click on the RUN icon (next to PROG).
8. Load the ADV7192 Evaluation Software.  
Cancel the message which shows up in the main window.  
Remove jumper J18 and press RESET on the evaluation board.  
The switch settings will operate as indicated above.  
Note, when setting individual switches all other switches have to be set to ON.

# EVAL-ADV7192EB

## ADV7192EB CONNECTIONS

