Evaluation Board for the ADV7194 Digital Video Encoder

Eval-ADV7194EB

FEATURES
On-Board Reference
On-Board Clock
External PLL
8, 10, 16 or 20 bit Pixel Data Input
***YPrPb* Input**
ADuC812 Microconverter + Switch Control
Direct Hook-Up to Printer Port of PC
PC Software for Control of ADV7194 modes

INTRODUCTION

This Application Note describes the ADV7194EB evaluation board which supports the ADV7194 Digital Video Encoder. The device accepts CCIR601 data and converts into analog Composite, Y/C, RGB or YUV video signals in PAL or NTSC format. Full data on the ADV7194 is available in the ADV7194 data sheet, available from Analog Devices and should be consulted in conjunction with this note when using the Evaluation Board.

REQUIREMENTS

The ADV7194 requires a DC power supply which is able to deliver a minimum of 3.3V. Ideal operating voltage for the ADV7194EB is 5V. Current requirements are approx. 0.5 A**.**
To run the software which is supplied with the ADV7194 it is necessary to connect the printer port LPT1 of the PC to the boards 36pin Centronics connector.
In order to run the software on a PC the operating system needs to be Windows 95 or Windows 98. The system requirements ask for any Pentium I, PMMx or Pentium II PC.

GENERAL DESCRIPTION

The ADV7194EB provides a 25-pin input port over which pixel data in CCIR601 format can be input. Test pattern generators providing these standards are the Tektronix TSG601 handheld signal generator or the Tektronix TPG20. The input pixel data is converted from ECL level to TTL level via the MC10125TTLs.
It is also possible to input data in 16-Bit or 20Bit format or in progressive scan *YPrPb* format using P6, P14, P15 and P16.
If a different clock source as that provided by the pixel data is required, the ADV7194EB features a 27Mhz Oscillator (Y1) which can be connected over jumper J8.
The ADV7194 contains an internal PLL which synchronizes 27MHz operation with 54 MHz operation. IC570 (U10) should be used if an external PLL is required.
Two on-board push-buttons provide control over the SCRESET/RTC/TR pin and the RESET pin. According to the setttings in Mode Register 4, whenever PB2 is pressed, a timing reset or a SCreset is applied.
When RESET (PB1) is pressed the internal registers of the ADV7194 reset to default register settings (see following page).
The ADV7194EB also features an external Voltage Reference (U19) which provides 1.235V Output Voltage.

The DAC outputs are fed to an AD847 buffer op-amp (U1-U6) followed by a passive low-pass filter before being output over the BNC connection. The DAC outputs can be directly accessed at test points T1-T6.

The ADV7194EB is fitted with the ADuC812 Microconverter. With the supplied ADV7194 software, there is an additional 8051 .asm Code. This code contains demo settings for the ADV7194. According to the switch setting of SW1 the individual demos can be displayed.

The ADuC812 is optional and is not required to make full use of the ADV7194EB.

Rev 2

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REGISTER SETTINGS ON POWER-UP AND ON RESET

After pressing the reset button PB1 on the evaluation board, the register settings of the ADV7194 will set up as follows:

NTSC Video Standard.
2xOversampling Mode
DAC A, B, C off
DAC D, E, F on

Disabled:
MR2: Sleep Mode Control,- Pixel Data Valid, Standard I2C, Square Pixel, SCART
MR3: Closed Captioning, TTX Bit Request, Teletext, VBI
MR4: Color Bars, VSYNC_3H
MR5: CLAMP, RGB Sync, Y-Level Control
MR7: Sharpness Filter, Brightness Control, Hue Adjust, Luma Saturation, Color Control
MR8: Gamma Control, DNR, Double Buffering, Progressive Scan input, 10-Bit input
MR9: Undershoot Limiter
OCR:CLKOUT Pin

Enabled:
MR2: Pedestal,
MR4: Burst, Chrominance,
MR6: PLL, Power-Up Sleep Mode,

Output Configuration:
DAC A: G
DAC B: B
DAC C: R
DAC D: CVBS
DAC E: LUMA
DAC F: CHROMA

Timing Mode 0, Slave, Blank Disabled
Interlaced Mode, 720 active pixel line duration, normal operating mode (no genlock), UV default levels, TTX input, HSO Out, 8-bit Pixel Port, no Chroma Delay

Subcarrier Frequency Register 0: CB
Subcarrier Frequency Register 1: 8A
Subcarrier Frequency Register 2: 09
Subcarrier Frequency Register 3: 2A

The following register settings will correspond to the above settings:

MR0	00hex
MR1	07hex
MR2	08hex
MR3	00hex
MR4	00hex
MR5	00hex
MR6	00hex
MR7	00hex
MR8	00hex
MR9	00hex
OCR	72hex
TR0	08hex
TR1	00hex
SFR0	CBhex
SFR1	8Ahex
SFR2	09hex
SFR3	2Ahex
SPR	00hex

all other registers : 00hex

After powering up the ADV7194EB a hardware reset should be applied (PB1).

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EVALUATION SOFTWARE

In order to give the user complete control over the ADV7194, a computer program is supplied with the board.

Setting Up:

Insert DISK 1 into the floppy drive and double click on "SETUP.EXE" and you will be prompted for all other necessary information.

Running the Software:

Double clicking the ADV7194 icon will run the software for the evaluation board.

Initialisation:

After starting the software you will be asked to load a preset.
If you are not familiar with the software it is recommended to o.k. this message.
You will have the ADV7194 immediately configured in such a way that it will output a color bar signal when the DAC A BNC output is connected to a NTSC monitor.
For this configuration it is not necessary to provide an input signal because the internal color bars are enabled. The register settings for this preset can be checked in clicking on the READ ALL REGISTERS in the main window.
Otherwise it is recommended to consult the datasheet for information about each control.

IMPORTANT THINGS TO KNOW:

Validity of Settings:

The evaluation software can automatically check for an acknowledge or, when any register is changed can automatically read-back the new value stored in that register. The "ACKcheck" function is in the "Options" menu. The "Continuous Read" function may be enabled in the "Register Access" menu.

I²C Compatible Programming:

This version of software does not take into account the ability of the ADV7194 to accept continuous streams of data. Instead, for every register write or read, it completely re-initiates a start sequence (see the ADV7194 Data sheet for information on different ways registers can be written to). This means that more information has to be written to the MPU port extending the time required to program the ADV7194.This, while being a valid way of writing to the ADV7194 is not the optimum method of writing to the ADV7194.

Dynamically Linked Menu System:

All menues in this software are interactive, so when (for example) you change the value of a register all switch settings relevant to that register change will automatically change to the correct state, the inverse is also correct.

LINK HEADERS

ADV7194 LINKS

These links are used for operating the ADV7194 encoder:

J1 Ground link

J2 Link clock signal to header P2.

J3 Ground link

J4, J6 Link Pull-Down Resistors (2K2) of 8/10-bit pixel input to Ground.

J8 Clock Mode
- J8A: ADV7194 is clocked from the on-board 27Mhz clock.
- J8B : ADV7194 is clocked from the clock contained in the pixel input.

J9, J12 If U10 (IC570) is used as an external PLL (as an alternative to the internal PLL).
J12A provides the 27Mhz input clock and
J9A provides the 54Mhz clock to the ADV7194.

J10 Link clock signal to CLKIN pin of the ADV7194 and bypass the external PLL circuitry.

J19 Link ALSB pin to Ground. This jumper should be inserted when ALSB is chosen to be set low.

J20 Link BLANK pin to Ground. This allows control over the BLANK pin functionality over the software. If unconnected the BLANK pin is disabled permanently and the software can not control the BLANK pin functionality.

J21 Link PAL_NTSC pin to Ground. Inserting this jumper will configure the ADV7194 to run in NTSC mode regardless of the settings in Mode Register 0. The settings in Mode Register 2 can however override this pin (Standard I2C Control).

J22 Timing Reset or SCReset / PB2

- J22A: The SCRESET/RTC/TR pin and PB2 are configured as a Timing Reset.
- J22B: The SCRESET/RTC pin is configured as a subcarrier phase reset input pin or as a RTC input pin, according to the settings in Mode Register 4. When Mode Register 4 is configured in Subcarrier Reset mode, PB2 will initiate a Subcarrier Phase reset and the Subcarrier Phase will reset to Field 0 at the start of the next Field.

MICROCONVERTER ADuC812 LINKS

These links are required in conjunction with the ADuC812 Microconverter:

J11 Link Vertical Sync signals to Interrrupt.
- J11A: the vertical sync signal VSO initiates an interrrupt.
- J11B: the vertical sync signal VSYNC initiates an interrupt.

J13 Link Horizontal Sync signal to Interrrupt.
- J13A: the horizontal sync signal HSO initiates an interrrupt.
- J13B: the horizontal sync signal HSYNC initiates an interrupt.

J14 Link TTX signal to Interrrupt.

J15 Link TTXRQ signal to Interrupt.

J16 If the Microconverter is to be used with the ADV7194 this link sets the SCL of the I2C interface. This link must be set whenever the Microconverter is to be used with the ADV7194.

J17 If the Microconverter is to be used with the ADV7194 this link sets the SDA of the I2C interface. This link must be set whenever the Microconverter is to be used with the ADV7194.

J18 When this link is set, serial download on power-up or external Reset is enabled. After downloading the program this jumper must never be inserted, otherwise the ADuC program will be lost forever.

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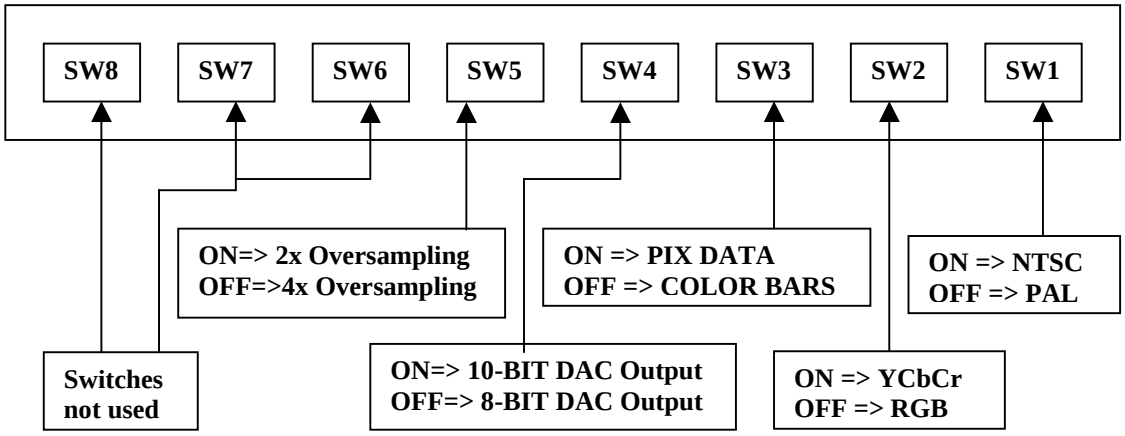
ADuC812 MICROCONVERTER

To make moste efficient use of the ADuC812's capacities, it is recommended to consult the datasheet for the ADuC812 and the 'Get Started Guide' for the QuickStart™ Development System V1.1 which is the software to interface the PC and the Microconverter. All can be obtained from Analog Devices.

In this application the ADuC812 is used to load some presets, which are controlled over the Mode Control switch SW1:

ADV7194 :SWITCHES FUNCTIONALITIES



In order to make use of this facility the following instructions should be followed:

1. The ADV7194EB has to be connected over the 25pin pixel port to a signal generator supplying valid CCIR601 data.
Jumper J8 has to be set to J8B.

2. The disks supplied with the ADV7194EB contain a file called '94dem.asm'.
Double click on ASM51.exe and name the path and filename of the .asm file. A message should come up which reads:
'ASSEMBLY COMPLETE, 0 ERRORS FOUND'

3. Connect the 5pin connector to P3 (N.C. on pin 5).
Insert jumper J18.
Power-up the board.
This special cable can be provided or requested from Analog Devices.

4. Double click on DEBUG812.exe. Under SESSION, click on DEMO.SES. In the CONFIGURATION window, click on FILES and load the compiled .lst and .hex files for 94dem.asm, that is 94dem.lst and 94dem.hex.

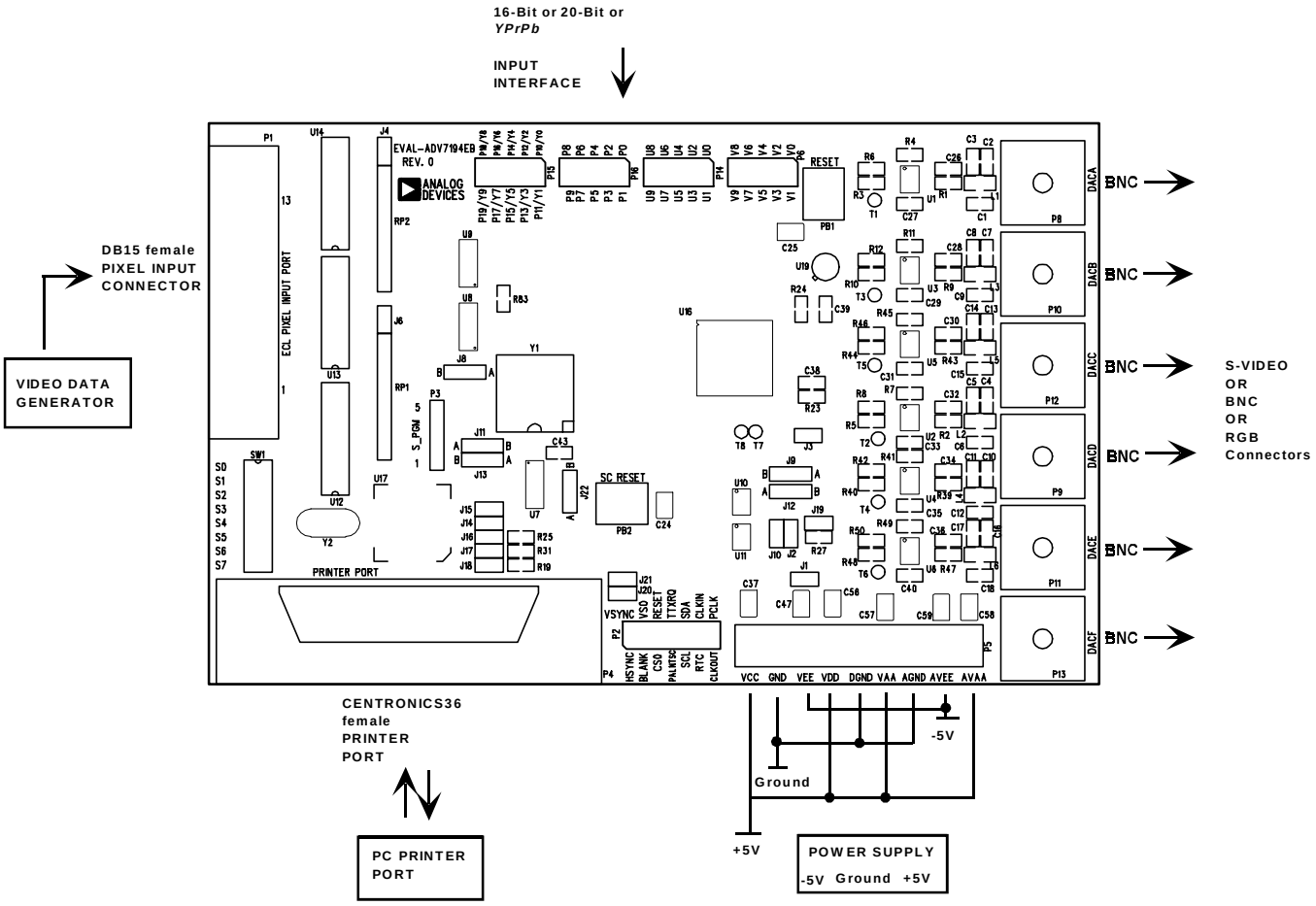
5. Press the RESET button on the board. Click on RESET in the CONFIGURATION window. The data will be uploaded and the
status bar should read:' Data uploaded successfully'.

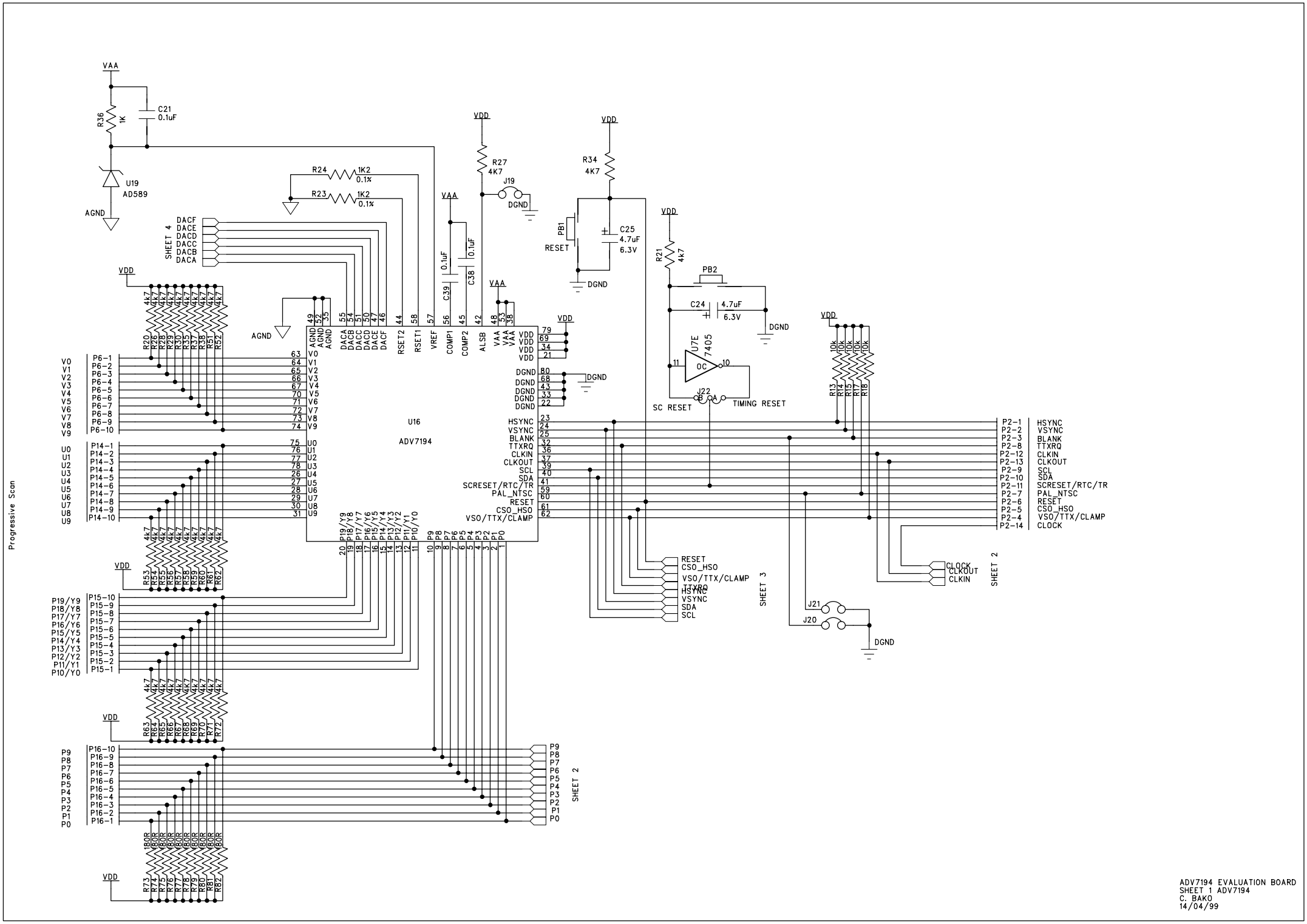
6. Click on the PROG icon in the ADuC812 Debugger. The status bar should read: 'Data uploaded successfully'.

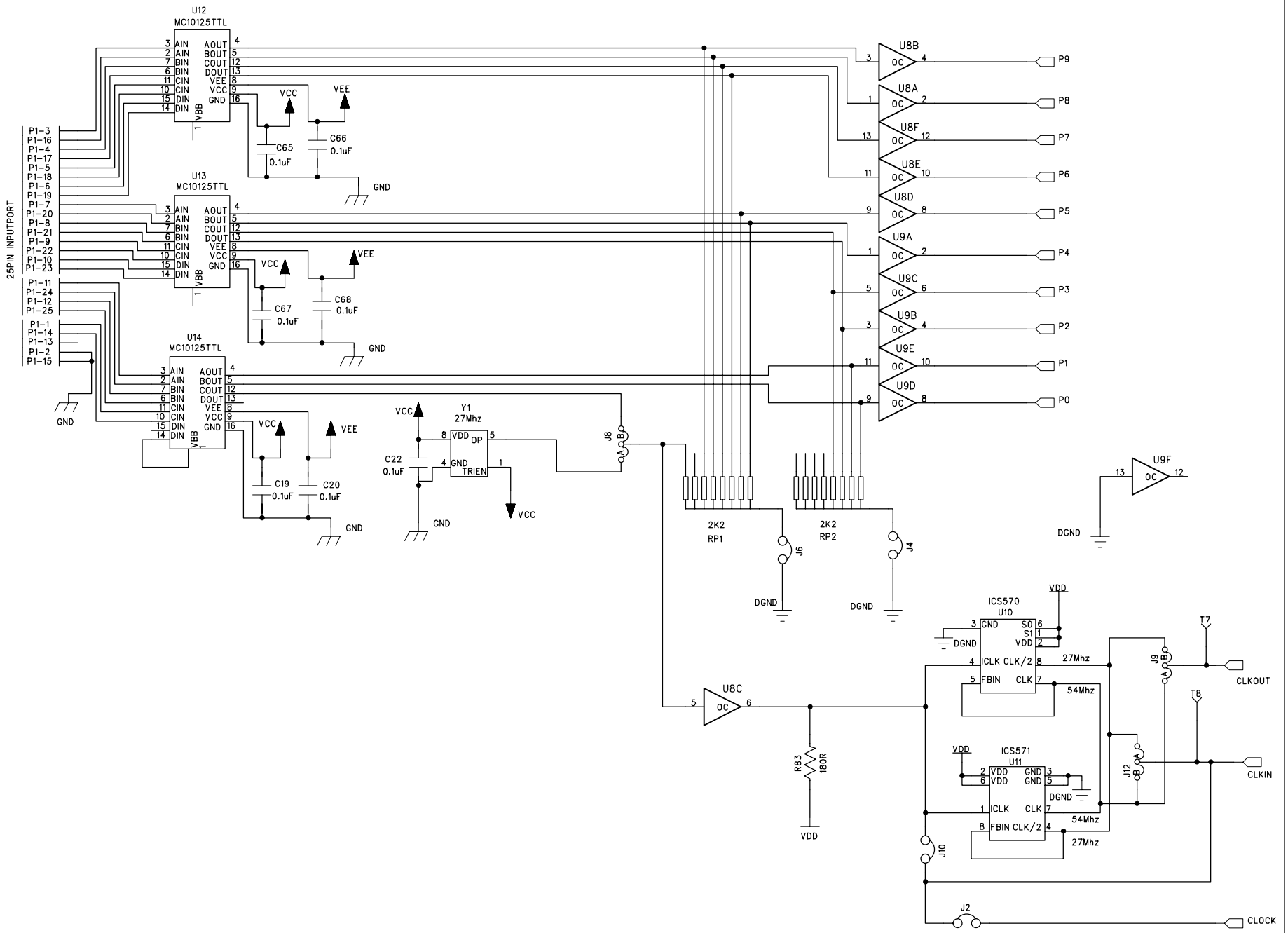
7. Click on the RUN icon (next to PROG).

8. Load the ADV7194 Evaluation Software.
Cancel the message which shows up in the main window.
Remove jumper J18 and press RESET on the evaluation board.
The switch settings will operate as indicated above.
Note, when setting individual switches
all other switches have to be set to ON.

ADV7194EB CONNECTIONS




Progressive Scan
VAA
R36 1K
C21 0.1uF
U19 AD589
AGND
R24 1K2 0.1%
R23 1K2 0.1%
VDD
R27 4K7
J19
DGND
R34 4K7
PB1
RESET
C25 4.7uF 6.3V
R21 4K7
PB2
C24 4.7uF 6.3V
U7E 7405
OC
J22
SC RESET
TIMING RESET
SHEET 4
DACF
DACE
DACD
DACC
DACB
DACA
C39 0.1uF
C38 0.1uF
U16
ADV7194
HSYNC
VSYNC
BLANK
TTXRQ
CLKIN
CLKOUT
SCL
SDA
SCRESET/RTC/TR
PAL_NTSC
RESET
CSO_HSO
VSO/TTX/CLAMP
SHEET 2
SHEET 3
J21
J20
P2-1 HSYNC
P2-2 VSYNC
P2-3 BLANK
P2-8 TTXRQ
P2-12 CLKIN
P2-13 CLKOUT
P2-9 SCL
P2-10 SDA
P2-11 SCRESET/RTC/TR
P2-7 PAL_NTSC
P2-6 RESET
P2-5 CSO_HSO
P2-4 VSO/TTX/CLAMP
P2-14 CLOCK
CLOCK
CLKOUT
CLKIN
ADV7194 EVALUATION BOARD
SHEET 1 ADV7194
C. BAKO
14/04/99



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SHEET 2 INPUT
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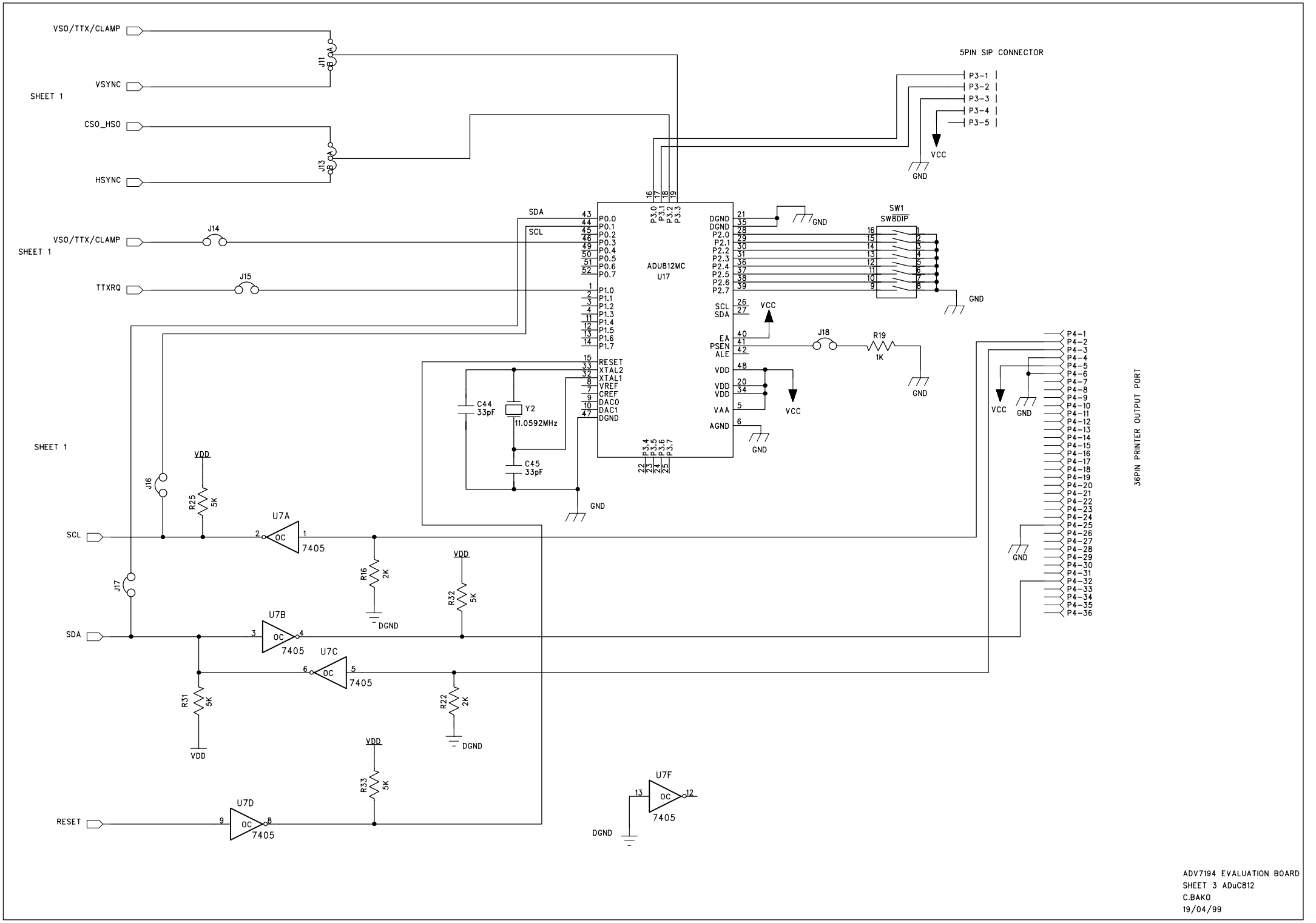
VSO/TTX/CLAMP
VSYNC
SHEET 1
CSO_HSO
HSYNC
J11
J13
5PIN SIP CONNECTOR
P3-1
P3-2
P3-3
P3-4
P3-5
VCC
GND
SDA
SCL
J14
VSO/TTX/CLAMP
SHEET 1
TTXRQ
J15
ADU812MC
U17
P0.0
P0.1
P0.2
P0.3
P0.4
P0.5
P0.6
P0.7
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
RESET
XTAL2
XTAL1
VREF
CREF
DAC0
DAC1
DGND
P3.0
P3.1
P3.2
P3.3
P3.4
P3.5
P3.6
P3.7
DGND
P2.0
P2.1
P2.2
P2.3
P2.4
P2.5
P2.6
P2.7
SCL
SDA
EA
PSEN
ALE
VDD
VAA
AGND
SW1
SW8DIP
J18
R19
1K
C44
33pF
Y2
11.0592MHz
C45
33pF
SHEET 1
J16
VDD
R25
5K
U7A
SCL
7405
R16
2K
DGND
VDD
R32
5K
J17
U7B
SDA
7405
U7C
7405
R31
5K
VDD
R22
2K
DGND
VDD
R33
5K
U7D
RESET
7405
U7F
7405
DGND
P4-1
P4-2
P4-3
P4-4
P4-5
P4-6
P4-7
P4-8
P4-9
P4-10
P4-11
P4-12
P4-13
P4-14
P4-15
P4-16
P4-17
P4-18
P4-19
P4-20
P4-21
P4-22
P4-23
P4-24
P4-25
P4-26
P4-27
P4-28
P4-29
P4-30
P4-31
P4-32
P4-33
P4-34
P4-35
P4-36
36PIN PRINTER OUTPUT PORT
ADV7194 EVALUATION BOARD
SHEET 3 ADuC812
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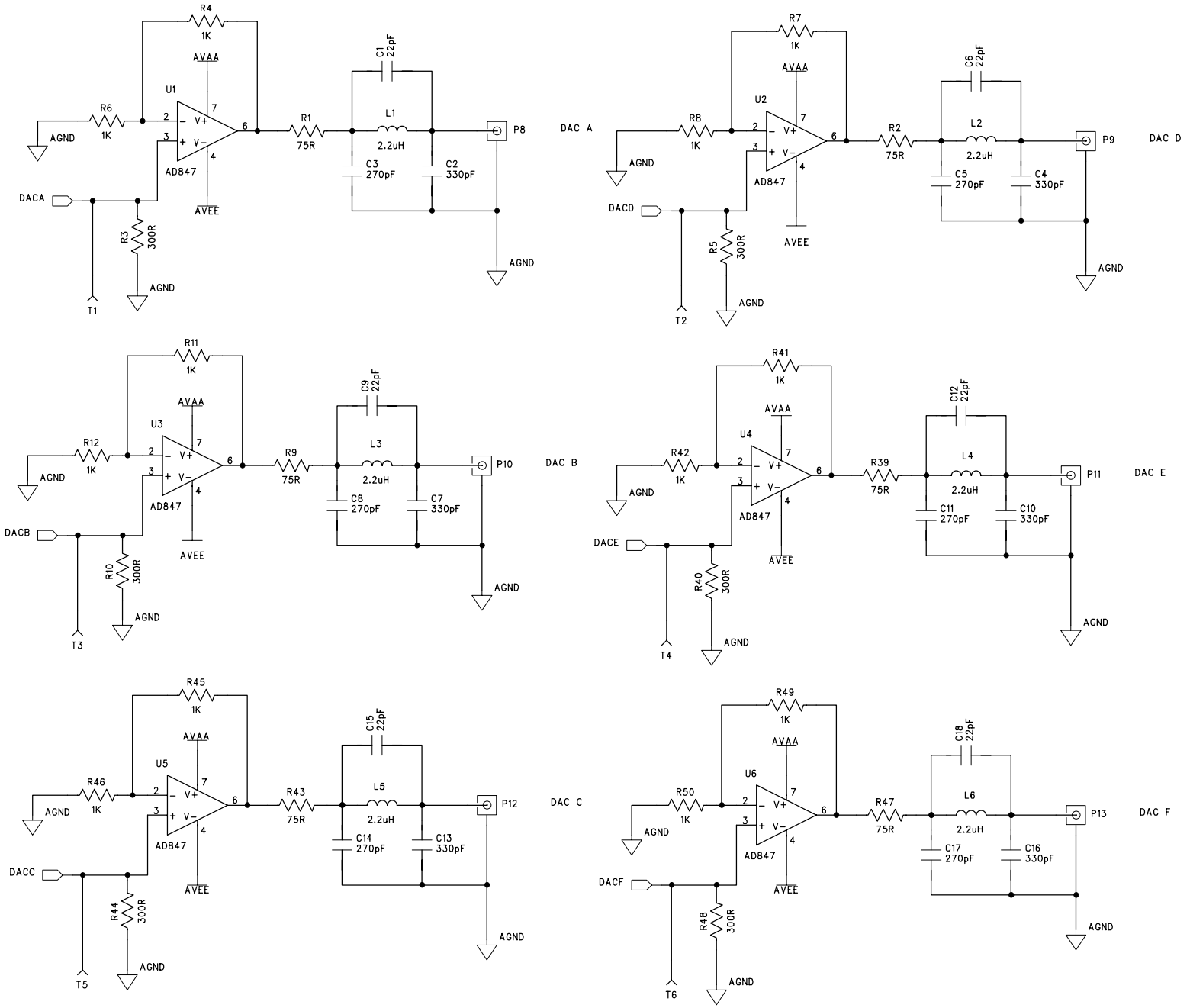
SHEET 1



ADV7194 EVALUATION BOARD
SHEET 4 OUTPUT
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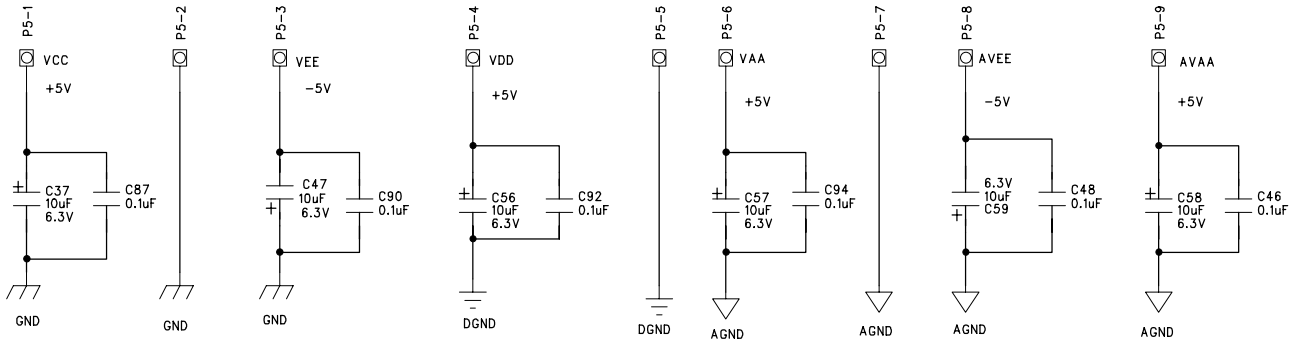
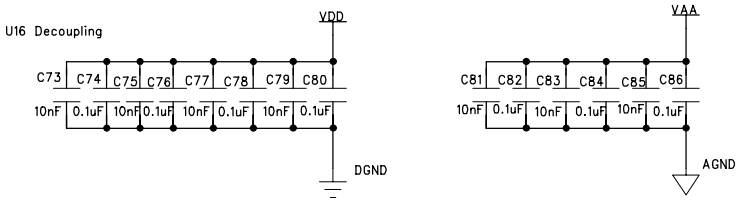
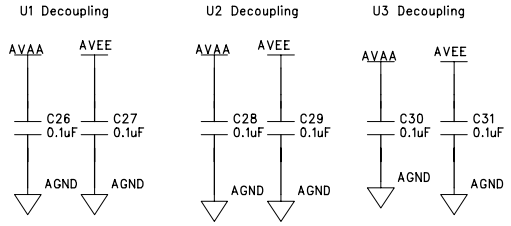
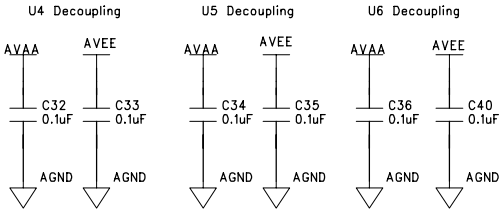
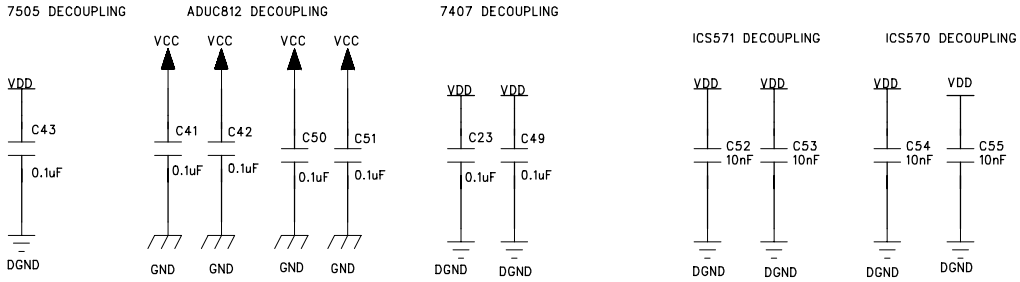
POWER CONNECTIONS











ADV7194 EVALUATION BOARD

SHEET 5 POWER AND DECOUPLING

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