ANALOG DEVICES

# Three Phase Energy Metering IC with Pulse Output

## Preliminary Technical Data

## ADE7752*

### FEATURES

**High Accuracy, Supports 50 Hz/60 Hz IEC 687/1036 Less than 0.1% Error Over a Dynamic Range of 500 to 1**
**Compatible with 3-phase/3-wire and 3-phase/4-wire configurations**
**The ADE7752 Supplies Average Real Power on the Frequency Outputs F1 and F2**
**The High Frequency Output CF Is Intended for Calibration and Supplies *Instantaneous Real Power***
**The Logic Output REVP indicates a Potential Miswiring or Negative Power for each phase**
**Direct Drive for Electromechanical Counters and Two Phase Stepper Motors (F1 and F2)**
**Proprietary ADCs and DSP Provide High Accuracy over Large Variations in Environmental Conditions and Time**
**On-Chip Power Supply Monitoring**
**On-Chip Creep Protection (No Load Threshold)**
**On-Chip Reference 2.5 V ± 8% (30 ppm/8C Typical) with External Overdrive Capability**
**Single 5 V Supply, Low Power (15 mW Typical)**
**Low Cost CMOS Process**

### GENERAL DESCRIPTION

The ADE7752 is a high accuracy three phase electrical energy measurement IC. The part specifications surpass the accuracy requirements as quoted in the IEC1036 standard. The only analog circuitry used in the ADE7752 is in the ADCs and reference circuit. All other signal processing (e.g., multiplication, filtering and summation) is carried out in the digital domain. This approach provides superior stability and accuracy over extremes in environmental conditions and over time.

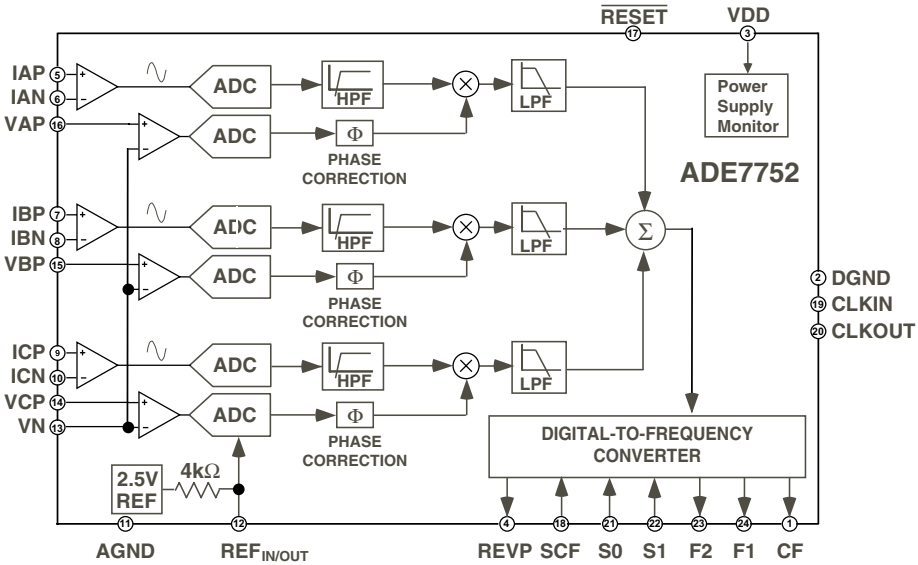
The ADE7752 supplies average real power information on the low frequency outputs F1 and F2. These logic outputs may be used to directly drive an electromechanical counter or interface with an MCU. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes, or as interface with an MCU.

The ADE7752 includes a power supply monitoring circuit on the $AV_{DD}$ supply pin. The ADE7752 will remain inactive until the supply voltage on $V_{DD}$ reaches 4 V. If the supply falls below 4 V, the ADE7752 will also be reset and no pulses will be issued on F1, F2 and CF.

Internal phase matching circuitry ensures that the voltage and current channels are phase matched. An internal no-load threshold ensures that the ADE7752 does not exhibit any creep when there is no load.

The ADE7752 is available in 24-lead SOIC packages.

### FUNCTIONAL BLOCK DIAGRAM




*Patents pending

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# ADE7752–SPECIFICATIONS

($V_{DD}$ = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, CLKIN = 10 MHz, $T_{MIN}$ to $T_{MAX}$ = –40°C to +85°C)

| Parameter | | Units | Test Conditions/Comments |
|---|---|---|---|
| ACCURACY[1,2] | | | |
| Measurement Error[1] on Current Channel | | | Voltage Channel with Full-Scale Signal (±500 mV), +25°C |
| | 0.1 | % Reading typ | Over a Dynamic Range 500 to 1 |
| Phase Error[1] Between Channels | | | Line Frequency = 45 Hz to 65 Hz |
| (PF = 0.8 Capacitive) | ±0.1 | Degrees(°) max | |
| (PF = 0.5 Inductive) | ±0.1 | Degrees(°) max | |
| AC Power Supply Rejection[1] | | | S0 = S1 = 1 |
| Output Frequency Variation (CF) | 0.01 | % Reading typ | V1 = 100 mV rms, V2 = 100 mV rms, @ 50 Hz Ripple on $V_{DD}$ of 200 mV rms @ 100 Hz |
| DC Power Supply Rejection[1] | | | S0 = S1 = 1 |
| Output Frequency Variation (CF) | 0.01 | % Reading typ | V1 = 100 mV rms, V2 = 100 mV rms, $V_{DD}$ = 5 V ± 250 mV |
| ANALOG INPUTS | | | See Analog Inputs Section |
| Maximum Signal Levels | ±0.125 | V max | VAP, VBP, VCP, VN, IAP, IAN, IBP, IBN, ICP and ICN to AGND |
| Input Impedance (DC) | 400 | kΩ min | CLKIN = 10 MHz |
| Bandwidth (–3 dB) | TBD | kHz typ | CLKIN/256, CLKIN = 10 MHz |
| ADC Offset Error[1,2] | ±15 | mV max | See Terminology and |
| Gain Error[1] | ±4 | % Ideal typ | External 2.5 V Reference, V1 = 125 mV dc, V2 = 125 mV dc |
| Gain Error Match[1] | ±0.2 | % Ideal typ | External 2.5 V Reference |
| REFERENCE INPUT | | | |
| $REF_{IN/OUT}$ Input Voltage Range | 2.7 | V max | 2.5 V + 8% |
| | 2.3 | V min | 2.5 V – 8% |
| Input Impedance | 3.7 | kΩ min | |
| Input Capacitance | 10 | pF max | |
| ON-CHIP REFERENCE | | | Nominal 2.5 V |
| Reference Error | ±200 | mV max | |
| Temperature Coefficient | 30 | ppm/°C typ | |
| CLKIN | | | Note All Specifications for CLKIN of 10 MHz |
| Input Clock Frequency | 15 | MHz max | |
| | 5 | MHz min | |
| LOGIC INPUTS[3] | | | |
| SCF, S0, S1, and $\overline{RESET}$ | | | |
| Input High Voltage, $V_{INH}$ | 2.4 | V min | $V_{DD}$ = 5 V ± 5% |
| Input Low Voltage, $V_{INL}$ | 0.8 | V max | $V_{DD}$ = 5 V ± 5% |
| Input Current, $I_{IN}$ | ±3 | μA max | Typically 10 nA, $V_{IN}$ = 0 V to $V_{DD}$ |
| Input Capacitance, $C_{IN}$ | 10 | pF max | |
| LOGIC OUTPUTS[3] | | | |
| F1 and F2 | | | |
| Output High Voltage, $V_{OH}$ | | | $I_{SOURCE}$ = 10 mA |
| | 4.5 | V min | $V_{DD}$ = 5 V |
| Output Low Voltage, $V_{OL}$ | | | $I_{SINK}$ = 10 mA |
| | 0.5 | V max | $V_{DD}$ = 5 V |
| CF and REVP | | | |
| Output High Voltage, $V_{OH}$ | 4 | V min | $V_{DD}$ = 5 V, $I_{SOURCE}$ = 5 mA |
| Output Low Voltage, $V_{OL}$ | 0.5 | V max | $V_{DD}$ = 5 V, $I_{SINK}$ = 5 mA |
| POWER SUPPLY | | | For Specified Performance |
| $V_{DD}$ | 4.75 | V min | 5 V – 5% |
| | 5.25 | V max | 5 V + 5% |
| $I_{DD}$ | 4 | mA typ | |

NOTES

[1] See Terminology Section for explanation of specifications.

[2] See Plots in Typical Performance Graphs.

[3] Sample tested during initial release and after any redesign or process change that may affect this parameter.

Specifications subject to change without notice.

## TIMING CHARACTERISTICS[1, 2] ($V_{DD}$ = 5 V ± 5%, AGND = DGND = 0 V, On-Chip Reference, CLKIN = 10 MHz, $T_{MIN}$ to $T_{MAX}$ = –40°C to +85°C)

| Parameter | | Units | Test Conditions/Comments |
|---|---|---|---|
| $t_1$[3] | 275 | ms | F1 and F2 Pulsewidth (Logic High) |
| $t_2$ | See Table III | sec | Output Pulse Period. See Transfer Function Section |
| $t_3$ | 1/2 $t_2$ | sec | Time Between F1 Falling Edge and F2 Falling Edge |
| $t_4$[3, 4] | 90 | ms | CF Pulsewidth (Logic High) |
| $t_5$ | See Table IV | sec | CF Pulse Period. See Transfer Function Section |
| $t_6$ | CLKIN/4 | sec | Minimum Time Between F1 and F2 Pulse |

NOTES
[1]Sample tested during initial release and after any redesign or process change that may affect this parameter.
[2]See Figure 1.
[3]The pulsewidths of F1, F2 and CF are not fixed for higher output frequencies. See Frequency Outputs Section.
[4]The CF pulse is always 1 µs in the high frequency mode. See Frequency Outputs section and Table IV.

Specifications subject to change without notice.

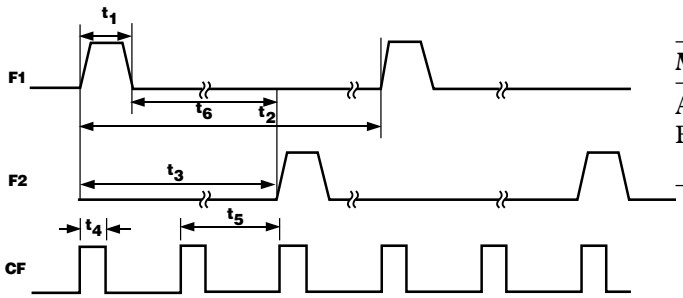



*Figure 1. Timing Diagram for Frequency Outputs*

**ORDERING GUIDE**

| Model | Package Description | Package Option |
|---|---|---|
| ADE7752AR | SOIC Package | R-24 |
| EVAL-ADE7752EB | ADE7752 Evaluation Board | |

**ABSOLUTE MAXIMUM RATINGS***

($T_A$ = +25°C unless otherwise noted)

$V_{DD}$ to AGND ..... –0.3 V to +7 V
$V_{DD}$ to DGND ..... –0.3 V to +7 V
Analog Input Voltage to AGND
VAP, VBP, VCP, VN, IAP, IAN, .....
IBP, IBN, ICP and ICN ..... –6 V to +6 V
Reference Input Voltage to AGND –0.3 V to $V_{DD}$ + 0.3 V
Digital Input Voltage to DGND . –0.3 V to $V_{DD}$ + 0.3 V
Digital Output Voltage to DGND –0.3 V to $V_{DD}$ + 0.3 V
Operating Temperature Range
Industrial ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Junction Temperature ..... +150°C
24-Lead SOIC, Power Dissipation ..... TBD mW
$\theta_{JA}$ Thermal Impedance ..... 250 °C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADE7752 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.


## TERMINOLOGY

### MEASUREMENT ERROR

The error associated with the energy measurement made by the ADE7752 is defined by the following formula:

$$Percentage\ Error = \frac{\text{Energy Registered by the ADE7752} - \text{True Energy}}{\text{True Energy}} \times 100\%$$

### PHASE ERROR BETWEEN CHANNELS

The HPF (High Pass Filter) in the current channel has a phase lead response. To offset this phase response and equalize the phase response between channels a phase correction network is also placed in the current channel. The phase correction network ensures a phase match between the current channels and voltage channels to within ±0.1° over a range of 45Hz to 65Hz and ±0.2° over a range 40Hz to 1kHz. This phase mismatch between the voltage and the current channels can be further reduced with the phase calibration register in each phase.
See Figures 18 and 19.

### POWER SUPPLY REJECTION

This quantifies the ADE7752 measurement error as a percentage of reading when the power supplies are varied.

For the ac PSR measurement a reading at nominal supplies (5 V) is taken. A 200 mV rms/100 Hz signal is then introduced onto the supplies and a second reading obtained under the same input signal levels. Any error introduced is expressed as a percentage of reading—see *Measurement Error definition*.

For the dc PSR measurement a reading at nominal supplies (5 V) is taken. The supply is then varied ±5% and a second reading is obtained with the same input signal levels. Any error introduced is again expressed as a percentage of reading.

### ADC OFFSET ERROR

This refers to the dc offset associated with the analog inputs to the ADCs. It means that with the analog inputs connected to AGND the ADCs still see an analog input signal of 1 mV to 10 mV, depending on gain setting. However, as the HPF is always present, the offset is removed from the current channel and the power calculation is not affected by this offset.

### GAIN ERROR

The gain error of the ADE7752 is defined as the difference between the measured output frequency (minus the offset) and the ideal output frequency. The difference is expressed as a percentage of the ideal frequency. The ideal frequency is obtained from the ADE7752 transfer function—see *Transfer Function section*.

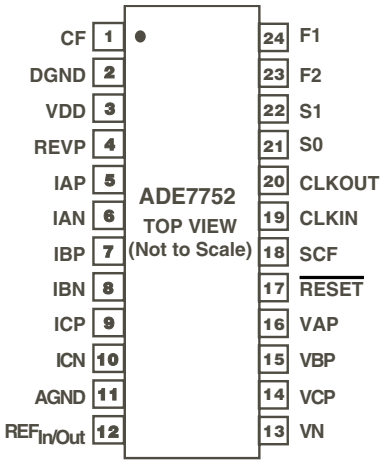
**PIN FUNCTION DESCRIPTION**

| Pin No. | MNEMONIC | DESCRIPTION |
|---|---|---|
| 1 | CF | Calibration Frequency Logic Output. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes. Also see SCF pin description. |
| 2 | DGND | This provides the ground reference for the digital circuitry in the ADE7752, i.e. multiplier, filters and digital-to-frequency converter. Because the digital return currents in the ADE7752 are small, it is acceptable to connect this pin to the analog ground plane of the whole system - see *Applications Information*. However high bus capacitance on the DOUT pin may result in noisy digital current which could affect performance. |
| **3** | $V_{DD}$ | Power supply. This pin provides the supply voltage for the digital circuitry in the ADE7752. The supply voltage should be maintained at 5V ± 5% for specified operation. This pin should be decoupled to DGND with a 10µF capacitor in parallel with a ceramic 100nF capacitor. |
| 4 | REVP | This logic output will go logic high when negative power is detected on any of the three phase inputs, i.e., when the phase angle between the voltage and the current signals is greater that 90°. This output is not latched and will be reset when positive power is once again detected. The output will go high or low at the same time as a pulse is issued on CF. |
| 5,6;<br>7,8;<br>9,10 | $I_{AP}$, $I_{AN}$;<br>$I_{BP}$, $I_{BN}$;<br>$I_{CP}$, $I_{CN}$ | Analog inputs for current channel. This channel is intended for use with the current transducer and is referenced in this document as the current channel. These inputs are fully differential voltage inputs with maximum differential input signal levels of ±0.125V -See *Analog Inputs*. Both inputs have internal ESD protection circuitry, and in addition an overvoltage of ±6V can be sustained on these inputs without risk of perma nent damage. |
| 11 | AGND | This pin provides the ground reference for the analog circuitry in the ADE7754, i.e. ADCs, temperature sensor, and reference. This pin should be tied to the analog ground plane or the quietest ground reference in the system. This quiet ground reference should be used for all analog circuitry, e.g. anti aliasing filters, current and voltage transducers etc. In order to keep ground noise around the ADE7754 to a minimum, the quiet ground plane should only connected to the digital ground plane at one point. It is acceptable to place the entire device on the analog ground plane - see *Applications Information.* |
| 12 | $REF_{IN/OUT}$ | This pin provides access to the on-chip voltage reference. The on-chip reference has a nominal value of 2.5V ± 8% and a typical temperature coefficient of 30ppm/°C. An external reference source may also be connected at this pin. In either case this pin should be decoupled to AGND with a 1µF ceramic capacitor. |
| 13-16 | $V_N$,$V_{CP}$,<br>$V_{BP}$, $V_{AP}$ | Analog inputs for the voltage channel. This channel is intended for use with the voltage transducer and is referenced as the voltage channel in this document. These inputs are single-ended voltage inputs with maximum signal level of ±0.125V with respect to $V_N$ for specified operation. All inputs have internal ESD protection circuitry, and in addi tion an over voltage of ±6V can be sustained on these inputs without risk of permanent damage. |
| 17 | $\overline{\text{RESET}}$ | Reset pin for the ADE7752. A logic low on this pin will hold the ADCs and digital circuitry (including the Serial Interface) in a reset condition. |
| 18 | SCF | Select Calibration Frequency. This logic input is used to select the frequency on the calibration output CF. Table IV shows how the calibration frequencies are selected. |

| Pin No. | MNEMONIC | DESCRIPTION |
|---|---|---|
| 19 | CLKIN | Master clock for ADCs and digital signal processing. An external clock can be provided at this logic input. Alternatively, a parallel resonant AT crystal can be connected across CLKIN and CLKOUT to provide a clock source for the ADE7752. The clock frequency for specified operation is 10MHz. Ceramic load capacitors of between 22pF and 33pF should be used with the gate oscillator circuit. Refer to crystal manufacturers data sheet for load capacitance requirements |
| 20 | CLKOUT | A crystal can be connected across this pin and CLKIN as described above to provide a clock source for the ADE7752. The CLKOUT pin can drive one CMOS load when either an external clock is supplied at CLKIN or a crystal is being used. |
| 21, 22 | S0, S1 | These logic inputs are used to select one of four possible frequencies for the digital-to-frequency conversion. This offers the designer greater flexibility when designing the energy meter. See Selecting a Frequency for an Energy Meter Application section. |
| 23, 24 | F2, F1 | Low Frequency Logic Outputs. F1 and F2 supply *average real power* information. The logic outputs can be used to directly drive electromechanical counters and two phase stepper motors. See Transfer Function section. |

**PIN CONFIGURATION**

SOIC Package



**Meter connections**

In three phase service, two main power distribution services exist: 3-phase 4-wire or 3-phase 3-wire. The additional wire in the 3-phase 4-wire arrangement is the Neutral wire. The voltage lines have a phase difference of ±120° (± 2π/3 radians) between each other - See Equation 5.

$$V_A(t) = \sqrt{2} \cdot V_A \cdot \cos(\omega_l t) \quad ; \quad V_B(t) = \sqrt{2} \cdot V_B \cdot \cos(\omega_l t + \frac{2\pi}{3}) \quad (5)$$
$$V_C(t) = \sqrt{2} \cdot V_C \cdot \cos(\omega_l t + \frac{4\pi}{3})$$

Where: $V_A$, $V_B$ and $V_C$ represent the voltage RMS value of the different phases

The current inputs are represented by Equations 6,

$$I_A(t) = \sqrt{2} \cdot I_A \cdot \cos(\omega_l t + \varphi_A) \quad ; \quad I_B(t) = \sqrt{2} \cdot I_B \cdot \cos(\omega_l t + \frac{2\pi}{3} + \varphi_B) \quad (6)$$
$$I_C(t) = \sqrt{2} \cdot I_C \cdot \cos(\omega_l t + \frac{4\pi}{3} + \varphi_C)$$

Where: $I_A$, $I_B$ and $I_C$ represent the RMS value of the current of each phase and $\phi_A$, $\phi_B$ and $\phi_C$ the phase difference of the current and voltage channel of each phase.

The instantaneous powers can then be calculated as follows:

$$P_A(t) = V_A(t) \cdot I_A(t)$$
$$P_B(t) = V_B(t) \cdot I_B(t)$$
$$P_C(t) = V_C(t) \cdot I_C(t)$$

Then,

$$P_A(t) = V_A \cdot I_A \cdot \cos(\varphi_A) - V_A \cdot I_A \cdot \cos(2\omega_l t + \varphi_A)$$
$$P_B(t) = V_B \cdot I_B \cdot \cos(\varphi_B) - V_B \cdot I_B \cdot \cos(2\omega_l t + \frac{4\pi}{3} + \varphi_B) \quad (7)$$
$$P_C(t) = V_C \cdot I_C \cdot \cos(\varphi_C) - V_C \cdot I_C \cdot \cos(2\omega_l t + \frac{8\pi}{3} + \varphi_C)$$

As can be seen from Equation 7, in the ADE7752 the real power calculation per phase is made when current and voltage inputs of the one phase are connected to the same channel (A, B or C). Then, the summation of each individual real power calculation gives the total Real Power information. P(t) = $P_A(t)$ + $P_B(t)$ + $P_C(t)$

Figure 14 demonstrates the connections of the analog inputs of the ADE7752 with the power lines in a 3-phase 3-wire Delta service.

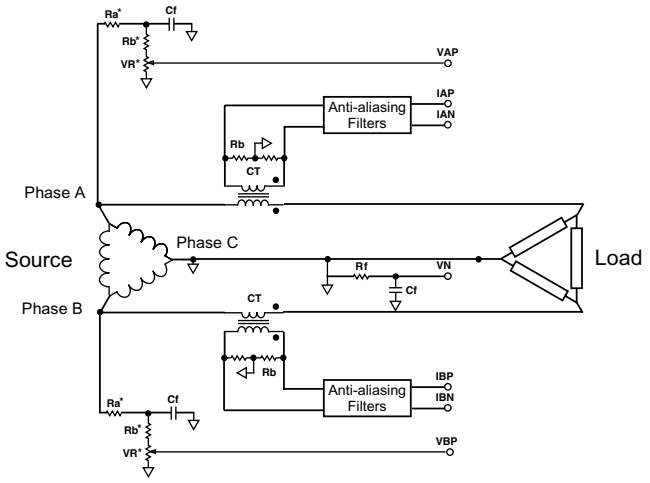



*Figure 14 - 3-phase 3-wire meter connection with ADE7752*

Note: Only 2 current inputs and 2 voltage inputs of the ADE7752 are used in this case. The Real power calculated by the ADE7752 does not depend on the selected channel.

Figure 15 demonstrates the connections of the analog inputs of the ADE7752 with the power lines in a 3-phase 4-wire Wye service.

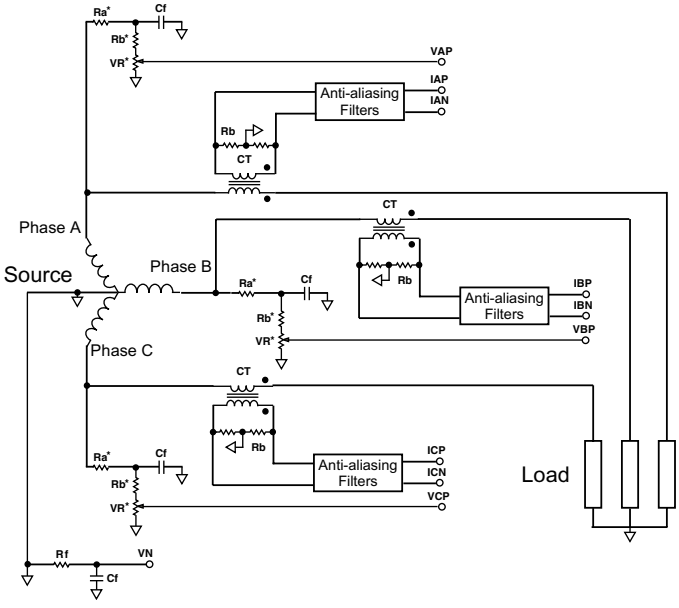



*Figure 15 - 3-phase 4-wire meter connection with ADE7752*

## TRANSFER FUNCTION

### Frequency Outputs F1 and F2

The ADE7752 calculates the product of six voltage signals (on Current channel and Voltage channel) and then low-pass filters this product to extract real power information. This real power information is then converted to a frequency. The frequency information is output on F1 and F2 in the form of active high pulses. The pulse rate at these outputs is relatively low, e.g., 0.08 Hz maximum for AC signals with SCF = S0 = S1 = 1—see Table III. This means that the frequency at these outputs is generated from real power information accumulated over a relatively long period of time. The result is an output frequency that is proportional to the average real power. The averaging of the real power signal is implicit to the digital-to-frequency conversion. The output frequency or pulse rate is related to the input voltage signals by the following equation.

$$Freq = \frac{109.2 \times (V_{AN} \times I_A + V_{BN} \times I_B + V_{CN} \times I_C) \times F_{1-5}}{V_{REF}^2}$$

where:

*Freq* = Output frequency on F1 and F2 *(Hz)*

$V_{AN}$, $V_{BN}$ *and* $V_{CN}$ = Differential rms voltage signal on Voltage channels (volts)

$I_A$, $I_B$ *and* $I_C$ = Differential rms voltage signal on Current channels (volts)

$V_{REF}$ = The reference voltage (2.5 V ± 8%) (volts)

$F_{1-5}$ = One of five possible frequencies selected by using the logic inputs SCF, S0 and S1—see Table II.

**Table II. $F_{1-5}$ Frequency Selection**

| SCF | S1 | S0 | $F_{1-5}$ (Hz) | XTAL/CLKIN* |
|---|---|---|---|---|
| 1 | 1 | 1 | 0.596 | 10 MHz/$2^{24}$ |
| 0 | 1 | 1 | 76.3 | 10 MHz/$2^{17}$ |
| - | 1 | 0 | 19.07 | 10 MHz/$2^{19}$ |
| - | 0 | 1 | 4.77 | 10 MHz/$2^{21}$ |
| - | 0 | 0 | 1.19 | 10 MHz/$2^{23}$ |

NOTE

*$F_{1-5}$ is a binary fraction of the master clock and therefore will vary if the specified CLKIN frequency is altered.

**Example 1**

Thus if full-scale differential DC voltages of +125 mV and –125 mV are applied to VA, VB, VC, IA, IB and IC respectively (125 mV is the maximum differential voltage that can be connected to Current and Voltage channels), the expected output frequency is calculated as follows:

$F_{1-5}$ = 0.596 Hz, *SCF* = *S*0 = *S*1 = 1

$V_{AN} = V_{BN} = V_{CN}$ = IA = IB = IC

= +125 mV dc = 0.125 V (rms of dc = dc)

$V_{REF}$ = 2.5 V (nominal reference value).

NOTE: If the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = 3 \times \frac{109.2 \times 0.125 \times 0.125 \times 0.596}{2.5^2} = 0.488\ Hz$$

**Example 2**

In this example, with AC voltages of ±500 mV peak applied to the Voltage channels and Current channels, the expected output frequency is calculated as follows:

$F_{1-5}$ = 0.596 Hz, *SCF* = *S*0 = *S*1 = 1

$V_{AN} = V_{BN} = V_{CN}$ = IA = IB = IC

= 125 mV peak AC = $0.125/\sqrt{2}$ volts rms

$V_{REF}$ = 2.5 V (nominal reference value).

NOTE: If the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = 3 \times \frac{109.2 \times 0.125 \times 0.125 \times 0.596}{\sqrt{2} \times \sqrt{2} \times 2.5^2} = 0.24\ Hz$$

As can be seen from these two example calculations, the maximum output frequency for AC inputs is always half of that for DC input signals. The maximum frequency depends also on the number of phases connected to the ADE7752. In a 3-phase 3-wire delta service the maximum output frequency is different from the maximum output frequency in a 3-phase 4-wire Wye service. The reason is that there are only 2 phases connected to the analog inputs but also that in a delta service, the Current channel input and Voltage channel input of the same phase are not in phase in normal operation.

**Example 3**

In this example, the ADE7752 is connected to a 3-phase 3-wire delta service as shown in Figure 14. The total real energy calculation processed in the ADE7752 can be expressed as:

$$Total\ \text{Re}al\ Energy = (V_A - V_C) \times I_A + (V_B - V_C) \times I_B$$

Where $V_A$, $V_B$ and $V_C$ represent respectively the voltage on phase A, B and C. $I_A$ and $I_B$ represent respectively the current on phase A and B.

As the voltage and current inputs respect Equations 5 and 6, the Total Real Energy (P) is:

$$P = (VA - VC) \times (IAP - IAN) + (VB - VC) \times (IBP - IBN)$$

$$P = \left(\sqrt{2} \cdot V_A \cdot \cos(\omega_l t) - \sqrt{2} \cdot V_C \cdot \cos\left(\omega_l t + \frac{4\pi}{3}\right)\right) \cdot \sqrt{2} \cdot I_A \cdot \cos(\omega_l t) + \left(\sqrt{2} \cdot V_B \cdot \cos\left(\omega_l t + \frac{2\pi}{3}\right) - \sqrt{2} \cdot V_C \cdot \cos\left(\omega_l t + \frac{4\pi}{3}\right)\right) \cdot \sqrt{2} \cdot I_B \cdot \cos\left(\omega_l t + \frac{2\pi}{3}\right)$$

For simplification, we assume that $\phi_A = \phi_B = \phi_C = 0$ and $V_A = V_B = V_C = V$. The equation above becomes:

$$P = 2 \cdot V \cdot I_A \cdot \sin\left(\frac{2\pi}{3}\right) \cdot \sin\left(\omega_l t + \frac{2\pi}{3}\right) \cdot \cos(\omega_l t) + 2 \cdot V \cdot I_B \cdot \sin\left(\frac{\pi}{3}\right) \cdot \sin(\omega_l t + \pi) \cdot \cos\left(\omega_l t + \frac{2\pi}{3}\right) \quad (9)$$

P then becomes:

$$P = V_{AN} \cdot I_A \cdot \left(\sin\left(\frac{2\pi}{3}\right) + \sin\left(2\omega_l t + \frac{2\pi}{3}\right)\right) + V_{BN} \cdot I_B \cdot \left(\sin\left(\frac{\pi}{3}\right) + \sin\left(2\omega_l t + \frac{\pi}{3}\right)\right) \quad (10)$$

Where:

$V_{AN} = V \cdot \sin(2\pi/3)$ represents the RMS voltage between VAP and VN pins of the ADE7752

$V_{BN} = V \cdot \sin(\pi/3)$ represents the RMS voltage between VBP and VN pins of the ADE7752.

As the LPF on each channel eliminates the $2\omega_l$ component of the equation, the Real power measured by the ADE7752 is:

$$P = V_{AN} \cdot I_A \cdot \frac{\sqrt{3}}{2} + V_{BN} \cdot I_B \cdot \frac{\sqrt{3}}{2}$$

Where:

$V_{AN}$ and $V_{BN}$ are the voltage RMS at the voltage inputs of the ADE7752 after voltage sensing

$I_A$ and $I_B$ are the voltage RMS at the current input of the ADE7752 after current sensing

If full scale AC voltage of ±125 mV peak are applied to the Voltage channels and Current channels, the expected output frequency is calculated as follows:

$F_{1-5}$ = 0.596 Hz, $SCF = S0 = S1 = 1$

VAN = VBN = IA = IB

= 125 mV peak AC = $0.125/\sqrt{2}$ volts rms

VCN = IC = 0

$V_{REF}$ = 2.5 V (nominal reference value).

NOTE: If the on-chip reference is used, actual output frequencies may vary from device to device due to reference tolerance of ±8%.

$$Freq = 2 \times \frac{109.2 \times 0.125 \times 0.125 \times 0.596}{\sqrt{2} \times \sqrt{2} \times 2.5^2} \times \frac{\sqrt{3}}{2} = 0.14$$

Table III shows a complete listing of all maximum output frequencies when using all three channels inputs.

**Table III. Maximum Output Frequency on F1 and F2**

| SCF | S1 | S0 | Max Frequency for DC Inputs (Hz) | Max Frequency for AC Inputs (Hz) |
|---|---|---|---|---|
| 1 | 1 | 1 | 0.48 | 0.24 |
| 0 | 1 | 1 | 62.52 | 31.26 |
| - | 1 | 0 | 15.6 | 7.8 |
| - | 0 | 1 | 3.9 | 1.95 |
| - | 0 | 0 | 0.96 | 0.48 |

**Frequency Output CF**

The pulse output CF (Calibration Frequency) is intended for use during calibration. The output pulse rate on CF can be up to 160 times the pulse rate on F1 and F2. The lower the $F_{1-5}$ frequency selected, the higher the CF scaling. Table IV shows how the two frequencies are related, depending on the states of the logic inputs S0, S1 and SCF. Because of its relatively high pulse rate, the frequency at this logic output is proportional to the instantaneous real power. As is the case with F1 and F2, the frequency is derived from the output of the low-pass filter after multiplication. However, because the output frequency is high, this real power information is accumulated over a much shorter time. Hence less averaging is carried out in the digital-to-frequency conversion. With much less averaging of the real power signal, the CF output is much more responsive to power fluctuations—see Signal Processing Block in Figure 8.

**Table IV. Maximum Output Frequency on CF**

| SCF | S1 | S0 | $F_{1-5}$ (Hz) | CF Max for AC Signals (Hz) |
|---|---|---|---|---|
| 0 | 0 | 0 | 1.19 | 160 x F1, F2 = 78.12 |
| 1 | 0 | 0 | 1.19 | 8 x F1, F2 = 3.90 |
| 0 | 0 | 1 | 4.77 | 160 x F1, F2 = 312.51 |
| 1 | 0 | 1 | 4.77 | 16 x F1, F2 = 31.26 |
| 0 | 1 | 0 | 19.07 | 16 x F1, F2 = 130.56 |
| 1 | 1 | 0 | 19.07 | 8 x F1, F2 = 62.49 |
| 0 | 1 | 1 | 76.29 | 8 x F1, F2 = 250 |
| 1 | 1 | 1 | 0.596 | 16 x F1, F2 = 3.90 Hz |

**Frequency Outputs**

Figure 1 shows a timing diagram for the various frequency outputs. The outputs F1 and F2 are the low frequency outputs that can be used to directly drive a stepper motor or electromechanical impulse counter. The F1 and F2 outputs provide two alternating high going pulses. The pulsewidth ($t_1$) is set at 275 ms and the time between the rising edges of F1 and F2 ($t_3$) is approximately half the period of F1 ($t_2$). If however the period of F1 and F2 falls below 550 ms (1.81 Hz) the pulsewidth of F1 and F2 is set to half of their period. The maximum output frequencies for F1 and F2 are shown in Table III.

The high frequency CF output is intended to be used for communications and calibration purposes. CF produces a 90 ms-wide active high pulse ($t_4$) at a frequency proportional to active power. The CF output frequencies are given in Table IV. As in the case of F1 and F2, if the period of CF ($t_5$) falls below 180 ms, the CF pulsewidth is set to half the period. For example, if the CF frequency is 20 Hz, the CF pulsewidth is 25 ms.

### NO LOAD THRESHOLD

The ADE7752 also includes a "no load threshold" and "start-up current" feature that will eliminate any creep effects in the meter. The ADE7752 is designed to issue a minimum output frequency. Any load generating a frequency lower than this minimum frequency will not cause a pulse to be issued on F1, F2 or CF. The minimum output frequency is given as 0.0007% of the full-scale output frequency for each of the $F_{1-5}$ frequency selections—see Table II. For example, an energy meter with a meter constant of 100 imp/kWhr on F1, F2 using $F_2$ (4.77 Hz), the minimum output frequency at F1 or F2 would be 0.0007% of 4.77 Hz or 33.3 x $10^{-6}$ Hz. This would be 533 x $10^{-6}$ Hz at CF (16 x F1 Hz). In this example the no load threshold would be equivalent to 1.2 W of load or a start-up current of 5.5 mA at 220 V.

### REVERSE POWER INFORMATION

The ADE7752 detects when the current and voltage channels of any of the three phase inputs have a phase difference greater than 90° i.e. $\Phi_A$ or $\Phi_B$ or $\Phi_C$ > 90°. This mechanism can detect wrong connection of the meter or generation of Active Energy.

The REVP pin output will go active high when negative power is detected on any of the three phase inputs. If positive Active Energy is detected on all the three phases, REVP pin output is Low. The REVP pin output changes state at the same time as a pulse is issued on CF. If several phases measure negative power, the REVP pin output will stay low until all the phases measure positive power.

### NOTE

For a complete datasheet of the ADE7752, please contact us on our website at:

**http://forms.analog.com/Form_Pages/energymeter/contact.asp**

### OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

**24-SOIC Outline Package**
**(AR-24)**