Industrial Current/Voltage Output Driver, Programmable Ranges

Preliminary Technical Data

AD5750

FEATURES

Current Output Ranges: 4–20mA, 0–20mA or 0–24mA, ±20ma, ±24ma
- **B Grade - 0.1% Total Unadjusted Error (TUE)**
- **A Grade - 0.3% Total Unadjusted Error (TUE)**
- **5ppm/°C Output Drift**

Voltage Output Ranges: 0-5V, 0-10V, ±5V, ±10V, 20% over-range
- **B Grade - 0.1% Total Unadjusted Error (TUE)**
- **A Grade - 0.3% Total Unadjusted Error (TUE)**

Flexible Serial Digital Interface
On-Chip Output Fault Detection
PEC Error Checking
Asynchronous CLEAR Function
Power Supply Range
- **AV_{DD} : = +12V to +24V (+/-10%)**
- **AV_{SS} : = -12V to -24V (+/-10%)**

Output Loop Compliance to AV_{DD} – 2.5 V
Temperature Range: -40°C to +105°C
LFCSP Packages

APPLICATIONS

Process Control
Actuator Control
PLC

GENERAL DESCRIPTION

The AD5750 is a single channel, low-cost, precision, voltage/current output driver with hardware or software programmable output ranges. The software ranges are configured via an SPI/Microwire compatible serial interface. The AD5750 targets applications in PLC and industrial process control. The analog input to the AD5750 is provided from a low voltage, single supply digital-to-analog converter and is internally conditioned to provide the desired output current/voltage range.
The output current range is programmable across five current ranges - 4–20mA, 0–20mA or 0–24mA, ±20ma and ±24ma.

Voltage output is provided from a separate pin that can be configured to provide 0V to 5V, 0V to 10V, ±5V or ±10V output ranges. An over-range of 20% is available on the voltage ranges.

Analog outputs are short and open circuit protected and can drive capacitive loads of 1uF and inductive loads of 0.1H. The device is specified to operate with a power supply range from ±12 V to ±24 V. Output loop compliance is 0 V to AV_{DD} – 2.5 V.

The flexible serial interface is SPI and MICROWIRE compatible and can be operated in 3-wire mode to minimize the digital isolation required in isolated applications. The interface also features an optional PEC error checking feature using CRC-8 error checking, useful in industrial environments where data communication corruption can occur.

The device also includes a power-on-reset function ensuring that the device powers up in a known state and an asynchronous CLEAR pin which sets the outputs to zero-scale / mid-scale voltage output or the low end of the selected current range.

A HW SELECT pin is used to configure the part for hardware or software mode on power up.

The total output error is typically ±0.1% in both current mode and voltage mode.

Table 1. Related Devices

Part Number	Description
AD5422	Single Channel, 16-Bit, Serial Input Current Source and Voltage Output DAC

Rev. PrC

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REVISION HISTORY

PrC – Preliminary Version. May 6, 2008

FUNCTIONAL BLOCK DIAGRAM

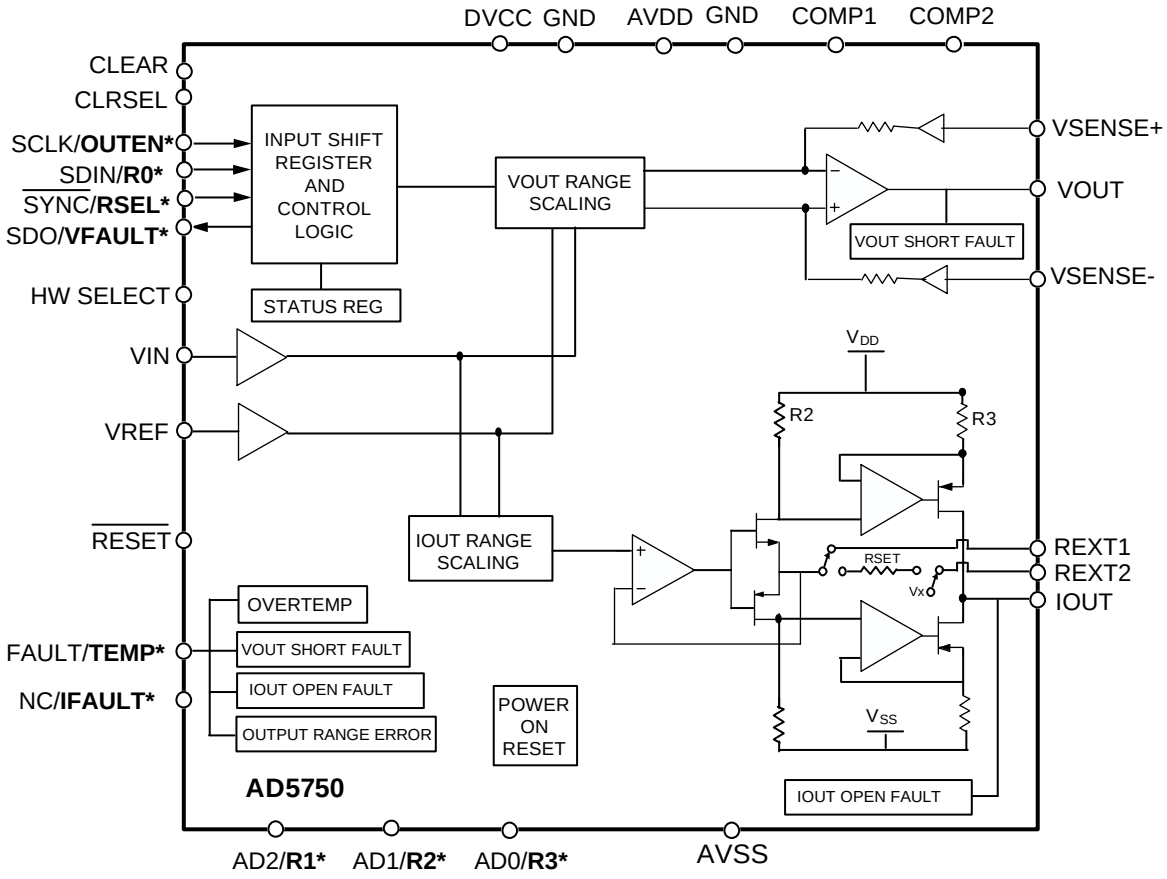


Figure 1. Functional Block Diagram

* Denotes shared pin. Software mode denoted by regular text, hardware mode denoted by **bold** text. E.G. for FAULT/**TEMP** pin, in software mode this pin will take on FAULT function. In Hardware mode, this pin will take on **TEMP** function.

SPECIFICATIONS

AV_{DD}/AV_{SS}=±12V (+/-10%) to ±24V (+/-10%) , DV_{CC} =2.7 V to 5.5 V, GND = 0 V. R_L = 2 kΩ, C_L = 200 pF, I_{OUT} : R_L = 300Ω, H_L = 50mH; All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B grade[1]	A grade[2]	Unit	Test Conditions/Comments
INPUT VOLTAGE RANGE	0 to 4.096	0 to 4.096	V	
Input Leakage Current	1	1	uA max	
VOLTAGE OUTPUT				
Output Voltage Ranges	0 to 5	0 to 5	V	
	0 to 10	0 to 10	V	AVDD needs to have minimum 1.1v headroom, or > +11.1v.
	-5 to +5	-5 to +5	V	
	-10 to +10	-10 to +10	V	AVDD/AVSS needs to have minimum 1.1v headroom, or > +/-11.1v.
ACCURACY				Output unloaded
Bipolar Output				
Total Unadjusted Error (TUE)	0.1	0.3	% FSR max	Over temperature and supplies.
Relative Accuracy (INL)	±0.02	±0.02	% FSR max	
Bipolar Zero Error	0.01	0.01	% FSR typ	Error at analog input = mid scale
Bipolar Zero TC	TBD	TBD	ppm % FSR max	
Offset Error	0.015	0.015	% FSR typ	Error at analog input = 10mv
Zero Scale Error	0.015	0.015	% FSR typ	Error at analog input = 0.0v
Zero Scale TC	TBD	TBD	ppm % FSR max	
Gain Error	0.005	0.005	% FSR typ	(Ideal Span – Measured Span)/Ideal Span
Gain Error TC	TBD	TBD	ppm % FSR max	
Full Scale Error	0.015	0.015	% FSR typ	Error at analog input = 4.096v (FS)
Full Scale Error TC	TBD	TBD	ppm % FSR max	
Unipolar Output				
Total Unadjusted Error (TUE)	0.1	0.1	% FSR max	Over temperature and supplies.
Relative Accuracy (INL)	±0.02	±0.02	% FSR max	
Offset Error	0.01	0.01	% FSR typ	Error at analog input = 10mv
Zero Scale Error	0.015	0.015	% FSR typ	Error at analog input = 0.0v
Zero Scale TC	TBD	TBD	ppm % FSR max	
Gain Error	0.003	0.003	% FSR typ	(Ideal Span – Measured Span)/Ideal Span
Gain Error TC	TBD	TBD	ppm % FSR max	
Full Scale Error	0.01	0.01	% FSR typ	Error at analog input = 4.096v (FS)
Full Scale Error TC	TBD	TBD	ppm % FSR max	
Output Voltage Over-Ranges	0 to 6	0 to 6	V	Programmable Over-Ranges. See Features Section.
	0 to 12	0 to 12	V	
	-6 to +6	-6 to +6	V	
	-12 to +12	-12 to +12	V	
Overrange Relative Accuracy (INL)	±0.02	±0.02	% FSR max	
OUTPUT CHARACTERISTICS				

Parameter	B grade[1]	A grade[2]	Unit	Test Conditions/Comments
Short-Circuit Current	15	15	mA max	
Load Conditions				
Resistance	1	1	K Ohm min	For Specified Performance
Capacitance Load Stability				
$R_L = \infty$	20	20	nF max	
$R_L = 2\ k\Omega$	TBD	TBD	nF max	
$R_L = \infty$	1	1	µF max	External compensation capacitor of 4nF connected.
0.1% Settling Time	10	10	Us	Specified with 200pF load
Slew Rate	1	1	V/µs typ	
Output Noise	TBD	TBD	µV rms max	0.1 Hz to 10 Hz Bandwidth
	80	80	µV rms max	100 kHz Bandwidth
Output Noise Spectral Density	100	100	nV/√Hz typ	Measured at 10KHz
DC Output Impedance	0.3	0.3	Ω typ	
DC PSRR	10	10	µV/V	
AC PSRR	TBD	TBD	dB	200mV 50/60Hz Sinewavesuperimposed on power supply voltage.
Power-On Glitch Energy	10	10	nV-sec typ	
CURRENT OUTPUT				
Output Current Ranges	0 to 24	0 to 24	mA	
	0 to 20	0 to 20	mA	
	4 to 20	4 to 20	mA	
	±20	±20	mA	
	±24	±24	mA	
ACCURACY				
Total Unadjusted Error (TUE)	±0.1	±0.3	% FSR max	With External Precision Resistor
TUE TC	±5	±5	ppm max	With External Precision Resistor
Bipolar Output				
Relative Accuracy (INL)	±0.02	±0.02	% FSR max	
Bipolar Zero Error	0.0325	0.0325	% FSR typ	Error at analog input = mid scale
Bipolar Zero TC	TBD	TBD	ppm % FSR max	
Offset Error	0.0175	0.0175	% FSR typ	Error at analog input = 10mv
Zero Scale Error	0.0175	0.0175	% FSR typ	Error at analog input = 0.0v
Zero Scale TC	TBD	TBD	ppm % FSR max	
Gain Error	0.01	0.01	% FSR typ	(Ideal Span – Measured Span)/Ideal Span
Gain Error TC	TBD	TBD	ppm % FSR max	
Full Scale Error	0.0125	0.0125	% FSR typ	Error at analog input = 4.096v (FS)
Full Scale Error TC	TBD	TBD	ppm % FSR max	
Unipolar Output				
Relative Accuracy (INL)	±0.02	±0.02	% FSR max	
Offset Error	0.01	0.01	% FSR typ	Error at analog input = 10mv
Zero Scale Error	0.01	0.01	% FSR typ	Error at analog input = 0.0v
Zero Scale TC	TBD	TBD	ppm % FSR max	
Gain Error	0.15	0.15	% FSR typ	(Ideal Span – Measured Span)/Ideal Span
Gain Error TC	TBD	TBD	ppm % FSR max	
Full Scale Error	0.01	0.01	% FSR typ	Error at analog input = 4.096v (FS)
Full Scale Error TC	TBD	TBD	ppm % FSR max	

Parameter	B grade[1]	A grade[2]	Unit	Test Conditions/Comments
Total Unadjusted Error (TUE)	±0.3	±0.3	% FSR max	With Internal Resistor
TUE TC	±20	±20	ppm typ	With Internal Resistor
	±50	±50	ppm max	
Bipolar Output				
Relative Accuracy (INL)	±0.02	±0.02	% FSR max	
Bipolar Zero Error	0.0325	0.0325	% FSR typ	Error at analog input = mid scale
Bipolar Zero TC	TBD	TBD	ppm % FSR max	
Offset Error	0.01	0.01	% FSR typ	Error at analog input = 10mv
Zero Scale Error	0.01	0.01	% FSR typ	Error at analog input = 0.0v
Zero Scale TC	TBD	TBD	ppm % FSR max	
Gain Error	0.003	0.003	% FSR typ	(Ideal Span – Measured Span)/Ideal Span
Gain Error TC	TBD	TBD	ppm % FSR max	
Full Scale Error	0.01	0.01	% FSR typ	Error at analog input = 4.096v (FS)
Full Scale Error TC	TBD	TBD	ppm % FSR max	
Unipolar Output				
Relative Accuracy (INL)	±0.02	±0.02	% FSR max	
Offset Error	0.01	0.01	% FSR typ	Error at analog input = 10mv
Zero Scale Error	0.01	0.01	% FSR typ	Error at analog input = 0.0v
Zero Scale TC	TBD	TBD	ppm % FSR max	
Gain Error	0.005	0.005	% FSR typ	(Ideal Span – Measured Span)/Ideal Span
Gain Error TC	TBD	TBD	ppm % FSR max	
Full Scale Error	0.01	0.01	% FSR typ	Error at analog input = 4.096v (FS)
Full Scale Error TC	TBD	TBD	ppm % FSR max	
CURRENT MODE OVERRANGES	0 to 24.5	0 to 24.5	mA	SEE FEATURES SECTION
	0 to 20.4	0 to 20.4	mA	SEE FEATURES SECTION
	4 to 20.4	4 to 20.4	mA	SEE FEATURES SECTION
OUTPUT CHARACTERISTICS				
Current Loop Compliance Voltage	AVDD – 2.5	AVDD – 2.5	V max	
Resistive Load	See Comment	See Comment	kΩ max	Chosen such that compliance is not exceeded.
Inductive Load	0.1	0.1	H max	
0.1% Settling Time	10	10	us	
DC PSRR	1	1	µA/V max	
Output Impedance	25	25	MΩ typ	
REFERENCE INPUT				
Reference Input				
Reference Input Voltage	4.096	4.096	V nom	±1% for specified performance
Input Leakage Current	1	1	uA max	
DIGITAL INPUTS				DV_{CC} = 2.7 V to 5.5 V, JEDEC compliant
V_{IH}, Input High Voltage	2	2	V min	
V_{IL}, Input Low Voltage	0.8	0.8	V max	
Input Current	±1	±1	µA max	Per pin
Pin Capacitance	10	10	pF typ	Per pin

Parameter	B grade[1]	A grade[2]	Unit	Test Conditions/Comments
DIGITAL OUTPUTS				
FAULT, IFAULT, TEMP, VFAULT				
V_{OL}, Output Low Voltage	0.4	0.4	V max	10kΩ pull-up resistor to DV_{CC}
V_{OL}, Output Low Voltage	0.6	0.6	V typ	@ 2.5 Ma
V_{OH}, Output High Voltage	3.6	3.6	V min	10kΩ pull-up resistor to DV_{CC}
SDO				
V_{OL}, Output Low Voltage	0.5	0.5	V max	Sinking 200ua
V_{OH}, Output High Voltage	DVCC-0.5	DVCC-0.5	V min	Sourcing 200ua
High Impedance Leakage current	±TBD	±TBD	ua max	
High Impedance Output Capacitance	20	20	pF max	
POWER REQUIREMENTS				
AV_{DD}	12 to 24	12 to 24	V min to V max	+/-10%
AV_{SS}	-12 to 24	-12 to 24	V min to V max	+/-10%
DV_{CC}				
Input Voltage	2.7 to 5.5	2.7 to 5.5	V min to V max	Internal supply disabled
AV_{DD}	TBD	TBD	mA	Output unloaded
AV_{SS}	TBD	TBD	mA	Output unloaded
DI_{CC}	TBD	TBD	mA max	$V_{IH} = DV_{CC}$, V_{IL} = GND, TBD mA typ
Power Dissipation	TBD	TBD	mW typ	

[1] Temperature range: -40°C to +105°C; typical at +25°C.
[2] Temperature range: -40°C to +105°C; typical at +25°C.

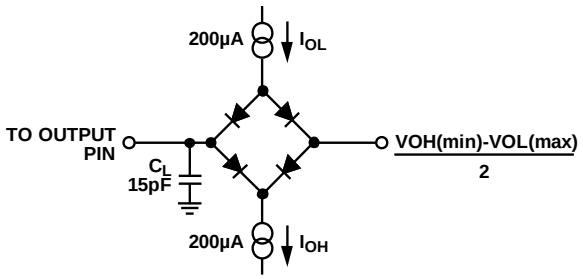
TIMING CHARACTERISTICS

AV_{DD}/AV_{SS}=±12V (+/-10%) to ±24V (+/-10%) , DV_{CC} =2.7 V to 5.5 V, GND = 0 V. R_L = 2 kΩ, C_L = 200 pF, I_{OUT} : R_L = 300Ω, H_L = 50mH; All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Limit at T_{MIN}, T_{MAX}	Unit	Description
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK high time
t_3	13	ns min	SCLK low time
t_4	13	ns min	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5	13	ns min	16th SCLK falling edge to $\overline{SYNC}$ rising edge
t_6	13	ns min	Minimum $\overline{SYNC}$ high time (WRITE MODE)
t_7	6	ns min	Data setup time
t_8	0	ns min	Data hold time
t_{10} , t_9	1	µs max	CLEAR pulse high/low activation time
t_{11}	25	ns min	Minimum $\overline{SYNC}$ high time (READ MODE)
t_{12}	25	ns max	SCLK rising edge to SDO valid (SDO CL=20pf)

1 Guaranteed by characterization. Not production tested.
2 All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.



SDO Load Timing.

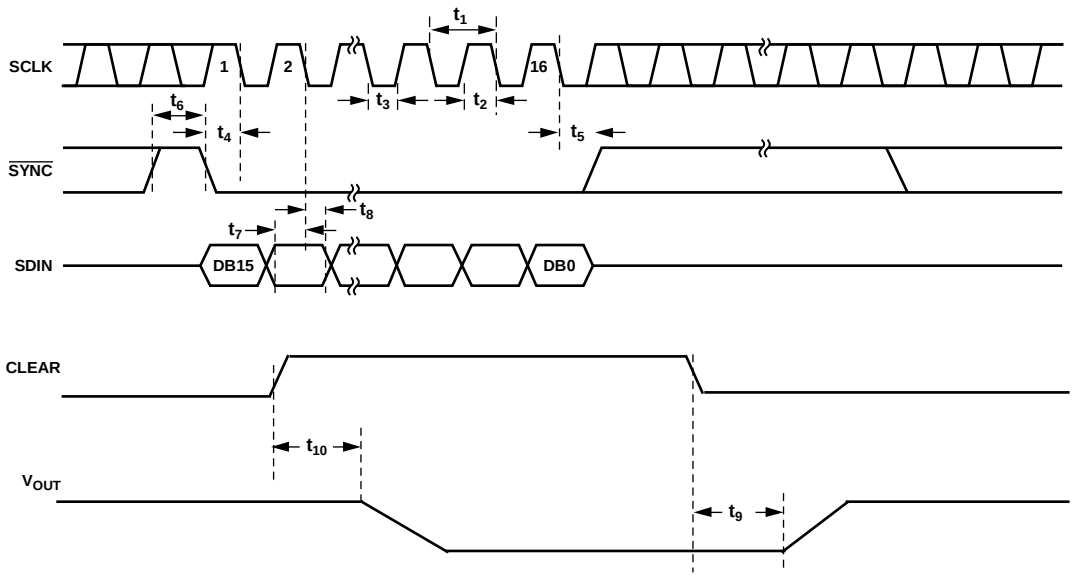


Figure 2. Write Mode Timing Diagram

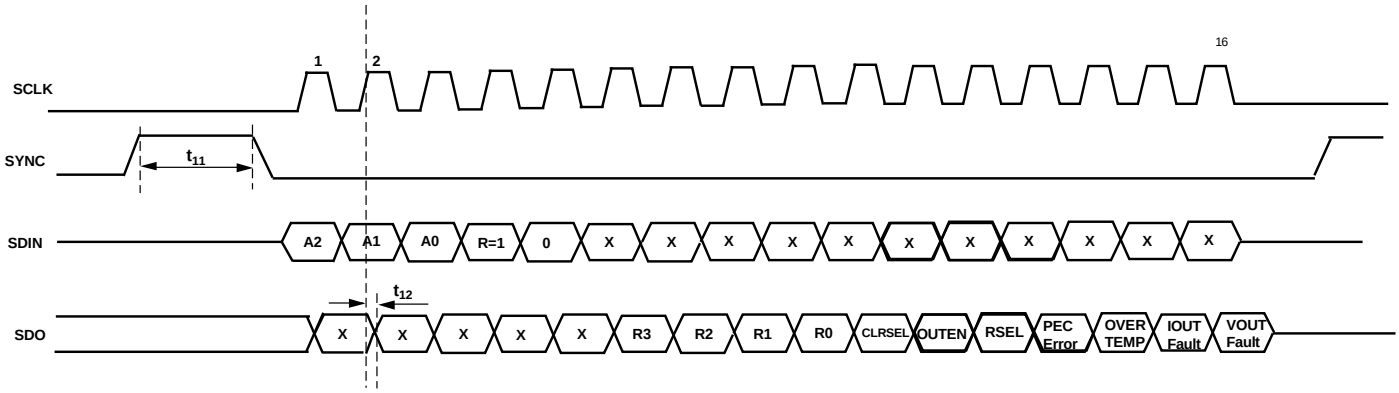


Figure 3. Readback Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.
Transient currents of up to 100 mA do not cause SCR latch-up.

Table 4.

Parameter	Rating
AV_{DD} to GND	−0.3V to 30v
AV_{SS} to GND	+0.3 V to -30v
AV_{DD} to AV_{SS}	-0.3V to 60v
DV_{CC} to GND	−0.3 V to +7 V
$+V_{SENSE}$ to GND	AV_{SS} to AV_{DD}
$-V_{SENSE}$ to GND	+/-5.0v
Digital Inputs to GND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs to GND	−0.3 V to DV_{CC} + 0.3 V or 7V (whichever is less)
REFIN/REFOUT to GND	−0.3 V to +5 V
VIN to GND	−0.3 V to +5 V
V_{OUT} to GND	AV_{SS} to AV_{DD}
I_{OUT} to GND	−0.3V to AV_{DD}, +0.3V to AV_{SS}
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
32-Lead LFCSP Package	
θ_{JA} Thermal Impedance	28°C/W
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

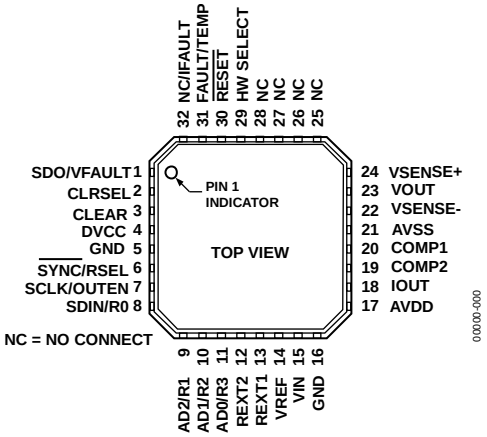


Figure 4. LFCSP Pin Configuration

Table 5. Pin Function Descriptions

LFCSP Pin No.	Mnemonic	Description
1	SDO/VFAULT	In Software Mode, Serial Data Output. Used to clock data from the serial register in readback mode. Data is clocked out on the rising edge of SCLK and is valid on the falling edge of SCLK. Open Drain Output, must be connected to a pull up resistor. In Hardware mode, acts as a SHORT circuit Fault alert pin. This pin is asserted low when an SHORT circuit. Error is detected. Open drain output, must be connected to a pull-up resistor.
2	CLRSEL	In Hardware or software mode, selects the clear value, either zero-scale or mid-scale code. In Software mode, this pin is implemented as a logic OR with the internal CLRSEL bit.
3	CLEAR	Active High Input. Asserting this pin sets the Output Current/Voltage to zero-scale code or mid-scale code of range selected (user-selectable). CLEAR is a LOGIC OR with the internal CLEAR bit.
4	DVCC	Digital Power Supply
5	GND	Ground Connection.
6	SYNC/RSEL	In Software Mode, Positive edge sensitive latch, a rising edge will parallel load the input shift register data into the INPUT register, also updating the output. In Hardware mode, this pin chooses whether internal/external current sense resistor is used
7	SCLK/OUTEN	In Software Mode, Serial Clock Input. Data is clocked into the shift register on the falling edge of SCLK. This operates at clock speeds up to 30 MHz. In Hardware mode, this pin acts as an output enable pin.
8	SDIN/RO	In Software Mode, Serial Data Input. Data must be valid on the falling edge of SCLK. In Hardware Mode, R0 is Range Decode Bit. This pin, in conjunction with R2, R3, R1 choose the output current/voltage range setting on the part.
9	AD2/R1	In Software Mode, AD2 is Device Addressing bit. This pin, in conjunction with AD1, AD0 allow up to 8 devices to be addressed on one bus. In Hardware Mode, R1 is Range Decode Bit. This pin, in conjunction with R2, R3, R0 choose the output current/voltage range setting on the part.
10	AD1/R2	In Software Mode, AD1 is Device Addressing bit. This pin, in conjunction with AD2, AD0 allow up to 8 devices to be addressed on one bus.

LFCSP Pin No.	Mnemonic	Description
		In Hardware Mode, R2 is Range Decode Bit. This pin, in conjunction with R3, R1, R0 choose the output current/voltage range setting on the part.
11	AD0/R3	In Software Mode, AD0 is Device Addressing bit. This pin, in conjunction with AD1, AD2 allow up to 8 devices to be addressed on one bus. In Hardware Mode, R3 is Range Decode Bit. This pin, in conjunction with R2, R1, R0 choose the output current/voltage range setting on the part.
12 13	REXT1 REXT 2	An external current setting resistor can be connected to this pin to improve the I_{OUT} temperature drift performance. **When using the Internal RSET resistor these pins must be left floating.**
14	VREF	Reference Input
15	VIN	Analog Input (0-4.096v)
16	GND	Ground Connection.
17	AV_{DD}	Positive Analog Supply Pin.
18	IOUT	Current Output Pin
19	COMP1	Optional compensation capacitor connection for the voltage output buffer
20	COMP2	Optional compensation capacitor connection for the voltage output buffer
21	AV_{SS}	Negative Analog Supply Pin.
22	$-V_{SENSE}$	Sense connection for the negative voltage output load connection. This pin must stay within +/-3.0v of ground for correct operation.
23	V_{OUT}	Buffered Analog Output Voltage.
24	$+V_{SENSE}$	Sense connection for the positive voltage output load connection.
25,26,27,28	NC	No Connect Pin. Can be tied to GND.
29	HW SELECT	This part is used to configure the part to hardware/software mode. HW SELECT = 0 selects Software Control. HW SELECT = 1 selects Hardware Control.
30	RESET	Resets the part to its power on state.
31	FAULT/TEMP	In Software mode, acts as a general Fault alert pin. This pin is asserted low when an open circuit, short circuit, over temperature or PEC Interface Error is detected. Open drain output, must be connected to a pull-up resistor. In Hardware mode, acts as an over temp FAULT pin. This pin is asserted low when an over temperature Error is detected. Open drain output, must be connected to a pull-up resistor.
32	NC/IFAULT	In Hardware mode, acts as a OPEN circuit Fault alert pin. This pin is asserted low when an OPEN circuit. Error is detected. Open drain output, must be connected to a pull-up resistor. In Software mode, is a NC. Tie to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

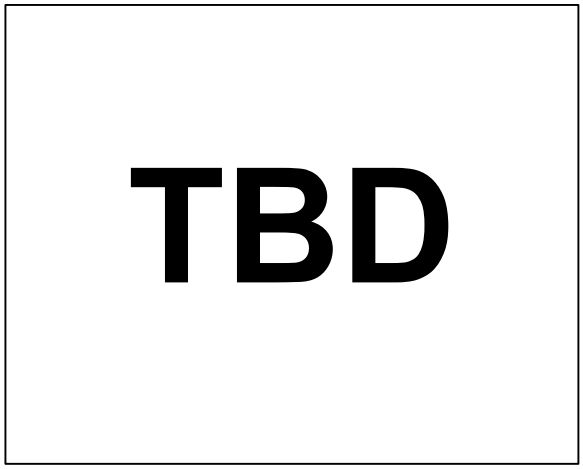


Figure 5.

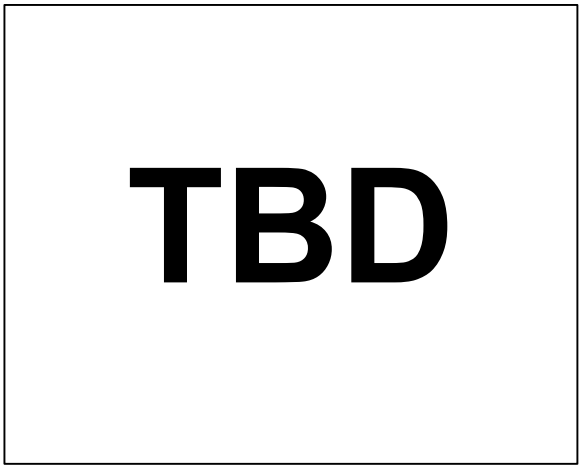


Figure 8.

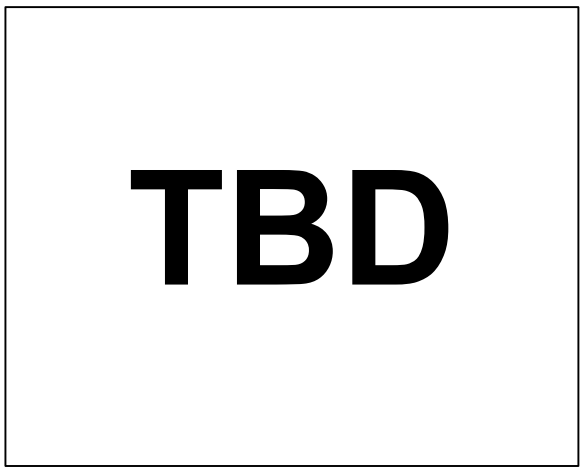


Figure 6.

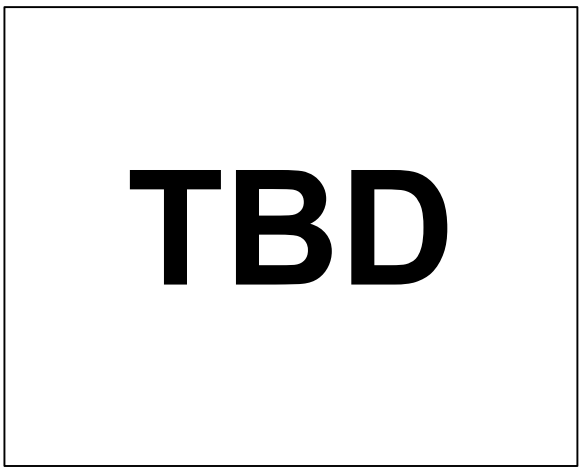


Figure 9.

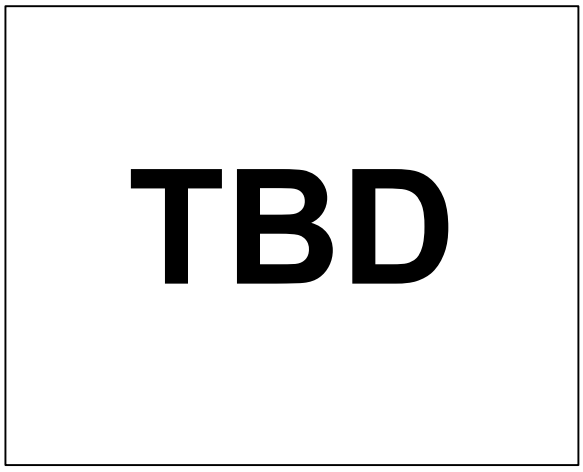


Figure 7.

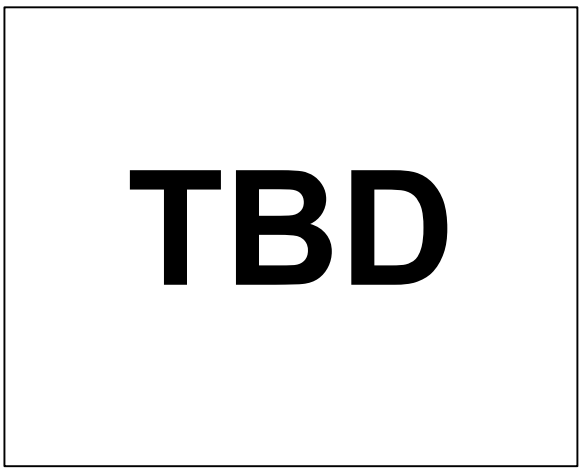


Figure 10

TERMINOLOGY

Output Voltage Settling Time

Output voltage settling time is the amount of time it takes for the output to settle to a specified level for a full-scale input change. A plot of settling time can be seen in Table TBD

Slew Rate
The slew rate of a device is a limitation in the rate of change of the output voltage. Slew rate is measured from 10% to 90% of the output signal and is given in V/µs.

Total Unadjusted Error
Total unadjusted error (TUE) is a measure of the output error taking all the various errors into account. TUE is expressed in % FSR.

Current Loop Voltage Compliance
The maximum voltage at the I_{OUT} pin for which the output currnet will be equal to the programmed value.

Power-On Glitch Energy
Power-on glitch energy is the impulse injected into the analog output when the AD5750 is powered-on. It is specified as the area of the glitch in nV-sec.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output is affected by changes in the power supply voltage.

THEORY OF OPERATION

Figures 11 and 12 shows a typical configuration of AD5750 in Software Mode (Figure 11) and in Hardware mode (Figure 12) in an output module system. The HW SELECT pin chooses whether the part is configured in software or hardware mode. The analog input to the AD5750 is provided from a low voltage, single supply digital-to-analog converter such as the AD5061 which provides an output range of 0-4.096V. The supply and reference for the DAC, as well as the reference for the AD5750 can be supplied from a reference such as the ADR392. The AD5750 can operate from supplies up to +26.4 volts.

In current mode, software selectable output ranges include ±20mA, ±24mA, 0-20 mA, 4mA–20mA or 0mA–24mA.
In voltage mode, software selectable output ranges include 0V–5V, 0V–10V, ±5V or ±10V. The current and voltage outputs are available on separate pins. Only one output can be enabled at one time. The output range is selected by programming the range bits in the control register.

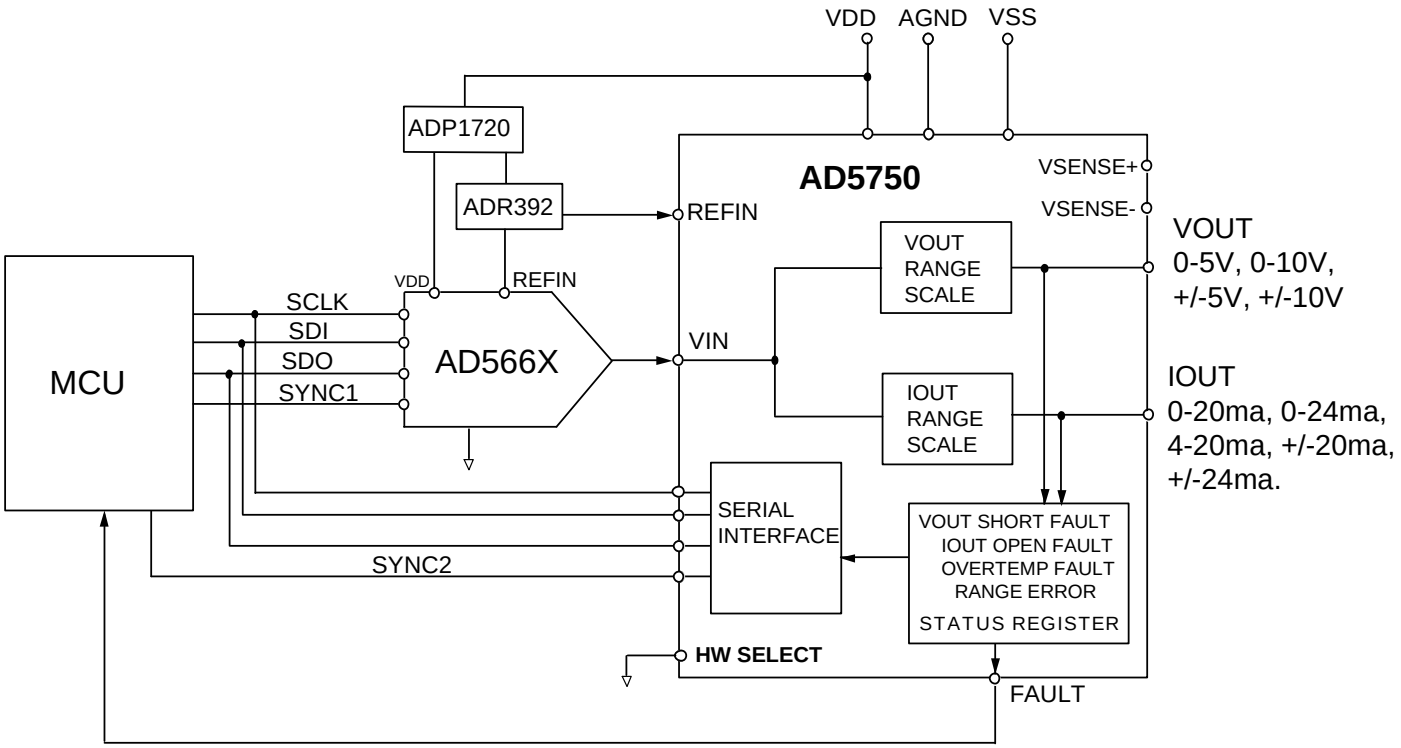


Figure 11. Typical System Configuration in Software Mode .Pull up resistors not shown for open drain outputs.

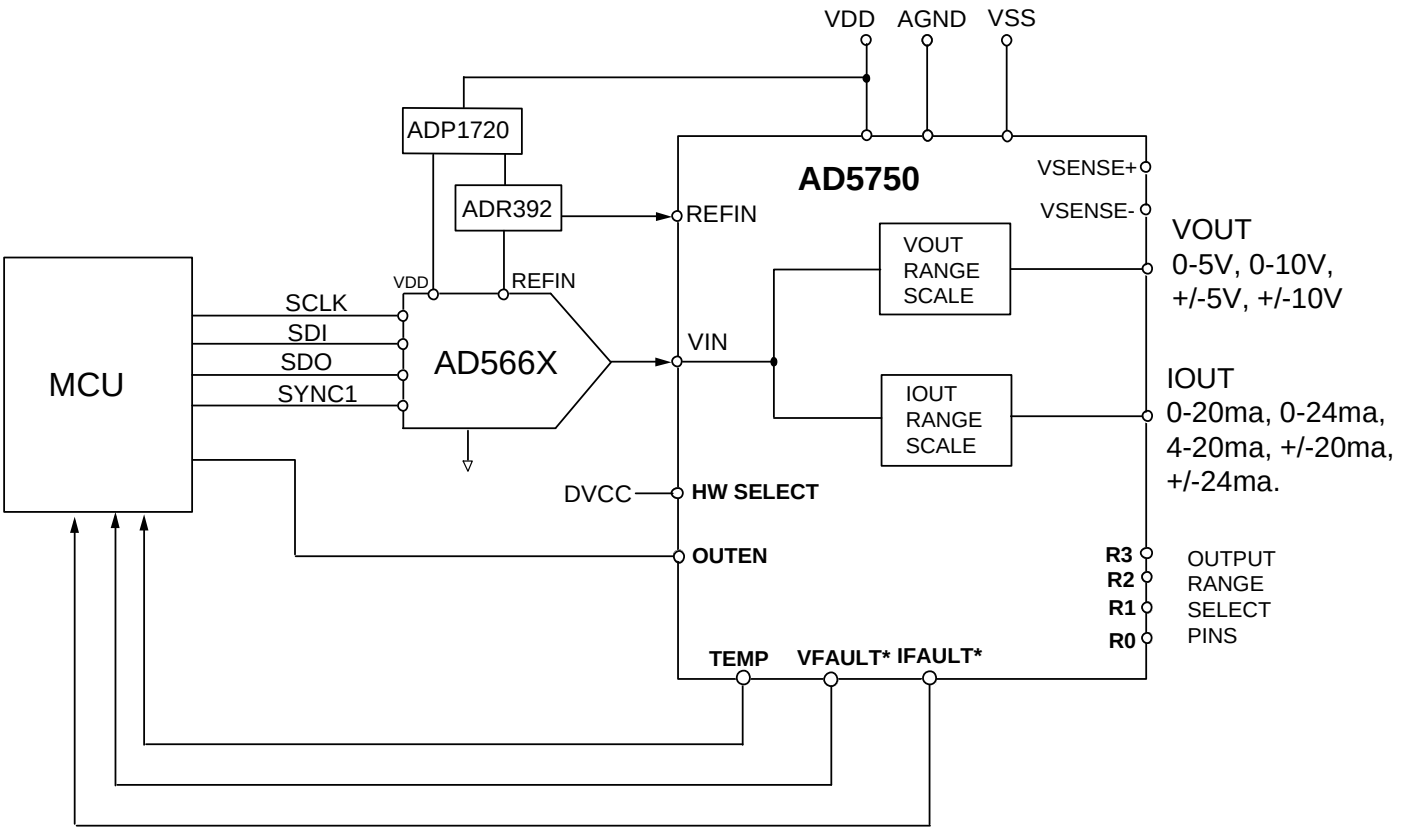


Figure 12. Typical System Configuration in Hardware Mode. Pull up resistors not shown for open drain outputs.

CURRENT OUTPUT ARCHITECTURE

The voltage input from the analog input VIN core (0-4.096v) is either converted to a current (see Figure 12) which is then mirrored to the supply rail so that the application simply sees a current source output with respect to an internal reference voltage or it is buffered and scaled to output a software selectable unipolar or bipolar voltage range (See Figure 13). The Reference is used to provide internal offsets for range and gain scaling. The selectable output range is programmable through the digital interface.

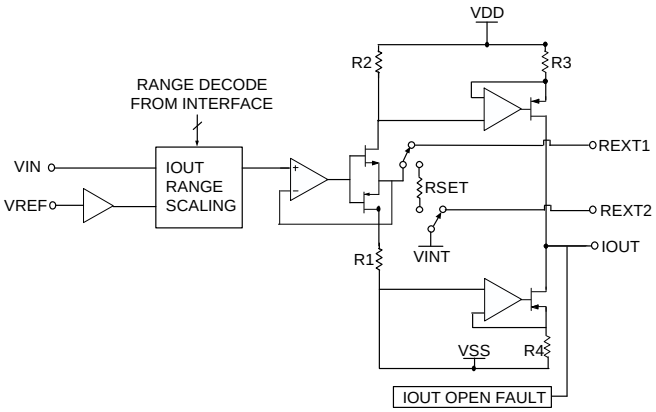


Figure 11. Current Output Configuration

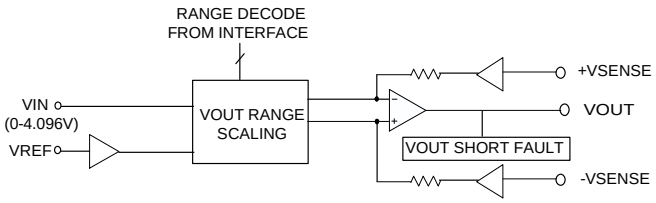


Figure 12. Voltage Output

Voltage Output Amplifier

The voltage output amplifier is capable of generating both unipolar and bipolar output voltages. It is capable of driving a load of 1 kΩ in parallel with 1.2 uF. The source and sink capabilities of the output amplifier can be seen in Figure TBD. The slew rate is 1 V/µs with a full-scale settling time of 10 µs.(10V step).

The current and voltage are output on separate pins and cannot be output simultaneously. This allows the user to tie both the current and voltage output pins together and configuring the end system as "one channel" output.

Driving Large Capacitive Loads

The voltage output amplifier is capable of driving capacative loads of up to 1uF with the addition of a non-polarised 4nF compensation capacitor between the C_{COMP1} and C_{COMP2} pins.

Without the compensation capacitor, up to 20nF capacitive loads can be driven.

POWER ON STATE OF AD5750

On Power-up, the AD5750 will sense whether hardware or software mode is loaded and set the power up conditions accordingly.

In software SPI mode, the part will power up with all outputs disabled (OUTEN bit=0). In disabled mode, both the current and voltage outputs are put into tri-state mode. The user will have to set the OUTEN bit in the control register to enable the output and in the same write the user will also set the output range configuration using the range bits.

If hardware mode is selected, the part will power up to the conditions defined by the range bits and the status of the OUTEN pin. It is recommended to keep the output disabled when powering up the part in hardware mode.

RESET:

The AD5750 contains a reset function.

In Software mode, the part can be reset using the RESET pin (active low) or the RESET bit (RESET=1). A reset will disable both the current and voltage outputs and put them in tri-state mode. The user will have to write to the OUTEN bit to enable the output and in the same write the user will also set the output range configuration. The RESET pin is a level sensitive input - the part will stay in RESET mode as long as RESET pin is low. The RESET bit will clear to zero following a RESET command to the control register.

In hardware mode, there is no RESET. If using the part in hardware mode the RESET pin should be tied high.

OUTEN

In Software mode, the output can be enabled/disabled using the OUTEN bit in the control register. When the output is disabled, both the current and voltage channels both go into tri-state. The user will have to set the OUTEN bit to enable the output and at this time the user will also set the output range configuration.

In Hardware mode, the output can be enabled/disabled using the OUTEN pin. When the output is disabled, both the current and voltage channels both go into tri-state. The user will have to write to the OUTEN pin to enable the output. It is recommended that the output be disabled when changing the ranges.

SOFTWARE CONTROL:

Software control is enabled by connecting the HW SELECT pin to ground. In software mode, the AD5750 is controlled over a versatile 3-wire serial interface that operates at clock rates up to 30 MHz. It is compatible with SPI®, QSPI™, MICROWIRE™, and DSP standards The input shift register is 16 bits wide. Data is loaded into the device MSB first as a 16-bit word under the control of a serial clock input, SCLK. Data is clocked in on the falling edge of SCLK. The input register consists of 16 control bits as shown in Table 5. The timing diagram for this operation is shown in Figure 2. The first 3 bits of the Input Register are used to set the hardware address of the AD5750 device on the PCB board. Up to 8 devices can be addressed per board.

Bits D11, D1, D0 must always be set to 0 during any write sequence.

Table 3. Input Shift Register Format

MSB															**LSB**
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A2	A1	A0	R/$\overline{\mathbf{W}}$	0	R3	R2	R1	R0	CLRSEL	OUTEN	CLEAR	RSEL	RESET	0	0

Table 6. Input Shift Register Decoded

Register				
A2, A1, A0	Used in association with External Pins AD2, AD1, AD0 to determine which part is being addressed by the system controller.			
	A2	**A1**	**A0**	**Function**
	0	0	0	Addresses Part with pins AD2=0, AD1=0, AD0=0
	0	0	1	Addresses Part with pins AD2=0, AD1=0, AD0=1
	0	1	0	Addresses Part with pins AD2=0, AD1=1, AD0=0
	0	1	1	Addresses Part with pins AD2=0, AD1=1, AD0=1
	1	0	0	Addresses Part with pins AD2=1, AD1=0, AD0=0
	1	0	1	Addresses Part with pins AD2=1, AD1=0, AD0=1
	1	1	0	Addresses Part with pins AD2=1, AD1=1, AD0=0
	1	1	1	Addresses Part with pins AD2=1, AD1=1, AD0=1
R/$\overline{\mathbf{W}}$	Indicates a read from or a write to the addressed register.			
CLEAR	Software Clear Bit – Active High.			
CLRSEL	Sets Clear Mode to zero scale or midscale. See Text.			
	CLRSEL			
	0	Clear to Zero Volts		
	1	Clear to Mid Scale in Unipolar Mode, Clear to Zero Scale in Bipolar Mode.		
OUTEN	Output Enable Bit. This bit must be set to 1 to enable the outputs.			
RSEL	Select Internal/External Current Sense Resistor.			
	RSEL			
	1	Select Internal Current Sense Resistor /*used with Range bits to select Range */		
	0	Select External Current Sense Resistor /*used with Range bits to select Range */		
R3,R2,R1,R0	Selects output Configuration in conjunction with RSEL.			

	RSEL	**R3**	**R2**	**R1**	**R0**	**Output Configuration**
	0	0	0	0	0	4-20MA External Current Sense Resistor 15k ohm.
	0	0	0	0	1	0-20MA External Current Sense Resistor 15k ohm.
	0	0	0	1	0	0-24MA External Current Sense Resistor 15k ohm.
	0	0	0	1	1	+/-20MA External Current Sense Resistor 15k ohm.
	0	0	1	0	0	+/-24MA External Current Sense Resistor 15k ohm.
	0	0	1	0	1	0-5V
	0	0	1	1	0	0-10V
	0	0	1	1	1	+/-5V
	0	1	0	0	0	+/-10V
	0	1	0	0	1	0-6.0V (20% over range)
	0	1	0	1	0	0-12.0V (20% over range)
	0	1	0	1	1	+/-6.0V (20% over range)

	0	1	1	0	0	+/-12.0V (20% over range)
	0	1	1	0	1	+/-2.5v
	0	1	1	1	0	N/A. If selected output will drive 0V.
	0	1	1	1	1	N/A. If selected output will drive 0V.
	1	0	0	0	0	4-20MA Internal Current Sense Resistor.
	1	0	0	0	1	0-20MA Internal Current Sense Resistor.
	1	0	0	1	0	0-24MA Internal Current Sense Resistor.
	1	0	0	1	1	+/-20MA
	1	0	1	0	0	+/-24MA
	1	0	1	0	1	0-5V
	1	0	1	1	0	0-10V
	1	0	1	1	1	+/-5V
	1	1	0	0	0	+/-10V
	1	1	0	0	1	0-6.0V (20% over range)
	1	1	0	1	0	0-12.0V (20% over range)
	1	1	0	1	1	+/-6.0V (20% over range)
	1	1	1	0	0	+/-12.0V (20% over range)
	1	1	1	0	1	3.92ma – 20.4ma Internal Current Sense Resistor.
	1	1	1	1	0	0ma – 20.4ma Internal Current Sense Resistor.
	1	1	1	1	1	0ma – 24.5ma Internal Current Sense Resistor.
Reset						Resets the part to its Power on State

Readback Operation

Readback mode is invoked by selecting the correct device address (A2,A1,A0) and then setting the R/W bit to 1. By default the SDO pin is disabled, after having addressed the AD5750 for a read operation, setting R/W to 1 will enable the SDO pin and SDO data will be clocked out on the 5th rising edge of SCLK. After the data has been clocked out on SDO, a rising edge on SYNC will disable (tri- state) the SDO pin once again. STATUS and CONTROL register data will be both available during the same read cycle. See Table 7 below.

Table 7. Input Shift Register Contents for a read operation

MSB															**LSB**
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
A2	A1	A0	**1**	0	R3	R2	R1	R0	CLRSEL	OUTEN	RSEL	PEC Error Bit	OVER TEMP	IOUT Fault	Vout Fault

The STATUS bits are 4 read only bits. They are used to notify the user of specific fault conditions that have arisen, such as open or short circuit on the output, over temperature, or an interface error. If any one of these fault conditions occur a hardware FAULT is also asserted low which can be used as a hardware interrupt to the controller.

Full explanation of fault conditions are given in the Features sections.

Table 9. STATUS Bits Options

Option	Description
PEC ERROR	Bit Set if there is an Interface Error detected by CRC-8 Error Checking. See features section.
VOUT FAULT	Bit set if there is a short Circuit on VOUT pin.
IOUT FAULT	Bit set is there is an open circuit on IOUT pin.
OVER TEMP	This bit will be set if the AD5750 core temperature exceeds approx. 150°C.

HARDWARE CONTROL:

Hardware control is enabled by connecting the HW SELECT pin to DVCC. In this mode, pins R3,R2,R1,R0 along with RSEL pin are used to configure the output range as per Table.

RSEL	R3	R2	R1	R0	Output Configuration
0	0	0	0	0	4-20MA External Current Sense Resistor 15k ohm.
0	0	0	0	1	0-20MA External Current Sense Resistor 15k ohm.
0	0	0	1	0	0-24MA External Current Sense Resistor 15k ohm.
0	0	0	1	1	+/-20MA External Current Sense Resistor 15k ohm.
0	0	1	0	0	+/-24MA External Current Sense Resistor 15k ohm.
0	0	1	0	1	0-5V
0	0	1	1	0	0-10V
0	0	1	1	1	+/-5V
0	1	0	0	0	+/-10V
0	1	0	0	1	0-6.0V (20% over range)
0	1	0	1	0	0-12.0V (20% over range)
0	1	0	1	1	+/-6.0V (20% over range)
0	1	1	0	0	+/-12.0V (20% over range)
0	1	1	0	1	+/-2.5v
0	1	1	1	0	N/A. If selected output will drive 0V.
0	1	1	1	1	N/A. If selected output will drive 0V.
1	0	0	0	0	4-20MA Internal Current Sense Resistor.
1	0	0	0	1	0-20MA Internal Current Sense Resistor.
1	0	0	1	0	0-24MA Internal Current Sense Resistor.
1	0	0	1	1	+/-20MA
1	0	1	0	0	+/-24MA
1	0	1	0	1	0-5V
1	0	1	1	0	0-10V
1	0	1	1	1	+/-5V
1	1	0	0	0	+/-10V
1	1	0	0	1	0-6.0V (20% over range)
1	1	0	1	0	0-12.0V (20% over range)
1	1	0	1	1	+/-6.0V (20% over range)
1	1	1	0	0	+/-12.0V (20% over range)
1	1	1	0	1	3.92ma – 20.4ma Internal Current Sense Resistor.
1	1	1	1	0	0ma – 20.4ma Internal Current Sense Resistor.
1	1	1	1	1	0ma – 24.5ma Internal Current Sense Resistor.

In hardware mode there is no status register. The fault conditions; open circuit, short circuit and over temperature are available on pins IFAULT, VFAULT and TEMP. If any one of these fault conditions are set then a low is asserted on the specific fault pin. IFAULT, VFAULT and TEMP are open drain outputs and therefore can be connected together to allow the user generate one interrupt to the system controller to communicate a fault. If hardwired in this way, it will not be possible to isolate which fault occurred in the system.

DEFAULT CONFIGURATION:

On initial power-up of the AD5750 the power-on-reset circuit ensures that all registers are loaded with zero-code, as such the default output is the current output with the 4mA to 20mA range selected, the current output until a value is programmed is 0mA. The voltage output pin will be in three-state. An alternative current range or a voltage output range may be selected via the CONTROL register.

TRANSFER FUNCTION

Voltage Output

For a unipolar voltage output range, the output voltage expression is given by

Vout = GAIN x VIN

For a bipolar voltage output range, the output voltage expression is given by

Vout = (GAIN x VIN – (GAIN x (VREF/2)) x VIN)

where:

VREF is the reference voltage applied at the REFIN pin.
Gain is an internal gain whose value depends on the output range selected by the user as shown in

Current Output

For a given current output range, the current output range is chosen setting the bits R3,R2,R1,R10 in the Input Register or pins. Transfer function will change depending on current range selected.

FEATURES

OUTPUT FAULT ALERT – SOFTWARE MODE

In Software mode, the AD5750 is equipped with one FAULT pin, this is an open-drain output allowing several AD5750 devices to be connected together to one pull-up resistor for global fault detection. In software control mode, the FAULT pin is forced active high by any one of the following fault scenarios;

1) The Voltage at I_{OUT} attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with "window limits" since this would require an actual output error before the FAULT output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately one volt of remaining drive capability. Thus the FAULT output activates slightly before the compliance limit is reached. Since the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain and an output error does not occur before the FAULT output becomes active.
2) A short is detected on the voltage output pin. Short circuit current limited to 25ma.
3) An interface error is detected due to the PEC error checking failure. See PEC error checking section.
4) A range change is detected without the user writing to the Interface.
5) If the core temperature of the AD5750 exceeds approx. 150°C.

OUTPUT FAULT ALERT – HARDWARE MODE

In hardware mode, the AD5750 is equipped with 3 FAULT pins, VFAULT, IFAULT, TEMP. These are an open-drain outputs allowing several AD5750 devices to be connected together to one pull-up resistor for global fault detection. In hardware control mode, these fault pins are forced active by any one of the following fault scenarios;

1) Open Circuit Detect. The Voltage at I_{OUT} attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The internal circuitry that develops the fault output avoids using a comparator with "window limits" since this would require an actual output error before the FAULT output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approximately one volt of remaining drive capability. Thus the FAULT output activates slightly before the compliance limit is reached. Since the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain and an output error does not occur before the FAULT output becomes active.

   If this fault is detected the IFAULT pin is forced low.
2) A short is detected on the voltage output pin. Short circuit current limited to 25ma. If this fault is detected the VFAULT pin is forced low.
3) If the core temperature of the AD5750 exceeds approx. 150°C. If this fault is detected the TEMP pin is forced low.

VOLTAGE OUTPUT SHORT CIRCUIT PROTECTION

Under normal operation the voltage output will sink/source 5mA and maintain specified operation. The maximum current that the voltage output will deliver is 15mA, this is the short circuit current.

ASYNCHRONOUS CLEAR (CLEAR)

CLEAR is an active high clear that allows the voltage output to be cleared to either zero-scale code or mid-scale code, user-selectable via the CLRSEL pin or the CLRSEL bit of the INPUT register as described in Table 6. (The Clear select feature is a logical OR function of the CLR SELECT pin and the CLRSEL bit). The Current loop output will clear to the bottom of its programmed range. It is necessary to maintain CLEAR high for a minimum amount of time (see Figure 2) to complete the operation. When the CLEAR signal is returned low, the output returns to its programmed value or a new value if programmed. A clear operation can also be performed via the CLEAR command in the control register.

Table 11. CLEAR SELECT Options

CLR SELECT	Output CLR Value	
	Unipolar Output Voltage Range	**Bipolar Output Range**
0	0 V	Negative Full-Scale
1	Mid-Scale	0 V
	Unipolar Current Output Range	**Bipolar Current Output Range**
0	Zero-Scale e.g. 4ma on 4-20ma 0ma on 0-20ma etc...	Zero Scale e.g. -24ma on +/-24ma
1	Mid-Scale e.g. 12ma on 4-20ma 10ma on 0-20ma	Mid-Scale e.g. 0ma on +/-24ma

EXTERNAL CURRENT SETTING RESISTOR

Referring to Figure 1, RSET is an internal sense resistor as part of the voltage to current conversion circuitry. The nominal value of internal current sense resistor is 15k ohm. To allow for overrange capability in current mode, the user can also select

the internal current sense resistor to be 14.7K, giving a nominal 2% overrange capability. This feature is available in the 0-20ma, 4-20ma, +/-20ma current ranges.

The stability of the output current value over temperature is dependent on the stability of the value of RSET. As a method of improving the stability of the output current over temperature an external low drift resistor can be connected to the RSET1 & RSET2 pins of the AD5750 to be used instead of the internal resistor RSET. The external resistor is selected via the input register. If the external resistor option is not used the RSET1 and RSET2 pins should be left floating.

PROGRAMMABLE OVER-RANGE MODES

The AD5750 contains an over range mode for most of the available ranges. In voltage mode the over-range is typically 20% and in current mode the over-range is typically 2%. The overranges are selected by configuring R3, R1, R1, R0 bits/pins accordingly.

In voltage mode the overranges are typically 20% providing programmable output ranges of 0-6v, 0-12v, +/-6v and +/-12v. The 0-4.096v analog input remains the same.
In current mode the overranges are typically 2%. In current mode the overrange capability is only available on 3 ranges, 0-20ma, 0-24ma, 4-20ma. For these ranges the analog input will also vary, according to the table below.

Over Range	Analog Input
0-20.4ma	0.075v – 4.096v
3.92-20.4ma	0.06v-4.096v
0-24.5ma	0.065-4.096v

For example, in 0-20.4ma range, an analog input of 0.075v will output 0ma and 4.096v will output full scale 20.4ma.

PACKET ERROR CHECKING

To verify that data has been received correctly in noisy environments, the AD5750 offers the option of error checking based on an 8-bit (CRC-8) cyclic redundancy check. The device controlling the AD5750 should generate an 8-bit frame check sequence using the polynomial

$$C(x) = x_8 + x_2 + x_1 + 1.$$

This is added to the end of the data word, and 24 data bits are sent to the AD5750 before taking SYNC high. If the AD5750 sees a 24-bit data frame, it will perform the error check when SYNC goes high. If the check is valid, then the data will be written to the selected register. If the error check fails, the FAULT will go high and bit D4 of the Status Register is set. After reading this register, this error flag is cleared automatically and PEC goes high again.

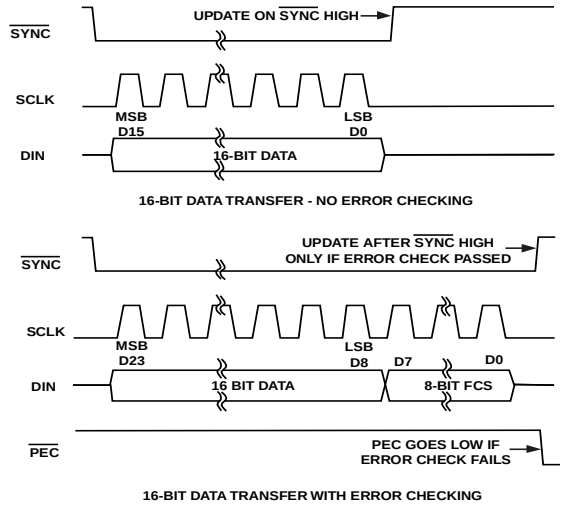


Figure 13. PEC Error Checking Timing

APPLICATIONS INFORMATION

TRANSIENT VOLTAGE PROTECTION

The AD5750 contains ESD protection diodes which prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. In order to protect the AD5750 from excessively high voltage transients , external power diodes and a surge current limiting resistor may be required, as shown in Figure 15. The constraint on the resistor value is that during normal operation the output level at IOUT must remain within its voltage compliance limit of $AV_{DD} - 2.0V$ and the two protection diodes and resistor must have appropriate power ratings.

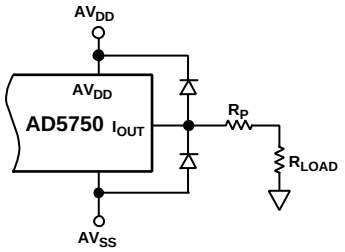


Figure 15. Output Transient Voltage Protection

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5750 is mounted should be designed so that the AD5750 lies on the analog plane.

The AD5750 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5750 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur. The *i*Coupler® family of products from Analog Devices provides voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5750 make it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 16 shows a 4-channel isolated interface to the AD5750 using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

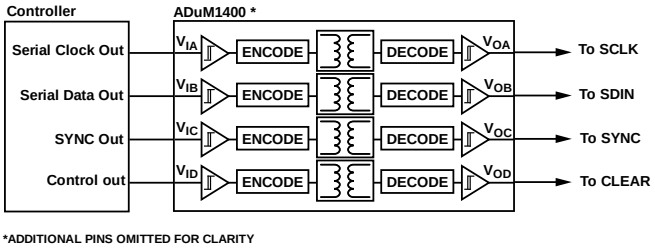


Figure16. Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5750 is via a serial bus that uses protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a sync signal. The AD5750 require a 16-bit data-word with data valid on the falling edge of SCLK.

OUTLINE DIMENSIONS

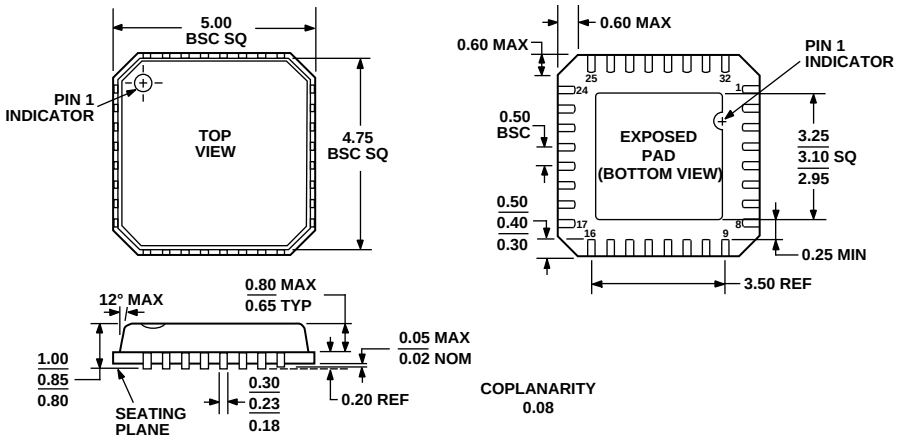


Figure 17. 32-Lead Lead Frame Chip Scale Package
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	TUE Accuracy	Temperature Range	Package Description	Package Option
AD5750ACPZ	0.3 %	-40°C to 105°C	32 Lead LFCSP	CP-32-2
AD5750BCPZ	0.1%	-40°C to 105°C	32 Lead LFCSP	CP-32-2