Synchronous DRAM 8M x 8 Bit x 4 Banks

General Description

The VDS8608A8A are four-bank Synchronous DRAMs organized as 8,388,608 words x 8 bits x 4 banks.

Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle.

Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth high performance memory system applications

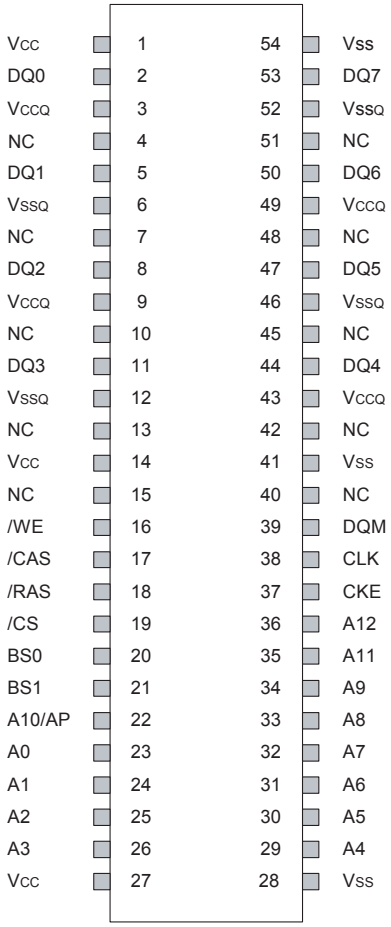
Features

- JEDEC standard LVTTL 3.3V power supply
- MRS Cycle with address key programs
  - -CAS Latency (2 & 3)
  - -Burst Length (1,2,4,8,& full page)
  - -Burst Type (sequential & Interleave)
- 4 banks operation
- All inputs are sampled at the positive edge of the system clock
- Burst Read single write operation
- Auto & Self refresh
- DQM for masking
- 8192 Refresh Cycles
- Package:54-pins 400 mil TSOP-Type II

Ordering Information.

Part No.	Frequency	Interface	Package
VDS8608A8A-75	133Mhz-333	LVTTL	400mil 54pin TSOPII
VDS8608A8A-75A	133Mhz-222	LVTTL	400mil 54pin TSOPII

Pin Assignment

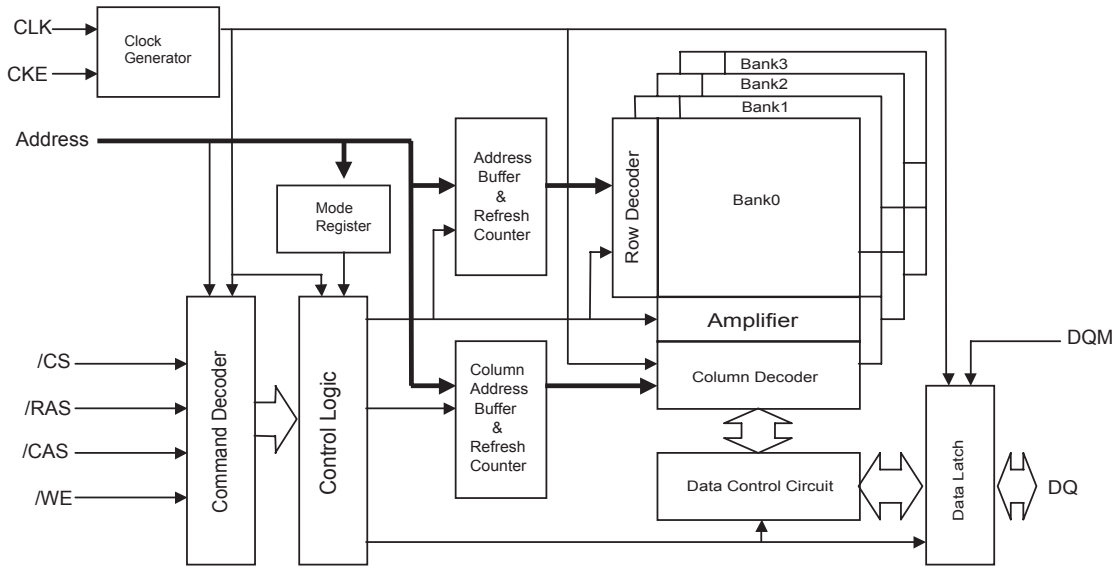


54-pin plastic TSOP II 400 mil

Pin Description

PIN	NAME	FUNCTION
CLK	System Clock	Active on the positive edge to sample all inputs.
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least on cycle prior new command. Disable input buffers for power down in standby
/CS	Chip Select	Disables or Enables device operation by masking or enabling all input except CLK, CKE and L(U)DQM
A0~A12	Address	Row / Column address are multiplexed on the same pins. Row address : A0~A12 Column address : A0~A9
BS0~BS1	Banks Select	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
DQ0~DQ7	Data	Data inputs / outputs are multiplexed on the same pins.
/RAS	Row Address Strobe	Latches row addresses on the positive edge of the CLK with /RAS low
/CAS	Column Address Strobe	Latches Column addresses on the positive edge of the CLK with /CAS low
/WE	Write Enable	Enables write operation and row recharge.
VCC/VSS	Power Supply/Ground	Power and Ground for the input buffers and the core logic.
V_{CCQ}/V_{SSQ}	Data Output Power/Ground	Power supply for output buffers.
NC	No Connection	This pin is recommended to be left No Connection on the device.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{out}	-0.3 ~Vcc+0.3	V
Voltage on VDD supply relative to Vss	V_{CC}, V_{CCQ}	-0.3 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	℃
Power dissipation	P_D	1	W
Short circuit current	I_{OUT}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATING are exceeded.

Functional operation should be restricted to recommended operating condition.

Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Condition

Voltage referenced to Vss = 0V, T_A = 0 to 70 ℃

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}, V_{CCQ}	3.0	3.3	3.6	V	
Input logic high voltage	V_{IH}	2.0	3.0	V_{CC}+0.3	V	2
Input logic low voltage	V_{IL}	-0.3	-	0.8	V	2

Note : 1. V_{IH} (max)=Vcc/ VccQ+1.2V for pulse width ≦ 5ns acceptable.

2.V_{IL}(min)=-Vss/ VssQ-1.2V for pulse width ≦ 5ns acceptable.

AC Operating Condition

Voltage referenced to Vss = 0V, T_A = 0 to 70 ℃

Parameter	Symbol	Value	Unit	Note
AC input high / low level voltage	V_{IH} / V_{IL}	2.4 / 0.4	V	
Input timing measurement reference level voltage	Vtrip	1.4	V	
Input rise / fall time	TR / tF	2	Ns	
Output timing measurement reference level	Voutfef	1.4	V	
Output load capacitance for access time measurement	CL	50	pF	2

Note: 1. 3.15V ≦ V_{DD} ≦ 3.6V is applied for VDS8608A8A55.

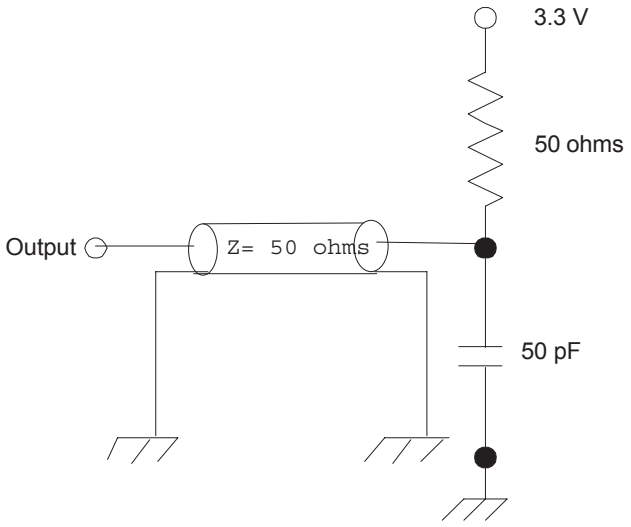
2. Output load to measure access times is equivalent to two TTL gates and one capacitor (30pF). For details, refer to AC/DC output load circuit.

Capacitance

TA=25℃, f-=1Mhz, VCC=3.3V

Parameter	Pin	Symbol	Min	Max	Unit
Input capacitance	CLK	Cclk	-	3.5	pF
	A0~A12,BS0 ,BS1,CKE,/CS,/RAS, /CAS,/WE,LDQM	CI1	-	3.8	pF
Data input / output capacitance		CI/O	-	6.5	pF

Output load circuit



DC Characteristics I

Parameter	Symbol	Min	Max	Unit	Note
Input leakage current	I_{LI}	-5	5	uA	
Output leakage current	I_{LO}	-5	5	uA	
Output high voltage	V_{OH}	2.4	-	V	I_{OH} = -4mA
Output low voltage	V_{OL}	-	0.4	V	I_{OL} = 4mA

Note : 1.V_{IN} = 0 TO 3.6V, All other pins are not tested under V_{IN} = 0V.

2.D_{OUT} is disabled, V_{OUT} = 0 to 3.6.

DC Characteristics II

Parameter	Symbol	Test condition	Speed		Unit	Note
			75	75A		
Operating Current	ICC1	Burst length=1, One bank active tRC≧tRC(min),I_{OL}=0mA	80	75	mA	1
Precharge standby current in power down mode	ICC2P	CKE≦V_{IL}(max), tCK=min	1	1		
	ICC2PS	CKE≦V_{IL}(max), tCK=∞	1	1		
Precharge standby current in Non power down mode	ICC2	CKE≧V_{IH}(min), /CS≧V_{IH}(min), tCK=min input signals are changed one time during 2clks. All other pins ≧VDD-0.2V or ≦ 0.2V	40	35		
	ICC2S	CKE≧V_{IH}(min), tCK=∞ Input signals are stable.	10	10		
No Operating Current in power down mode	ICC3	CKE≦V_{IL}(max), tCK=min	60	55		
	ICC3P	CKE≦V_{IL}(max), tCK=∞	10	10		
Burst mode operating current	ICC4	t_{CK}≧t_{CK}(min),I_{OL}=0 mA All banks active	100	95		1
Auto refresh current	ICC5	t_{CK}≧t_{CK}(min),I_{OL}=0 mA All banks active	170	160		2
Self refresh current	ICC6	Standard	3	3		
	ICC6L	Lower Power	1	-		

Note: 1. ICC1 and ICC4 depend on output loading and cycle rates. Specified values are measured with the output open.

2. Min. of ^{t}CK is shown at AC characteristics.

AC Characteristics

Parameter		Symbol	Speed				Unit	Note
			75		75A			
			Min	Max	Min	Max		
System clock Cycle time	/CAS Latency = 2	tCK2	7.5	1000	10	10	ns	
	/CAS Latency = 3	tCK3	7	1000	7.5	7		
Clock high pulse width		tCHW	2.5		2.5		ns	1
Clock low pulse width		tCLW	2.5		2.5		ns	1
Access time form clock	/CAS Latency = 2	tAC2		5.4			ns	2
	/CAS Latency = 3	tAC3		5.4				
Write Recovery Time	/CAS Latency = 2	tWR2	7.5		10	7.5		
	/CAS Latency = 3	tWR3	7		7.5			
/RAS cycle time		tRC	56		65		ns	
/RAS to /CAS delay		tRCD	15		20		ns	
/RAS active time		tRAS	40	100K	45	100K	ns	
/RAS precharge time		tRP	15		20		ns	
/RAS to /RAS bank active delay		tRRD	15		15		ns	
/CAS to /CAS delay		tCCD	1		1		CLK	
Data – input setup time		tDS	1.5		1.5		ns	1
Data – input hold time		tDH	0.8		0.8		ns	1
Address setup time		tAS	1.5		1.5		ns	1
Address hold time		tAH	0.8		0.8		ns	1
CKE setup time		tCKS	1.5		1.5		ns	1
CKE hold time		tCKH	0.8		0.8		ns	1
Command setup time		tCMS	1.5		1.5		ns	1
Command hold time		tCMH	0.8		0.8		ns	1
Output Data Hold Time		tOH	3		3		ns	
Output Data High Impedance Time		tHZ	3	7	3	7.5	ns	
Output Data Low Impedance Time		tLZ	0		0		ns	
Mode register Set Cycle Time		tRSC	14		15		ns	
Refresh time		tREF		64		64	ms	

Note : 1. Assume tR / tF (input rise and fall time) is 1 ns.

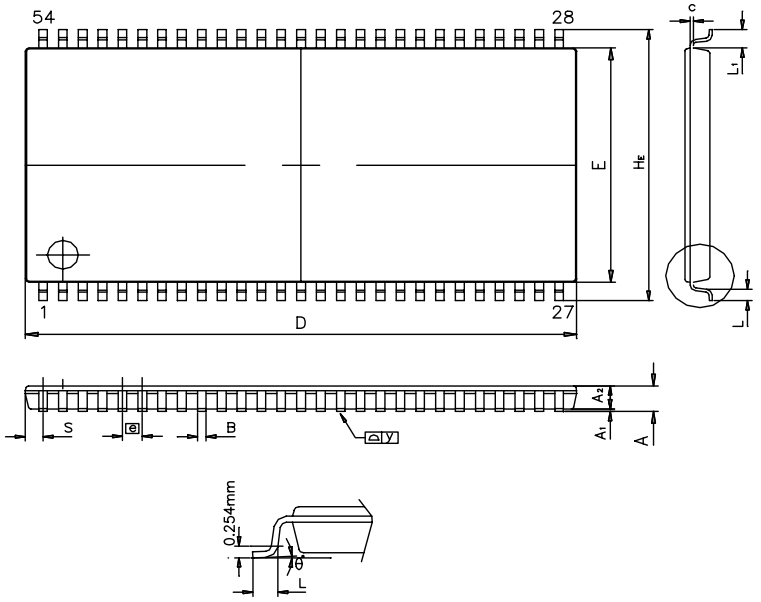
2. Access times to be measured with input signals of 1v / ns edge rate.

3.A new command can be given tRRC after self refresh exit.

Command Truth-Table

Command		CKEn-1	CKEn	/CS	/RAS	/CAS	/WE	DQM	ADDR	A10/AP	BA
Mode Register Set		H	X	L	L	L	L	X	OP code		
No Operation		H	X	H	X	X	X	X	X		
				L	H	H	H				
Bank Active		H	X	L	L	H	H	X	RA		V
Read		H	X	L	H	L	H	X	CA	L	V
Read with Auto Precharge										H	
Write		H	X	L	H	L	L	X	CA	L	V
Write with Auto Precharge										H	
Precharge All Bank		H	X	L	L	H	L	X	X	H	X
Precharge select Bank										L	V
Burst Stop		H	X	L	H	H	L	X	X		
DQM		H	X					V	X		
Auto Refresh		H	H	L	L	L	H	X	X		
Self Refresh	Entry	H	L	L	L	L	H	X	X		
	Exit	L	H	H	X	X	X	X			
				L	H	H	H				
Precharge Power down	Entry	H	L	H	X	X	X	X	X		
				L	H	H	H				
	Exit	L	H	H	X	X	X	X			
				L	H	H	H				
Clock Suspend	Entry	H	L	H	X	X	X	X	X		
				L	V	V	V				
	Exit	L	H	X				X	X		

Package Information



SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			1.20			0.047
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	-----	1.00	-----	-----	0.039	-----
B	0.24	0.32	0.40	0.009	0.012	0.016
c	-----	0.15	------	-----	0.005	-----
D	22.12	22.22	22.62	0.871	0.875	0.905
H_E	11.56	11.76	11.96	0.455	0.463	0.471
E	10.06	10.16	10.26	0.396	0.400	0.404
e	-----	0.80 BSC	-----	-----	0.031	-----
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.80 REF			0.032 REF		
S	0.71 REF			0.028 REF		
θ	0 °	-	8 °	0 °	-	8 °

400mil 54pin TSOP II Package