

ADM8211

IEEE802.11b WLAN NIC Solution PCI/miniPCI/Cardbus Interface with MAC Unit + Baseband Processor (BBP)

DATASHEET

Rev. 1.1

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REVISION HISTORY

Revision Date	Revision	Description
Mar, 2002	0.1	Draft
Apr, 2002	0.3	Preliminary version
Apr, 2002	0.4	Change EEPROM format Rename GPIO0
May, 2002	0.5	Rename EEPROM [54:60] as Tx Power
May, 2002	0.6	Add missed pins in Pin Description, C1, C2, D1, D2
Oct, 2002	0.7	Remove unnecessary chapters Update EEPROM format
Nov, 2002	0.8	Remove PWRLEDACT Remove GPIO2
Feb, 2003	1.0	Formal release
Mar, 2003	1.1	Correct Chapter 6, Electrical Specifications

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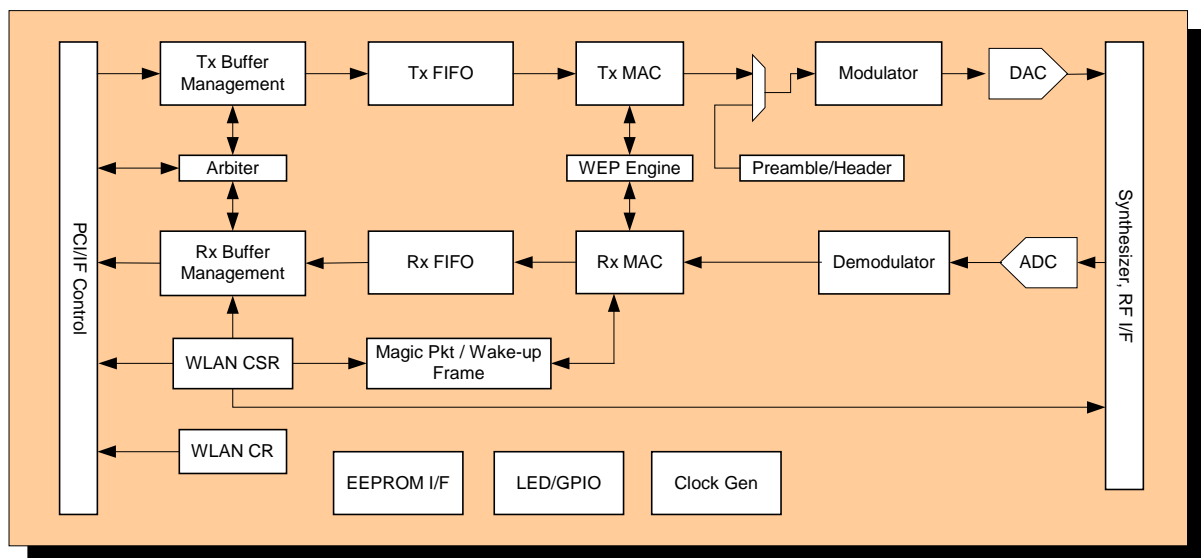
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1 General Description

ADM8211 is a high performance PCI/miniPCI/Cardbus single chip with WLAN MAC controller and Baseband processor integrated.

ADMtek is the leading of networking SOC, based on mature experience, ADM8211 is designed as hardwired architecture to reach the cost effective target.

With the features of SRAM-needless, power saving, WEP/fix, small-package...etc. ADM8211 is versatile for WLAN system manufacturers to develop IEEE 802.11b wireless product.



2 Features

2.1 Host PCI interface

- Provides 32-bit PCI bus master data transfer
- Supports network operation with PCI system clock from 22 MHz to 33MHz
- Provides performance meter, PCI bus master latency timer, for tuning the threshold to enhance the performance
- Provides burst-transmit packet interrupt and transmit/receive early interrupt to reduce host CPU utilization.
- Supports memory-read, memory-read-line, memory-read-multiple, memory-write, memory-write-and-invalidate command while being bus master
- Supports big or little endian byte ordering
- Arbitration between DMA channel to minimize underflow or overflow

2.2 Industry standard

- PCI 2.2 /Cardbus interface
- ACPI and PCI power management 1.1 standard compliant
- IEEE802.11, IEEE802.11b

2.3 802.11 MAC

- MAC implements with State Machine
- No External SRAM needed
- Support auto-fallback from 11Mbps to 5.5, 2 and 1Mbps.
- Support Infrastructure, Ad-hoc under Distributed Coordination Function (DCF)
- Implementation the Point Coordination Function (PCF) operation
- RTS/CTS generation, Fragmentation, Beacon monitor/loss detection/generation.
- RX DA address filtering (multicast) with 64 entries.
- TIM (Traffic Indication Map) field decoding at Beacon frame reception
- Support DSSS (Direct Sequence Spread Spectrum) PHY.
- Front end chip power sequence control

2.4 WEP

- Internal encryption engine for WEP function, RC4, 40/104 bits key length selectable.

- Randomly generated IV (Initialization Vector) for TX.
- ICV (Integrity Check Value) generation and check.
- 4 default shared key supported.
- TA/RA WEP individual key management with a 20-entry table.

2.5 WLAN TX/RX FIFO

- Provides two independent long FIFOs with 4k bytes each for transmission and receiving
- Bus master descriptor based host memory access
- Pre-fetch up to two transmit packets to guarantee standard inter frame space (IFS)
- Re-transmits no-ACKed packet without reloading from host memory.
- Support two TX descriptors for DCF and PCF application
- Automatically re-transmitting if TX under-run happened.

2.6 WLAN Synthesizer Interface

- Support RFMD compatible interface

2.7 EEPROM Interface

- Provides serial interface for read/write 93C46/93C66 EEPROM
- Automatically loads device ID, vendor ID, subsystem ID, subsystem vendor ID, Maximum-Latency, and Minimum-Grand from the 64 byte contents of 93C46/93C66 after PCI reset de-asserted in PCI environment.
- CIS data is recalled from 93C66 through ADM8211 in CARDBUS environment.

2.8 LED Display

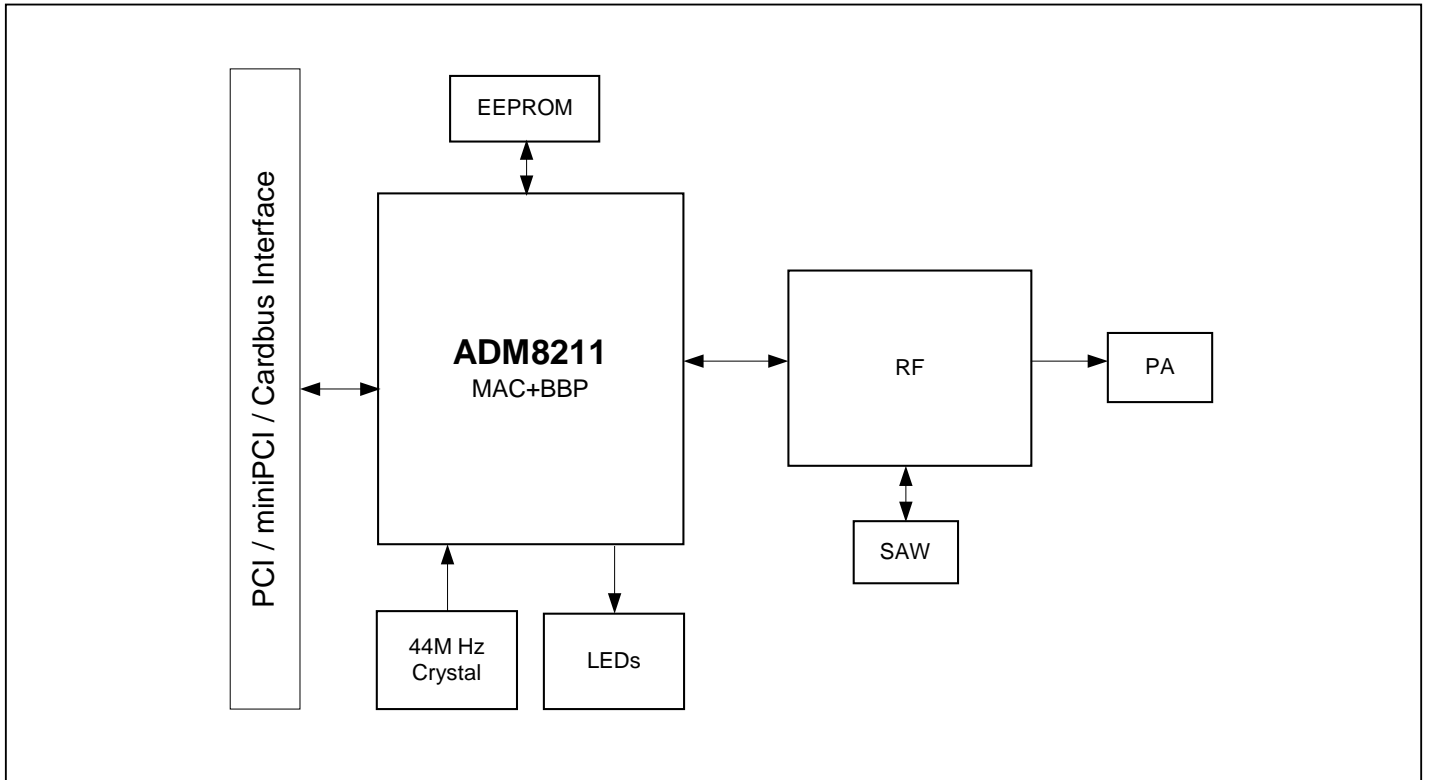
- Power: Power on indication
- Link: Keep on while link
- Activity: Blinking at 10Hz while activity

2.9 Miscellaneous

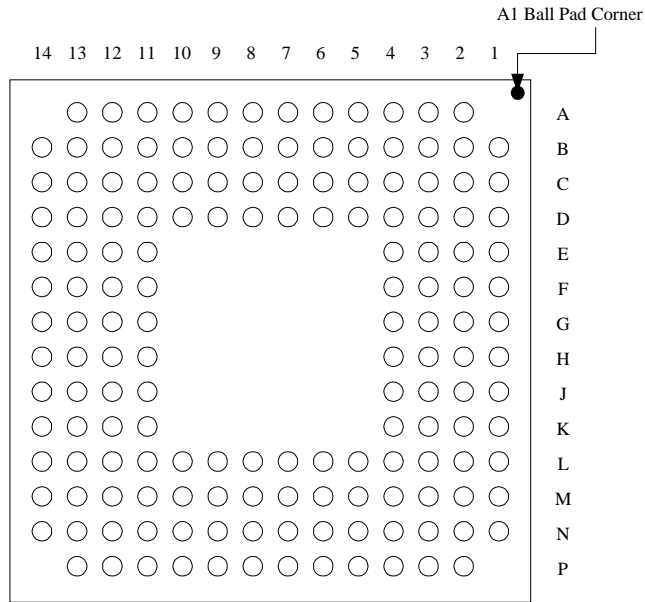
- Low power application
- Support 3 GPIO pins
- CMOS .25um Process
- Provides 156/BGA package
- On chip 3.3V ~ 2.5V regulator
- 3.3V power supply with 5V/3.3V I/O tolerance

3 Application Diagram

* Please refer to schematic provided by ADMtek



4 Pin Assignment Diagram



Bottom View
156-Pin BGA

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A		VSS					PA_PE	PE1	PE2	VD33	EECS	EEDI	LEDACT	
B	VDDA	GND A			LE_IF#	SYNDATA	SYNCLK		VD33	VD33	EECK	EEDO		VSSPST
C	Q_in	I_in	RXVGC						MCLK			LEDLINK	OSC440	CLK_44
D	Q_out	I_out	TXVGC	LNA_GS			GNDD	VDDD			VSSPST	VSSPST	OSC44I	GPIO3
E		VREF	ANTSEL								VSSPST	BW_SEL	VSSPST	VSSPST
F		VDDA	GND A	VD33							VSSPST	GPIO1		
G	VSS	INTA#	VSS	VSSPST							VSENSE	VSA	VCTL	VDDAH
H	REQ#	PCI-CLK		VD33							VD33	VSSPST	VAUX3.3	AD0
J	AD31	PME#/ CSTSCHG	VDD	VD33							AD2	AD1	VCC_DETECT	CLKRUN
K	GNT#	VSSPST	VSSPST	RST#							AD5	AD3	VSSPST	VD33
L	AD28	AD29	AD30	AD17	AD26	AD20	AD25	DEVSEL#	AD16	AD9	AD12	AD11	AD4	AD6
M	VDD	FRAME#	VDD	VDD	AD27	VD33	VSSPST	AD13	PERR#	STOP#	AD15	VSS	AD8	C-BEB0
N	AD24	C-BEB3	AD22	VDD	C-BEB2	VSS	AD18	SERR#	VSS	VD33	PAR	VSS	AD14	AD7
P		IDSEL	AD23	AD19	AD21	IRDY#	TRDY#	VSSPST	VSSPST	PCI/CB	VD33	C-BEB1	AD10	

5 Pin Description

5.1 PCI Interface

Pin	Name	Type	Description
G2	INTA#	O/D	PCI interrupt acknowledge.
K4	RST#	I	PCI reset signal, at least 100 μ s. During the reset period, all the output pins of ADM8211 will be set to tri-state and all the O/D pins are floated.
H2	PCI-CLK	I	This PCI clock inputs to ADM8211. The bus signals are recognized on rising edge of PCI-CLK. The frequency range of PCI-CLK is limited between 20MHz and 33MHz.
K1	GNT#	I	This signal indicates that the bus request of ADM8211 have been accepted.
H1	REQ#	O	Bus master device request.
J2	PME# / CSTSCHG	I/O	The Power Management Event signal is an open drain, active low signal for PCI (PME#) When CSR18.bit19 is set into "1", means that the ADM8211 is set into Power Save mode. In this mode, when the ADM8211 receives a Beacon (TIM) or ATIM frame from network then the ADM8211 will active this signal too.
J1 L3 L2 L1 M5 L5 L7 N1 P3 N3 P5 L6 P4 N8 L4 L9 M11 N13 M8 L11 M12 P13	AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10	I/O	Multiplexed address data pin of PCI Bus

L10	AD9		
M13	AD8		
N14	AD7		
L14	AD6		
K11	AD5		
L13	AD4		
K12	AD3		
J11	AD2		
J12	AD1		
H14	AD0		
N2	C-BEB3	I/O	Bus command and byte enable
N5	C-BEB2		
P12	C-BEB1		
M14	C-BEB0		
P2	IDSEL	I	Initialization Device Select. This signal is asserted when host issues the configuration cycles to the ADM8211.
M2	FRAME#	I/O	Begin and duration of bus access, driven by master device
P6	IRDY#	I/O	Master device is ready to data transaction
P7	TRDY#	I/O	Slave device is ready to data transaction
L8	DEVSEL#	I/O	Device select, target is driving to indicate the address is decoded
M10	STOP#	I/O	Target device request the master device to stop the current transaction
M9	PERR#	I/O	Data parity error is detected, driven by the agent receiving data
N8	SERR#	O/D	Address parity error
N11	PAR	I/O	Parity, even parity (AD[31:0] + C/BE[3:0]), master drives par for address and write data phase, target drives par for read data phase
J14	CLKRUN	I/O O/D	Clock Run for PCI system. In the normal operation situation, Host should assert this signal to indicate ADM8211 about the normal situation. On the other hand, when Host will deassert this signal when the clock is going down to a nonoperating frequency. When ADM8211 recognizes the deasserted status of clk-run, then it will assert clk-run to request host to maintain the normal clock operation. When clk-run function is disabled then the ADM8211 will set clk-run in tri-state.
P10	PCI/CB	I	Bonding low to select CARD bus mode. Internal pull up. 5V-tolerant

5.2 EEPROM Interface

Pin	Name	Type	Description
B11	EECK	I/O	ECK: Clock output to serial EEPROM. pull-up, 5V tolerant
A12	EEDI	I/O	EDI: Data output to serial EEPROM. pull-up, 5V tolerant

B12	EEDO	I/O	EDO: Data input from serial EEPROM pull-up, 5V tolerant
A11	EECS	O	Chip Select of serial EEPROM Pull-down, 5V tolerant

5.3 Serial Interface to Synthesizer

Pin	Name	Type	Description
B5	LEIF#	O, pull-up	Synthesizer 2 Chip Select
B7	SYNCLK	O, pull-up	Clock
B6	SYNDATA	O, pull-up	Data

5.4 RF I/F

Pin	Name	Type	Description
A8	PE1	O, pull-up	Power enable 1
A9	PE2	O, pull-up	Power enable 2
E12	BW_SEL	O	Channel 14 control pin
A7	PA_PE	O, pull-up	Transmit PA Power Enable
C1	Q_in	I	Analog Q input
D1	Q_out	O	Analog Q output 1.6V-1.8V
C2	I_in	I	Analog I input
D2	I_out	O	Analog I output 1.6V-1.8V

5.5 LED display, GPIO

Pin	Name	Type	Description
C12	LEDLINK	O, pull-up	LED Drive. 10 Hz blinking while either of following 2 conditions effective, even at D3-Cold. (1) Association successful with AP (2) Beacon reception when join IBSS
A13	LEDACT	O, pull-up	LED Drive. 10 Hz blinking while TX/RX Frame is detected
F12	GPIO1	I/O	General-purpose I/O pins, refer to GPIOEN setting (CSR11A). Pull-up, 5V tolerant
D14	GPIO3	I/O	General-purpose I/O pins, capable of event, rise/fall edge or toggle, capturing to generate interrupt to host, if enabled. Pull-up, 5V tolerant

5.6 Miscellaneous

Pin	Name	Type	Description
H13	Vaux3.3	I, Schmitt 5V tolerant	When asserted, it indicates an auxiliary power source is supported ACPI purpose, for detecting the auxiliary power source.
J13	VDD_detect	I, Schmitt 5V tolerant	When asserted, it indicates PCI power source is supported. ACPI purpose, for detecting the main power is remained or not, this pin should be connected to PCI bus power source +3.3V.

5.7 On chip regulator Pins

Pin	Name	Type	Description
G13	REGCTL	I/O	Regulator control pin
G12	VSA	Power	GND for regulator
G14	VDDAH	Power	3.3V for regulator
G11	VSENSE	I	2.5V sense input

5.8 Digital Power Pins

Pin	Name	Type	Description
F4, H4, J4, M6, B9, A10, B10, H11, N10, P11, J14	VDD33	Power	3.3V for IO
K2, K3, G4, M7, P8, P9, D11, E11, F11, D12, H12, E13, K13, B14, E14	VSSPST	Power	Gnd for IO
G1, M1, J1, M3, M4, N4, M12, N12	VDD	Power	2.5V for core
A2, G3, N6, N9,	VSS	Power	Gnd for core
D8	VDDD	Power	Vcc for BBP (leave open)
D7	GNDD	Power	Gnd for BBP

5.9 Analog Power Pins

Pin	Name	Type	Description
B1, F2	VDDA	Power	3.0V for BBP
B2, F3	GNDA	Power	Analog Gnd for BBP

5.10 Clock Pins

Pin	Name	Type	Description
A13	OSC44I	I	44 MHz clock input
C13	OSC44O	O	44 MHz clock output
C14	CLK44	O, pull-up	Buffered 44Mhz clock output This signal will be stopped, forced low, during MAC enter into power saving mode.

6 Electrical Specifications and Timings

6.1 Absolute Maximum Ratings

Supply Voltage (VDD)	-0.3 V to 3.6 V
DC Input Voltage (VIN)	-0.5 V to VDD+0.5V
DC Output Voltage (VOUT)	-0.5 V to VDD+0.5V
Storage Temperature	-65 C to 150 C
Ambient Temperature	0 C to 70 C
ESD Rating	2000V

6.2 Operating Condition

Symbol	Parameter	Condition	Min	Max	Units
VDD	Supply Voltage		3.0	3.6	V

6.3 DC Specifications

Symbol	Parameter	Condition	Min	Max	Units
V _{ih}	Input High Voltage		2.0		V
V _{il}	Input Low Voltage			0.8	V
I _{ih}	Differential Input Sensitivity		0.1		V
V _{cm}	Differential Common Mode Range		0.8	2.5	V
V _{oh}	Output High Voltage		2.8	3.6	V
V _{ol}	Output Low Voltage		0.0	0.3	V
V _{crs}	Output Signal Crossover Voltage		0.8	2.5	V

6.4 EEPROM Interface DC specification

Standard Vcc (4.5V to 5.5V) DC Specification

Symbol	Parameter	Condition	Min	Max	Units
V _{ih}	Input High Voltage		2.0	V _{cc} +1	V
V _{il}	Input Low Voltage		-0.1	0.8	V
I _{ih}	Input High Leakage Current	0 < V _{in} < V _{cc}		1	μA
I _{il}	Input Low Leakage Current	0 < V _{in} < V _{cc}		-1	μA
V _{ol}	Output Low Voltage	I _{oH} = -10 μA	V _{cc} -0.2		V
V _{oh}	Output High Voltage	I _{oL} = 10 μA		0.2	V
C _{in}	Input Pin Capacitance			5	pF

Low Vcc (2.7V to 5.5V) DC Specification

Symbol	Parameter	Condition	Min	Max	Units
V _{ih}	Input High Voltage		0.8V _{cc}	V _{cc} +1	V
V _{il}	Input Low Voltage		-0.1	0.15V _{cc}	V
I _{ih}	Input High Leakage Current	0 < V _{in} < V _{cc}		1	μA
I _{il}	Input Low Leakage Current	0 < V _{in} < V _{cc}		-1	μA
V _{oh}	Output High Voltage	I _{oh} = -10 μA	0.9V _{cc}		V
V _{ol}	Output Low Voltage	I _{ol} = 10 μA		0.1V _{cc}	V
C _{in}	Input Pin Capacitance			5	pF

6.5 GPIO Interface DC Specification

Symbol	Parameter	Condition	Min	Max	Units
V _{ih}	Input High Voltage		2.0		V
V _{il}	Input Low Voltage			0.8	V
I _{ih}	Input High Leakage Current	0 < V _{in} < V _{cc}		10	μA
I _{il}	Input Low Leakage Current	0 < V _{in} < V _{cc}		-10	μA
V _{oh}	Output High Voltage	I _{oh} = -4 mA	2.4		V
V _{ol}	Output Low Voltage	I _{ol} = 4 mA		0.4	V

6.6 Reset Timing

ADM8211 can be reset either by hardware, software or USB reset.

- A hardware reset is accomplished by asserting the RST# pin after power up the device. It should have a duration of at least 50 ms to ensure the external 48MHz crystal is in stable and correct frequency. All registers will be reset to default values.
- A software reset is accomplished by setting the reset bit. This software reset will reset all registers to default values.

6.7 EEPROM Interface Timing Specification

Symbol	Parameter	Min	Max	Units
t _{EESK}	EESK Clock Frequency	0	1	MHz
T _{EECSS}	EECS Setup Time to EESK	0.2		μs
T _{EECSH}	EECS Hold Time from EESK	0		ns
T _{EEDO}	EEDO Hold Time from EESK	70		ns
T _{EEDOP}	EEDO Output Delay to "1" or "0"		2	μs

t_{EEDIS}	EEDI Setup Time to EESK	0.4		μs
t_{EEDIH}	EEDI Hold Time from EESK	0.4		μs

7 Package

Package: 156-pin BGA

Dimension: 15mm*15mm*1.81mm

