ADM8513

USB-to-10/100 Mbps Ethernet LAN Controller

Feature

Industrial Standard

IEEE 802.3/802.3u 10Base-T/100Base-Tx compliant.

Support for IEEE 802.3x flow control.

Support Auto-Negotiation for 10Base-T and 100Base-Tx

USB specification 1.0 and 1.1 compliant.

USB Interface

USB specification 1.0 and 1.1 compliant

Full-Speed USB Device

Supports 1 USB configuration and 1 interface

Supports all USB standard commands

Supports two vendor specific commands

Supports USB Suspend/Resume detection logic

Supports 4 endpoints: 1 control endpoint with maximum 8-byte packet, 1 bulk IN endpoint with maximum 64-byte packet, 1 bulk OUT endpoint with maximum 64-byte packet and 1 interrupt IN endpoint with maximum 8-byte packet

MAC/PHY

Integrate the PHY by using address 1

Support configurable threshold for PAUSE frame.

Support Auto-Negotiation

Provide transmit wave-shaper, receive filter, and adapter equalizer.

Provide MLT-3 transceiver with DC restoration for Base-Line wander.

Support external transmit/receive transformer with turn ration 1:1.

EEPROM Interface

Provide serial interface to access 93c46 EEPROM

Automatically load device ID, vendor ID from EEPROM after power-on reset.

FIFO

Synchronous SRAM.

Internal 2K-byte two port asynchronous SRAM.

LED interface

2 LED operation modes

LED0: speed indication for 10Mbps or 100Mbps

LED1: link indication.

LED2: full duplex indication.

- **Support Power Save Function @ USB suspend mode**

  Mode 0 : Resume by remote wakeup or host resume when OS goes into standby

  Mode 1 : Resume by host when OS goes into standby

- **Miscellaneous**

  Support 6 GPIO pins.

  Provide 48-pin LQFP package.

  3.3V power supply with 5V/3.3V I/O tolerance.

- **Support Driver.**

  Win98/ME/2000/XP

  Linux driver, WinCE 3.0&4.0 driver

  Manufacturing test utilities :

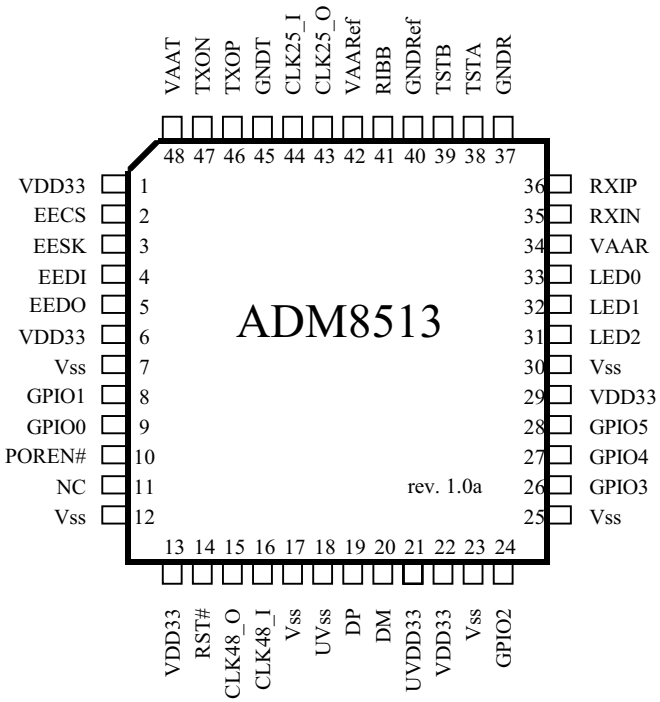
  EEPROM Burn-in program

  MFG testing program

Revision History:

Revision	Date	Description
0.1	Dec-2001	1. Preliminary
1.0	Jan-2002	1. Rearrange
1.1	June-2002	1. VAARef I/O is power pin, not input pin in P.7 2. GNDRef I/O is power pin, not input pin in P.7 3. Modify Pin Assignment Diagram P.5 4. Make small correction on P1, P2 , P5, P10, P13, P17, P19, P35, P37, P38
1.2	June-2002	1. Remove power consumption @ mode 1 in P.2 2. Change power consumption in P.33 3. Add layout guide in Appendix A

❖ Pin Assignment Diagram



❖ Pin Description

HOST Interface			
Name		I/O	Description
CLK48_I	16	I	48Mhz Clock Input from crystal or oscillator.
CLK48_O	15	O	Output for crystal.
RST#	14	I	External Hardware Reset Input, schmitt trigger, internal pull high
DM	20	I/O	USB Data Minus pin.
DP	19	I/O	USB Data Plus pin.
Physical Interface			
RXIP, RXIN	36,35	I	Rx input
TXOP, TXON	46,47	O	Tx Out
CLK25_I	44	I	Crystal In, 25Mhz
CLK25_O	43	O	Crystal Out, 25Mhz
RIBB	41	I	Reference Bias Resistor, tied to external 10K(1%) resistor to ground
TSTA, TSTB	38,39	O	Test Output Pin
LED Interface			
LED0	33	O	LED display for 100M b/s or 10M b/s speed. Active low indicates 100Base-TX, active high indicates 10 BaseT.
LED1	32	O	LED display for link and activity status. Active low when link is established.
LED2	31	O	LED display for Full Duplex or Collision status. Active low indicates full duplex, high indicates collision in half duplex.

Note:
The LED interface is EEPROM-programmable, 2 bit EEPROM control bit, Address 0B[7:6] at EEPROM, is used to select LED mode, the default setting are:
(1) LED0: 100Mbps(on, drive '0') or 10Mbps(off, drive '1')
(2) LED1: link (keeps on when link ok) or activity (blink with 10Hz when Pegasus II is receiving or transmitting but not collision)
(3) LED2: full duplex (keeps on when in full duplex mode) or collision (blink with 20Hz when colliding)
(4) All LED pins will be tri-state when using external PHY (offset 81h with bit[4:2] = 3'b001)

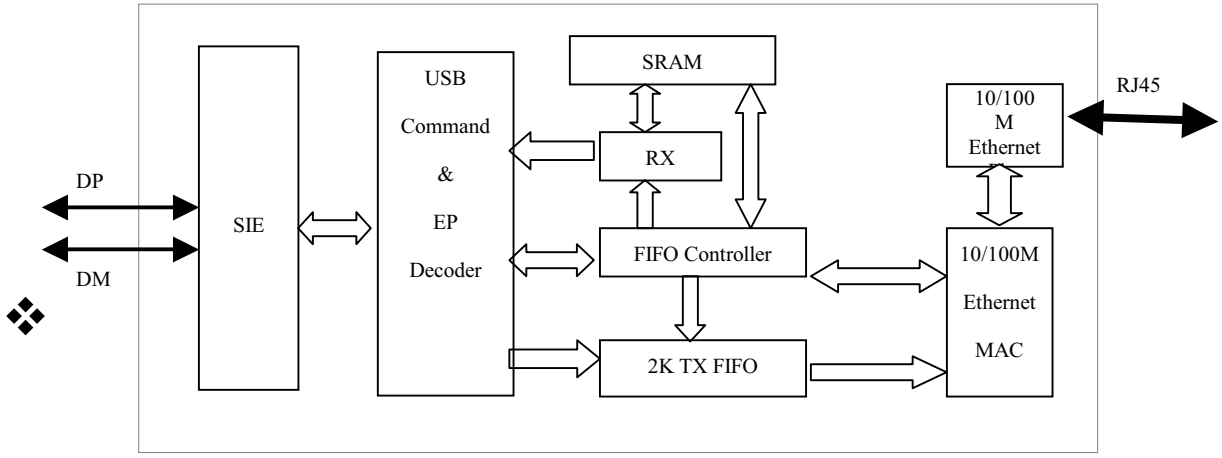
Mapping between LED action and EEPROM 0B[7:6] setting:

EEPROM 0B [7:6]	LED	Action
0,0	LED0	10/100(OFF/ON)
	LED1	LINK/ACTIVITY (ON / Flash)
	LED2	FULL DUP/COL (ON / Flash)
0,1	LED0	ACTIVITY when LINK (Flash)
	LED1	LINK 10(ON)
	LED2	LINK 100(ON

EEPROM Interface

EECS	2	O	EEPROM Chip Select This enables the EEPROM during loading of the Ethernet configuration data.
			CMOS I/O with 5V tolerant, 2mA
EEDI	4	O	EEPROM Data In The MAC will use this pin to serially write opcodes, addresses and data into the serial EEPROM.
			CMOS I/O with 5V tolerant, 2mA
EEDO	5	I	EEPROM Data Out, internal pull low The MAC will read the contents of the EEPROM serially through this pin.
			Input, pull down, 5V tolerant
EESK	3	O	EEPROM Clock After reset, the MAC if configured, will read the contents of the EEPROM using EESK, EEDO, and EEDI. This pin provides the clock for the EEPROM.
			CMOS I/O with 5V tolerant, 2mA
Miscellaneous			
GPIO[5:0]	9,8,24,26,27,28	I/O	These pins are used as general purpose Input/Output pins and offset 0A[1] = 0 in EEPROM. Default is internal pull-low
POREN#	10	I	Internal Power On Reset Logic Enable. Default is enable and internal pull - low. When external hardware reset is used, this pin should be connected to Vcc via 4.7k resistor.
NC	11	X	No connection
POWER USB			
UVDD 33	21	Power	3.3v power supply for USB transceiver
UVSS	18	Power	Ground for USB transceiver
Power			
VDD 33	1,6,13,22,29	Power	3.3v power supply
VSS	7,12,23, 17,25,30	Power	Ground
VAARef	42	power	+3.3V Power Supply for Phy
GNDRef	40	power	+3.3V Power Ground for Phy
VAAT	48	Power	+3.3V for transmitter
GNDT	45	Power	Gnd for Transmitter
VAAR	34	Power	+3.3V for receiver
GNDR	37	Power	Gnd for receiver

❖ Block Diagram



❖ Register Description

● System Register Table & Description

Offset	Register
00-02h	Ethernet control registers
03-07h	reserved
08-0Fh	multicast address table registers
10-15h	Ethernet ID registers
16-17h	Reserve
18-19h	pause_timer registers
1Ah	receive packet number based flow control register
1Bh	occupied receive FIFO based flow control register
1C-1Fh	reserved
20h	EEPROM offset register
21-22h	EEPROM data registers
23h	EEPROM access control register
24h	reserved
25h	PHY address register
26-27h	PHY data registers
28h	PHY access control register
29h	reserved
2Ah	USB status register
2B-2Ch	Ethernet transmit status registers
2Dh	Ethernet receive status register
2E-2Fh	Ethernet receive lost packet count register
30-3Fh	Wakeup frame 0 mask registers
40h	Wakeup frame0 offset register
41-42h	Wakeup frame0 CRC registers
43-47h	reserved
48-57h	Wakeup frame 1 mask registers
58h	Wakeup frame 1 offset register
59-5Ah	Wakeup frame 1 CRC registers
5B-5Fh	reserved
60-6Fh	Wakeup frame 2 mask registers
70h	Wakeup frame 2 offset register
71-72h	Wakeup frame 2 CRC registers
73-77h	reserved
78h	Wakeup control register
79h	reserved
7Ah	Wakeup status register
7Bh	PHY control register
7Ch	GPIO[5:4] control register
7Dh	Reserved
7E-7Fh	GPIO control register
80h	TEST register
81h	Test mode
82-FFh	reserved

■ offset 00h: Ethernet control_0

Bit	Field	HW access	SW access	Default value	Description
7	tx_en	R	R/W	0	Enable Ethernet transmission.
6	rx_en	R	R/W	0	Enable Ethernet receive.
5	rx_flowctl_en	R	R/W	0	Enable receive pause frame.
4	wakeon_en	R	R/W	0	Enable wake-on-LAN mode.
3	rxstatus_append	R	R/W	1	Enable status append at the end of received packet.
2	stop_back_off	R	R/W	0	1: back-off counter stop when carrier is active and resume when carrier drop. 0: back-off counter isn't affected by carrier.
1	rx_multicast_all	R	R/W	0	Receive all multicast packet
0	rx_crc_sent	R	R/W	1	Include CRC in receive packet.

■ offset 01h: Ethernet control_1

Bit	Field	HW access	SW access	Default value	Description
7	reserved				
6	reserved				
5	full_duplex	R	R/W	0	1: full-duplex mode. 0: half-duplex mode.
4	10mode	R	R/W	0	0: 10Base-T mode. 1: 100Base-T mode.
3	reset_mac	R	R/W	0	Reset MAC, After write 1, HW will clear this bit after MAC reset.
2	MII_mode	R	R	0	0: MII mode.
0-1	reserved				

■ offset 02h: Ethernet control_2

Bit	Field	HW access	SW access	Default value	Description
7	Max Ethernet pkt length	R	R/W	0	Max Ethernet pkt length: 0: 1528 bytes, 1: 1638 bytes, Default is 0.
6	reserved				
5	load EEPROM start	R	R/W	0	When this bit is written with 1, HW will start to load EEPROM.
4	EEPROM write enable/disable	R	R/W	0	1: EEPROM write command 0: EEPROM write enable/disable command
3	loop_back	R	R/W	0	Enable MAC loop back mode
2	promiscuous	R	R/W	0	1: receive any packet. 0: receive packets which pass the address filter.
1	rx_bad_pkt	R	R/W	0	1: receive bad packets which pass the address filter. 0: filter all bad packet
0	Ep3_rd_clr	R	R/W	0	1: Once EP3 is accessed, those registers(2B-2F, 7A) will be cleared. 0: Access EP3, no effect to those registers.

Multicast address

offset	Bit	Field	HW access	SW access	Default value	Description
08h	7-0	multicast0	R	R/W	0	Multicast address byte 0 (hash table[7:0]).
09h	7-0	multicast1	R	R/W	0	Multicast address byte 1 (hash table[15:8]).
0Ah	7-0	multicast2	R	R/W	0	Multicast address byte 2 (hash table[23:16]).
0Bh	7-0	multicast3	R	R/W	0	Multicast address byte 3 (hash table[31:24]).
0Ch	7-0	multicast4	R	R/W	0	Multicast address byte 4 (hash table[39:32]).
0Dh	7-0	multicast5	R	R/W	0	Multicast address byte 5 (hash table[47:40]).
0Eh	7-0	multicast6	R	R/W	0	Multicast address byte 6 (hash table[55:48]).
0Fh	7-0	multicast7	R	R/W	0	Multicast address byte 7 (hash table[63:56]).

EthernetID

offset	Bit	Field	HW access	SW access	Default value	Description
10h	7-0	etherid0	R/W	R/W	0	The 1st byte of ethernet ID is automatically loaded from EEPROM after HW reset.
11h	7-0	etherid1	R/W	R/W	0	The 2nd byte of ethernet ID.
12h	7-0	etherid2	R/W	R/W	0	The 3rd byte of ethernet ID.
13h	7-0	etherid3	R/W	R/W	0	The 4th byte of ethernet ID.
14h	7-0	etherid4	R/W	R/W	0	The 5th byte of ethernet ID.
15h	7-0	etherid5	R/W	R/W	0	The 6th byte of ethernet ID.

■ offset 18h: pause_timer low

Bit	Field	HW access	SW access	Default value	Description
7-0	pause_timer	R	R/W	0F	The [11:4] of pause time in the PAUSE frame.

■ offset 1Ah: receive packet number based flow control

Bit	Field	HW access	SW access	Default value	Description
7	reserved				
6-1	pkt_no	R	R/W	6'h0F	This field specifies the threshold for transmitting the PAUSE frame. As the received packet number is more than or equal to this field, the PAUSE frame is sent automatically by HW.
0	flowctl_pkt	R	R/W	0	Enable pause frame transmission bases on receive packet number.

■ offset 1Bh: occupied receive FIFO based flow control

Bit	Field	HW access	SW access	Default value	Description
7	reserved				
6-1	rxsize	R	R/W	6'h0F	This field specifies the K byte threshold for transmitting the PAUSE frame. As the received FIFO is occupied than or equal to this field, the PAUSE frame is sent automatically by HW. If this field =2, as receive FIFO is occupied more than or equal to 2K byte, the PAUSE frame is transmitted.
0	flowctl_rxsize	R	R/W	0	Enable pause frame transmission bases on occupied receive FIFO size.

■ offset 1Ch :EP1 control

Bit	Field	HW access	SW access	Default value	Description
7	ep1_send0_en	R	R/W	0	1: enable EP1 send 1-byte 00 when more than frame_interval's NAK is received 0: disable EP1 send 1-byte 00 function
6-5	frame_interval_detail	R	R/W	2'b00	This value is the detail scale of frame interval, it is from 0ms to 3ms. 2'b00: for more than 0 plus frame_interval ms NAK, EP1 sends 1-byte 00 2'b01: for more than 1 plus frame_interval ms NAK, EP1 sends 1-byte 00 2'b11: for more than 3 plus frame_interval ms NAK, EP1 sends 1-byte 00

4-0	frame_interval	R	R/W	5'd4	This value multiply with 4 is the frame interval, it is from 4ms to 124ms. 5'd1: for more than 4 ms NAK, EP1 sends 1-byte 00 5'd2: for more than 8 ms NAK, EP1 sends 1-byte 00 5'd31: for more than 124ms NAK, EP1 sends 1-byte 00

■ offset 1Dh: Reserved

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5-0	reserved				

■ offset 1E: Reserved

Bit	Field	HW access	SW access	Default value	Description
7-0	reserved				

■ offset 20h: EEPROM offset

Bit	Field	HW access	SW access	Default value	Description
7-6	Reserved				
5-0	rom_offset	R	R/W	0	SW sets this register when access to EEPROM.

■ offset 21h: EEPROM data low

Bit	Field	HW access	SW access	Default value	Description
7-0	romdata_lo	R/W	R/W	0	SW sets this register when writes to EEPROM. HW sets this register when read data from EEPROM.

■ offset 22h: EEPROM data high

Bit	Field	HW access	SW access	Default value	Description
7-0	romdata_hi	R/W	R/W	0	SW sets this register when writes to EEPROM. HW sets this register when reads data from EEPROM.

■ offset 23h: EEPROM access control

Bit	Field	HW access	SW access	Default value	Description
7-3	reserved				
2	done	R/W	R/W	0	Set by HW to indicate successful completion of EEPROM access. Clear by SW when initiate a new access to EEPROM

1	rd_eeprom	R	R/W	0	Set by SW to initiate a read access to EEPROM. SW sets this bit after it well setting the rom_offset.
0	wr_eeprom	R	R/W	0	Set by SW to initiate a write access to EEPROM. SW set this bit after it well setting the rom_offset, romdata_lo and romdata_hi.

■ offset 25h: PHY address

Bit	Field	HW access	SW access	Default value	Description
7-5	reserved				
4-0	phy_addr	R	R/W	0	MII PHY address.

■ offset 26h: PHY data low

Bit	Field	HW access	SW access	Default value	Description
7-0	phydata_low	R/W	R/W	0	SW set this register when write to phy registers. HW set this register when read data from PHY register.

■ offset 27h: PHY data high

Bit	Field	HW access	SW access	Default value	Description
7-0	phydata_high	R/W	R/W	0	SW set this register when write to phy registers. HW set this register when read data from PHY register.

■ offset 28h: PHY access control

Bit	Field	HW access	SW access	Default value	Description
7	done	R/W	R/W	0	Set by HW to indicate successful completion of PHY access. Clear by SW when initiate a new access to PHY.
6	rd_phy	R	R/W	0	Set by SW to initiate a read access to PHY register. SW set this bit after it well setting the phy_addr and phyreg_addr.
5	wr_phy	R	R/W	0	Set by SW to initiate a write access to PHY register. SW set this bit after it well setting the phy_addr, phyreg_addr and phyreg_data.
4-0	phyreg_addr	R	R/W	0	PHY register address.

■ offset 2Ah: usb bus status

Bit	Field	HW access	SW access	Default value	Description
7-2	reserved				
1	usb_resume	R/W	R/W	0	Set by HW to indicate usb bus in resume state. Clear by SW read this register.
0	usb_suspend	R/W	R/W	0	Set by HW to indicate usb bus in suspend state. Clear by SW read this register.

■ offset 2Bh: transmit status_1

Bit	Field	HW access	SW access	Default value	Description
7	txunderrun	R/W	R	0	Set by HW to indicate tx underrun error. Clear by SW read this register or after EP3 is accessed.
6	excessive_col	R/W	R	0	Set by HW to indicate excessive collision. Clear by SW read this register or after EP3 is accessed.
5	late_col	R/W	R	0	Set by HW to indicate late collision error. Clear by SW read this register or after EP3 is accessed.
4	no_carrier	R/W	R	0	Set by HW to indicate no carrier. Clear by SW read this register or after EP3 is accessed.
3	loss_carrier	R/W	R	0	Set by HW to indicate carrier loss. Clear by SW read this register or after EP3 is accessed.
2	jabber_timeout	R/W	R	0	Set by HW to indicate jabber time out. Clear by SW read this register or after EP3 is accessed.
1-0	reserved				

■ offset 2Ch: transmit status_2

Bit	Field	HW access	SW access	Default value	Description
7	txfifo_full	R/W	R	0	Set by HW to indicate tx fifo full. Clear by SW read this register or after EP3 is accessed.
6	txfifo_empty	R/W	R	0	Set by HW to indicate tx fifo empty. Clear by SW read this register or after EP3 is accessed.
5-4	reserved				
3-0	txpkt_cnt	R/W	R	0	Set by HW to indicate Ethernet transmit packet count every interrupt EP polling. If more than 15 packets have been transmitted, this value will keep as 15. Clear by SW read or after EP3 is accessed.

■ offset 2Dh: receive status

Bit	Field	HW access	SW access	Default value	Description
7-2	reserved				
1	rx_pause	R/W	R/W	0	Set by HW to indicate a PAUSE frame is received. Clear by SW read this register or after EP3 is accessed.
0	rx_overflow	R/W	R	0	Set by HW to indicate external SRAM overflow. Clear by SW read this register or after EP3 is accessed.

■ offset 2Eh: receive lost packet count high

Bit	Field	HW access	SW access	Default value	Description
7	Lostpkt_	R/W	R/W	0	
6-0	rx_lostpkt	R/W	R/W	0	The [14:8] of lost packet counts due to receive FIFO overflow. Clear by SW read this register or after EP3 is accessed.

■ offset 2Eh: receive lost packet count low

Bit	Field	HW access	SW access	Default value	Description
7-0	rx_lostpkt	R/W	R/W	0	The [7:0] of lost packet counts due to receive FIFO overflow. Clear by SW read this register or after EP3 is accessed.

● wake-up frames

offset	Bit	Field	HW access	SW access	Default value	Description
30-3Fh		f0_mask				The 128 mask bits for fram0.
40h	7-0	f0_offset	R	R/W	0	Offset for wakeup frame0.
41h	7-0	f0_crc_low	R	R/W	0	The low byte of CRC16 match for frame 0.
42h	7-0	f0_crc_hi	R	R/W	0	The high byte of CRC16 match for frame 0.
43-47h		reserved				
48-57h		f1_mask				The 128 mask bits for fram1.
58h	7-0	f1_offset	R	R/W	0	Offset for wakeup frame1.
59h	7-0	f1_crc_low	R	R/W	0	The low byte of CRC16 match for frame 1.
5Ah	7-0	f1_crc_hi	R	R/W	0	The high byte of CRC16 match for frame 1.
5B-5Fh		reserved				
60-6Fh		f2_mask				The 128 mask bits for fram2.
70h	7-0	f2_offset	R	R/W	0	Offset for wakeup frame2.
71h	7-0	f2_crc_low	R	R/W	0	The low byte of CRC16 match for frame 2.
72h	7-0	f2_crc_hi	R	R/W	0	The high byte of CRC16 match for frame 2.
73-77h		reserved				

■ offset 78h: wake-up control

Bit	Field	HW access	SW access	Default value	Description
7	mgcpkt_en	R	R/W	0	Set by SW to enable magic packet wakeup function.
6	link_en	R	R/W	0	Set by SW to enable link status wakeup function.
5	wakeframe0_en	R	R/W	0	Set by SW to enable wakeup frame0 wakeup function.
4	wakeframe1_en	R	R/W	0	Set by SW to enable wakeup frame1 wakeup function.
3	wakeframe2_en	R	R/W	0	Set by SW to enable wakeup frame2 wakeup function.
2	crc16type	R	R/W	1	0: CRC-16 initial contents = 0000h 1: CRC-16 initial contents = ffffh
1-0	reserved				

■ offset 7Ah: wake-up status

Bit	Field	HW access	SW access	Default value	Description
7	rx_mgcpkt	R/W	R	0	Set by HW when receive a magic packet. Clear by SW read this register.
6	link_wake	R/W	R	0	Set by HW when link status change. Clear by SW read this register.

5	rx_wakeframe	R/W	R	0	Set by HW when receive a wakeup frame. Clear by SW read this register.
4-1	Reserved				
0	link_sts	R/W	R	0	Indicate the current link status, 1 for link on, 0 for link off.

■ offset 7Bh: PHY control

Bit	Field	HW access	SW access	Default value	Description
7-2	reserved				
1	enable_phy	R	R	0	0: disable 10/100 PHY 1: enable 10/100 PHY
0	phyrst	R	R/W	0	1: Reset PHY The PHY is reset when this bit is written with 1 and stops reset when this bit is written with 0.

■ offset 7Ch: GPIO[5:4]

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5	GPIO5_oe	R	R/W	0	GPIO5 output enable. 1: GPIO5 is used for output 0: GPIO5 is used for input
4	GPIO5_o	R	R/W	0	GPIO5 output value. When GPIO5 is used for output, this value is driven to GPIO5 pin. Set by SW.
3	GPIO5_i	R/W	R		GPIO5 input value. When GPIO5 is used for input, this field reflects the status of GPIO5. Default is pulled-down.
2	GPIO4_oe	R	R/W	0	GPIO4 output enable. 1: GPIO4 is used for output 0: GPIO4 is used for input
1	GPIO4_o	R	R/W	0	GPIO4 output value. When GPIO4 is used for output, this value id driven to GPIO4 pin. Set by SW.
0	GPIO4_i	R/W	R		GPIO4 input value. When GPIO4 is used for input, this field reflects the status of GPIO4. Default is pulled-down.

■ offset 7Eh: GPIO[1:0]

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5	GPIO1_oe	R	R/W	0	GPIO1 output enable. 1: GPIO1 is used for output 0: GPIO1 is used for input

4	GPIO1_o	R	R/W	0	GPIO1 output value. When GPIO1 is used for output, this value id driven to GPIO1 pin. Set by SW.
3	GPIO1_i	R/W	R		GPIO1 input value. When GPIO1 is used for input, this field reflects the status of GPIO1. Set by HW.
2	GPIO0_oe	R	R/W	0	GPIO0 output enable. 1: GPIO0 is used for output 0: GPIO0 is used for input
1	GPIO0_o	R	R/W	0	GPIO0 output value. When GPIO0 is used for output, this value id driven to GPIO0 pin. Set by SW.
0	GPIO0_i	R/W	R		GPIO0 input value. When GPIO0 is used for input, this field reflects the status of GPIO0. Set by HW.

■ offset 7Fh: GPIO[3:2]

Bit	Field	HW access	SW access	Default value	Description
7-6	reserved				
5	GPIO3_oe	R	R/W	0	GPIO3 output enable. 1: GPIO3 is used for output 0: GPIO3 is used for input
4	GPIO3_o	R	R/W	0	GPIO3 output value. When GPIO3 is used for output, this value id driven to GPIO3 pin. Set by SW.
3	GPIO3_i	R/W	R		GPIO3 input value. When GPIO3 is used for input, this field reflects the status of GPIO3. Set by HW.
2	GPIO2_oe	R	R/W	0	GPIO2 output enable. 1: GPIO2 is used for output 0: GPIO2 is used for input
1	GPIO2_o	R	R/W	0	GPIO2 output value. When GPIO2 is used for output, this value id driven to GPIO2 pin. Set by SW.
0	GPIO2_i	R/W	R		GPIO2 input value. When GPIO2 is used for input, this field reflects the status of GPIO2. Set by HW.

■ offset 80h: Reserved

Bit	Field	HW access	SW access	Default value	Description
7-0	reserved				

■ offset 81h: Reserved

Bit	Field	HW access	SW access	Default value	Description
7-0	reserved				

● Phy Register & Description

Register 0 (MII Control)

BIT	NAME	DESCRIPTION	Read/Write	DEFAULT
15	Reset	1 = PHY Reset 0 = normal operation	R/W, SC	0
14	Loopback	1 = enable loopback 0 = disable loopback	R/W	0
13	Speed selection	1 = 100Mbps/s 0 = 10 Mb/s	R/W	Pin - see note
12	Autonegotiation enable	1 = enable autoneg 0 = disable autoneg	R/W	Pin – see note
11	Power down	1 = Power Down 0 = normal operation	R/W	0
10	Isolate	1 = isolate PHY from MII 0 = normal operation	R/W	0
9	Restart autonegotiation	1 = Restart Autoneg	R/W, SC	0
8	Duplex mode	1 = full, 0 = half	R/W	Pin – see note
7	Collision test	Not implemented	RO	0 - see note
6:0	Reserved		RO	0000000

SC Self Clearing

Reset Reset this port only. This will cause the following:

1. Restart the autonegotiation process.

2. Reset the registers to their default values. Note that this does not affect registers 20, 22, 30 or 31. These registers are not reset by this bit to allow test configurations to be written and then not affected by resetting the port.

Note: No reset is performed to analogue sections of the port. There is also no physical reset to any internal clock synthesisers or the local clock recovery oscillator which will continue to run throughout the reset period. However since the port is restarted and autoneg re-run the process of locking the frequency of the local oscillator (slave) to the reference oscillator (master) will be repeated as it is at the start of any link initialization process.

Loopback Loop back of transmit data to receive via a path as close to the wire as possible. When set inhibits actual transmission on the wire.

Speed selection Forces speed of Phy only when autonegotiation is disabled. The default state of this bit will be determined by a power-up configuration pin in this case. Otherwise it defaults to 1.

Auto-neg enable Defaults to pin programmed value. When cleared allows forcing of speed and duplex settings. When set (after being cleared) causes re-start of autoneg process. Pin programming at power-up allows it to come up disabled and for software to

write the desired capability before allowing the first negotiation to commence.

Restart Negotiation only has effect when autonegotiating. Restarts state machine.

Power down Has no effect in this device. Test mode power down modes may be implemented in other specific modules.

Isolate Puts RMII receive signals into high impedance state and ignores transmit signals.

Duplex mode When bit12 is cleared (i.e. autoneg disabled), this bit forces full duplex (bit = 1) or half duplex (bit = 0).

Collision test Always 0 because collision signal is not implemented.

Register 1 (Status):

BIT	NAME	DESCRIPTION	Read/Write	Default
15	100 BASE T4	Not supported	RO	0
14	100BASE-X Full Duplex	1 = PHY is 100BASE-X full duplex capable 0 = PHY is not 100BASE-X full duplex capable	RO	1
13	100BASE-X Half Duplex	1 = PHY is 100BASE-X half duplex capable 0 = PHY is not 100BASE-X half duplex capable	RO	1
12	10Mbps/s Full Duplex	1 = PHY is 10Mbps/s Full duplex capable 0 = PHY is not 10Mbps/s Full duplex capable	RO	1
11	10 Mb/s Half Duplex	1 = PHY is 10Mbps/s Half duplex capable 0 = PHY is not 10Mbps/s Half duplex capable	RO	1
10	100BASE-T2 full duplex	Not supported	RO	0
9	100BASE-T2 half duplex	Not supported	RO	0
8-7	Reserved		RO	00
6	MF Preamble Suppression	1 = PHY can accept management frames with preamble suppression 0 = PHY cannot accept management frames with preamble suppression	RO	1
5	Autoneg Complete	1 = autoneg completed, 0 = autoneg incomplete	RO	0
4	Remote Fault	1 = remote fault detected, 0 = no remote fault detected	RO, LH	0
3	Autoneg Ability	1 = PHY can auto-negotiate, 0 = PHY cannot auto-negotiate	RO	1

2	Link Status	1 = link is up, 0 = link is down	RO, LL	0
1	Jabber Detect	1 = jabber condition detected	RO, LH	0(see note)
0	Extended Capability	1 = extended register capabilities, 0 = basic register set capabilities only	RO	1

LL Latch Low

LH Latch High

Jabber detect Only used in 10Base-T mode. Reads as 0 in 100Base-TX mode.

Register 2 and 3

Each PHY has an identifier, which is assigned to the device.

The identifier contains a total of 32 bits, which consists of the following: 22 bits of a 24bit organisationally unique identifier (OUI) for the manufacturer; a 6-bit manufacturer's model number; a 4-bit manufacturer's revision number. For an explanation of how the OUI maps to the register, please refer to IEEE 802-1990 clause 5.1

Register 2

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:0	PHY_ID[31-16]	OUI (bits 3-18)	RO	001D(Hex)

Register 3

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:10	PHY_ID[15-10]	OUI (bits 19-24)	RO	001001(bin)
9:4	PHY_ID[9-4]	Manufacturer's Model Number (bits 5-0)	RO	000001(bin)
3:0	PHY_ID[3-0]	Revision Number (bits 3-0); Register 3, bit 0 is LS bit of PHY Identifier	RO	0001(bin)

This uses the OUI of ADMtek, device type of 1 and rev 0.

Register 4

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15	Next Page	1 = Device set to use Next Page, 0 = Device not set to use Next Page	R/W	0
14	Reserved		RO	0

13	Remote Fault	1 = Local remote fault sent to link partner 0 = no fault detected	R/W	0
12:11	Not implemented	Technology ability bits A7-A6	RO	00
10	Pause	Technology ability bit A5	R/W	0
9	Not implemented	Technology ability bit A4	RO	0
8	100BASE-TX full duplex	Technology ability bit A3 1 = Unit is capable of Full Duplex 0 = Unit is not capable of Full Duplex	R/W	0
7	100BASE-TX half duplex	Technology ability bit A2 1 = Unit is capable of Half Duplex 0 = Unit is not capable of Half Duplex 100BASE-TX	R/W	0
6	10BASE-T full duplex	Technology ability bit A1 1 = Unit is capable of Full Duplex 10BASE-T 0 = Unit is not capable of Full Duplex 10BASE-T	R/W	0
5	10BASE-T half duplex	Technology ability bit A0 1 = Unit is capable of Half Duplex 10BASE-T 0 = Unit is not capable of Half Duplex 10BASE-T	R/W	0
4:0	Selector Field	Identifies type of message being sent. Currently only one value is defined.	RO	00001

Register 5

The register is used to view the advertised capabilities of the link partner once autonegotiation is complete. The contents of this register should not be relied upon unless register 1 bit 5 is set (autoneg complete). After negotiation this register should contain a copy of the link partner's register 4. All bits are therefore defined in the same way as for register 4.

All bits are read only.

This register is used for Base Page code word only.

Base Page Register Format

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15	Next Page	1 = Link Partner is requesting Next Page function 0 = Base Page is requested	RO	0
14	Acknowledge	Link Partner acknowledgement bit	RO	0
13	Remote Fault	Link Partner is indicating a fault	RO	0

12:5	Technology Ability	Link Partner technology ability field.	RO	00(hex)
4:0	Selector Field	Link Partner selector field	RO	00000

Register 6

BIT	NAME	DESCRIPTION	READ/WRITE	DEFAULT
15:5	Reserved		RO	000(hex)
4	Parallel Detection Fault	1 = Local Device Parallel Detection Fault 0 = No fault detected	RO, LH	0
3	Link Partner Next Page Able	1 = Link Partner is Next Page Able 0 = Link Partner is not Next Page Able	RO	0
2	Next Page Able	1 = Local device is Next Page Able 0 = Local device is not Next Page Able	RO	1
1	Page Received	1 = A New Page has been received 0 = A New Page has not been received	RO, LH	0
0	Link Partner Autonegotiation Able	1 = Link Partner is Autonegotiation able 0 = Link Partner is not Autonegotiation able	RO	0

LH Latch High

❖ Function Description

● USB Interface

USB is likely solution any time you want to use a computer to communication with devices outside the computer. The interface is suitable for one-of-kind and small-scale designs as well as mass-produced, standard peripheral. The benefits to USB are ease of use, fast and reliable data transfers, flexibility, low cost and power conservation.

SIE

SIE (Serial Interface Engine) is to control USB communications and check USB protocol, then transfer protocol to EP decoder. The SIE and USB transceivers, which provide the hardware interface to the USB cable, together comprise the USB engine.

USB Command & EP Decoder

The detail description is in " USB Command"

● FIFO Controller

FIFO Controller in receive path is in charge of:

(1) Store received Ethernet packets to SRAM and multiple packets can be stored to SRAM. If more than maximum packet counts are received or total packet size is more than the size of SRAM, the subsequent coming Ethernet packet will be discarded.

(2) FIFO controller will load data from SRAM to internal RX FIFO then inform EP Decoder that 64-byte data or a packet is ready in RX FIFO. Before FIFO controller inform this, any USB access to bulk IN endpoint will return NAK. This is to maintain the data transfer on USB bus via bulk IN transfer is continuous, thus a 64-byte internal RX FIFO is needed.

(3) If an Ethernet packet is being received and loading into SRAM while FIFO Controller is moving data from SRAM to internal RX FIFO, writing the Ethernet packet to SRAM will get the higher priority.

● TX FIFO and RX FIFO

RX FIFO is a one-port 64-byte FIFO and TX FIFO is a two-port 2K-byte FIFO

● 10/100M Ethernet PHY

The Ethernet PHY is compliant to IEEE 802.3u 100BASE-TX and IEEE802.3 10BASE-T. It provides the whole physical layer functions for both 10M and 100M

Ethernet speed.

❖ USB Device Endpoint Operation

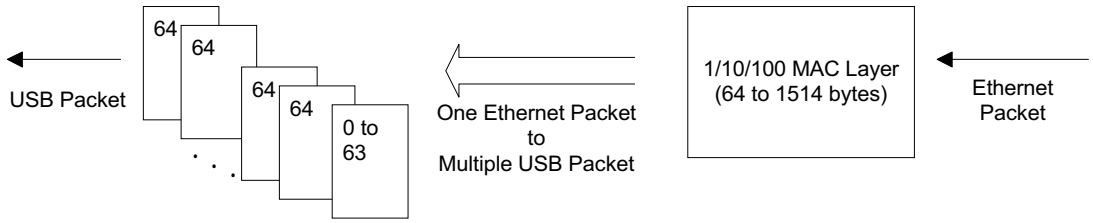
● Endpoint 0

Endpoint 0 is in charge of response to standard USB commands and vendor specific commands. Internal registers setting are also via this endpoint. The response to each command is described in section 6.

● Endpoint 1 bulk IN

Endpoint 1 is in charge of sending the received Ethernet packet to USB host. An Ethernet packet will be split to multiple 64 bytes USB packets on USB. The end of the Ethernet packet is indicated by less then 64-byte or 0 length data transfer in this pipe. The Ethernet received status is optionally reported at the end of the packet.

While accessing to this endpoint, if RXFIFO is either full or any packet is inside, the data in RXFIFO is returned in USB data stage. If ACK is received from USB host, data in RXFIFO is flushed. If no response or NAK is received from USB host, the content in RXFIFO will be re-transmitted. If RXFIFO isn't ready for transmission, NAK is returned to USB host.



The received status is reported as follows

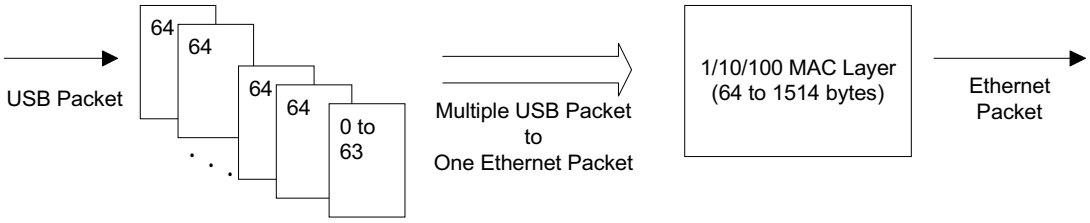
Offset	Bit	Field	Description
Offset0	7-0	rx_bytecnt_lo	The received byte count[7:0].
Offset1	3-0	rx_bytecnt_hi	The received byte count[11:8].
	7-4	reserved	
Offset2	0	multicast_frame	Indicate receive a multicast frame.
	1	long_pkt	Indicate received packet length > 1518 bytes.
	2	runt_pkt	Indicate received packet length < 64 bytes.
	3	crc_err	Indicate CRC check error.
	4	dribble_bit	Indicate packet length is not integer multiple of 8-bit.
	7-5	reserved	
Offset3	7-0	reserved	

● Endpoint 2 bulk OUT

Endpoint 2 is in charge of sending the USB packet to Ethernet. An Ethernet packet is concatenated by multiple 64 bytes USB packets on USB. The first two bytes in every first concatenated USB packet indicate the length of the Ethernet packet. The end of the Ethernet packet is indicated by less then 64-byte or 0 length data transfer in this pipe. The Ethernet transmit status is reported in transmit status register.

When access to this endpoint, data in USB data stage is transfer to TXFIFO, if TXFIFO is free and ACK is returned. If TXFIFO isn't free, NAK is returned.

field	1st byte in 1st USB packet	2nd byte in 1st USB packet	The following packets
content	len[7:0]: Low byte Ethernet packet length	{reserved[4:0], len[10:8]}	Ethernet packet



● Endpoint 3 interrupt IN

Endpoint 3 is in charge of returning the current Ethernet transfer status every polling interval. When access to this endpoint, 8 bytes data is returned to USB host. The 8-byte packet contains

Offset0	Offset1	Offset2	Offset3	Offset4
tx_status(Reg2Bh)	tx_status(Reg2Ch)	rx_status(Reg2Dh)	rx_lostpkt(Reg2Eh)	rx_lostpkt(Reg2Fh)

Offset5	Offset6(1B)	Offset7(1B)
wakeup_status(Reg7Ah)	Packet number in RX FIFO (Reg82h)	7'b00, length error

❖ USB Commands

● Get_Register (Vendor Specific) Single/Burst read

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex Low(1B)	wIndex High(1B)	wLength L(1B)	wLength H(1B)
C0	F0	0	RegIndex[7:0]	00	Length Low	Length High

■ Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)
{RegIndex}	{RegIndex+1)	{RegIndex+2)

The returned total number of registers depends on the length field.

● Set_Register(Vendor Specific) Burst write

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex Low(1B)	wIndex High(1B)	WLength L(1B)	wLength H(1B)
40	F1	0	RegIndex[7:0]	00	Length Low	Length High

■ Data Stage

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)
{RegIndex}	{RegIndex+1}	{RegIndex+2}	{RegIndex+3}

Ex. Write 44 to RegIndex=05h, the transfer will be

■ Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
40	F1	44	00	05	00	01	00

If wLength > 1, more than 1 register is accessed (burst write) and mask is not supported

=> DataStage for 8-byte OUT transfer appears

Ex. Burst write 20 registers from RegIndex=07h and data from 01_d to 20_d

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
40	F1	0000	07	00	14	00

■ Data Stage

➢ 1st OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
01	02	03	04	05	06	07	08

➢ 2nd OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)	Offset3(1B)	Offset4(1B)	Offset5(1B)	Offset6(1B)	Offset7(1B)
09	0A	0B	0C	0D	0E	0F	10

➢ 3rd OUT transfer

Offset0(1B)	Offset1(1B)	Offset2(1B)
11	12	13

● Get_Status(Device)

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	0	0	0	2	0

■ Data Stage

D[15:2]	D[1]: Remote Wakeup	D[0]:Self Powered
0	register of remote_wakeup	1

● Get_Status(Interface)

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
81	0	0	0	2	0

■ Data Stage

D[15:0]
0

● Get_Status(EP0)

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
82	0	0	80 or 00	00	2	0

■ Data Stage

D[15:1]	D[0]: Halt
0	register of ep0_halt

● Get_Status(EP1) bulk IN

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
82	0	0	81	00	2	0

■ Data Stage

D[15:1]	D[0]: Halt
0	register of ep1_halt

● Get_Status(EP2) bulk OUT

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	WLength H(1B)
82	0	0	02	00	2	0

■ Data Stage

D[15:1]	D[0]: Halt
0	register of ep2_halt

● Get_Status(EP3) interrupt IN

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex H(1B)	wLength L(1B)	wLength H(1B)
82	0	0	83	00	2	0

■ Data Stage

D[15:1]	D[0]: Halt
0	register of ep3_halt

● Get_Descriptor(Device) total 18-byte

■ Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	6	01	00	0	Length low	Length high

■ Data Stage: wLength field specifies the total byte count to return

Offset0	Offset1(type)	Offset 2(USB release no. L)	Offset 3(USB release no. H)	Offset4(Class code)	Offset5(Sub Class Code)	Offset6(Protocol)	Offset7(EP0 MaxPktSize)
12(1B)	01(1B)	10(1B)	01(1B)	ff(1B)	00(1B)	ff(1B)	8(1B)

Offset8(vendor ID) Low	Offset8(vendor ID) High	Offset10(productID) Low	Offset11(productID) High	Offset12(releaseID Low)	Offset13(releaseID High)	Offset14 (manufacture)	Offset15 (Product)
(1B)	(1B)	(1B)	(1B)	01(1B)	01(1B)	01(1B)	02(1B)

Offset16(serial no.)	Offset17(no. of config)
03(1B)	01(1B)

● Get_Descriptor(Configuration) total 39-byte

■ Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength L(1B)	wLength H(1B)
80	6	02	00	0	Length low	Length high

■ Data Stage

➢ Configuration Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2(Total Length)Low	Offset3(Total Length)High	Offset4 (NumInterface)	Offset5 (ConfgValue)	Offset6 (StringIndex)	Offset7 (Attribute)
09(1B)	02(1B)	27(1B)	00(1B)	01(1B)	00(1B)	00(1B)	E0(1B)

Offset8 (MaxPower)
max_pwr(1B)

➢ Interface 0 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (InterfaceNum)	Offset3 (AltInterface)	Offset4 (NumEP)	Offset5 (IntfClass)	Offset6 (IntfSubClass)	Offset7 (IntfProtocol)	Offset8 (StringIndex)
09(1B)	04(1B)	00(1B)	00(1B)	03(1B)	FF(1B)	E0(1B)	FF(1B)	00(1B)

➢ EP1 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4(MaxPktSize)Low	Offset5(MaxPktSize)High	Offset6 (Interval)
07(1B)	05(1B)	81(1B)	02(1B) bulk	64(1B)	00(1B)	00(1B)

- EP2 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4(MaxPktSize)Low	Offset4(MaxPktSize)High	Offset6 (Interval)
07(1B)	05(1B)	02(1B)	02(1B) bulk	64(1B)	00(1B)	00(1B)

- EP3 Descriptor

Offset 0 (Length)	Offset1 (DscrType)	Offset2 (EPAddr)	Offset3 (Attribute)	Offset4(MaxPktSize)Low	Offset5(MaxPktSize)High	Offset6 (Interval)
07(1B)	05(1B)	83(1B)	03(1B) interrupt	08(1B)	00(1B)	ep3_interval(1B)

● Get_Descriptor(String) Index0, LanguageID Code

■ Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength Low(1B)	wLength High(1B)
80	06	00	03	0000	Length Low	Length High

■ Data Stage

Offset0 (Length)	Offset1 (DscrType)	Offset2 (LanguageID) L	Offset3 (LanguageID) H
04(1B)	03(1B)	09(1B)	04(1B)

● Get_Descriptor(String) Index1, manufacture

■ Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex L(1B)	wIndex H(1B)	wLength Low(1B)	wLength High(1B)
80	06	01	03	09	04	Length Low	Length High

■ Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1B)	03(1B)	String

● Get_ Descriptor(String) Index2, product

■ Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex L(1B)	wIndex H(1B)	wLength Low(1B)	wLength High(1B)
80	06	02	03	09	04	Length Low	Length High

■ Data Stage

Offset0 (Length)	Offset1 (DscrType)	
length(1B)	03(1B)	String

● Get_ Descriptor(String) Index3, serial no.

■ Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex L(1B)	wIndex H(1B)	wLength Low(1B)	wLength High(1B)
80	06	03	03	09	04	Length Low	Length High

■ Data Stage

Offset0 (Length)	Offset1 (DscrType)	
Length(1B)	03(1B)	String

● Get_Configuration

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength Low(1B)	wLength High(1B)
80	08	0	0	1	0

■ Data Stage

Offset0 (ConfgValue)(1B)

● Get_Interface

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex(2B)	wLength Low(1B)	wLength High(1B)
81	10	0	0	1	0

■ Data Stage

Offset0 (AltIntf)(1B)
00

● Clear_Feature(Device) Remote Wakeup

■ Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength(2B)
00	01	01	00	0	0

● Set_feature(Device) Remote Wakeup

■ Setup Stage

bmReq	bReq	wValue L(1B)	wValue H(1B)	wIndex(2B)	wLength(2B)
00	03	01	00	0	0

● Clear_Feature(EP0,1,2,3) Halt

■ Setup Stage

bmReq	bReq	wValue(2B)	wIndex L(1B)	wIndex L(2B)	wLength(2B)
02	03	0000	EP no	00	0

● Set_Feature(EP0,1,2,3) Halt

■ Setup Stage

BmReq	bReq	wValue(2B)	wIndex H(1B)	wIndex H(2B)	wLength(2B)
02	03	0000	EP no	00	0

❖ Electrical Specifications

● Absolute Maximum Ratings

Supply Voltage (VDD)	4.6 V
DC Input Voltage (VIN)	6V
DC Output Voltage (VOUT)	4.6V
Power Comsumption	126mA @ Idle state
	7mA @ Suspend Mode
	142mA @ 10M Full Duplex Mode
	152 mA @ 100M Full Duplex Mode
Storage Temperature	-65 C to 150 C
Operation Temperature	-40 C to 125 C
ESD Rating	2000V

● Operating Condition

Symbol	Parameter	Condition	Min	Max	Units
VDD	Supply Voltage		3.0	3.6	V
I_{dd}	Supply Current			150	mA

● DC Specifications

USB Interface DC specification

Symbol	Parameter	Condition	Min	Max	Units
V_{ih}	Input High Voltage		2.0		V
V_{il}	Input Low Voltage			0.8	V
V_{DI}	Differential Input Sensitivity		0.2		V
V_{cm}	Differential Common Mode Range		0.8	2.5	V
V_{ol}	Output Low Voltage		0.0	0.3	V
V_{oh}	Output High Voltage		2.8	3.6	V
V_{crs}	Output Signal Crossover Voltage		1.3	2.0	V

❖ EEPROM Interface DC Specification

Recommanded Operating Conditions:

Symbol	Parameter	Condition	Min	Max	Units
V_{ih}	Input High Voltage		1.8	5.5	V
V_{il}	Input Low Voltage		-0.5	1.0	V
I_i	Input Leakage Current	V_{in} 3.3V or 0V	±1nA	±1μA	
V_{oh}	Output High Voltage		2.4		V
V_{ol}	Output Low Voltage			0.4	V
C_{in}	Input Pin Capacitance			5.66	pF

GPIO Interface DC Specification

Symbol	Parameter	Condition	Min	Max	Units
V_{ih}	Input High Voltage		1.8	5.5	V
V_{il}	Input Low Voltage		-0.5	1.0	V
I_i	Input Leakage Current	V_{in} 3.3V or 0V	±1nA	±1μA	
V_{oh}	Output High Voltage		2.4		V
V_{ol}	Output Low Voltage			0.4	V
C_{in}	Input Pin Capacitance			5.64	pF

❖ Timings

• Reset Timing

ADM8513 can be reset either by hardware, software or USB reset.

1. A hardware reset is accomplished by asserting the RST# pin after power up the device. It should have a duration of at least 100 ms to ensure the external 48MHz crystal is in stable and correct frequency. All registers will be reset to default values.
2. A software reset is accomplished by setting the reset bit (bit 4) of the Ethernet Control Register (address 01h). This software reset will reset all registers to default values.
3. When ADM8513 sees an SE0 on USB bus for more than 2.5μs. This USB reset will reset all registers to default values.

• USB Interface Timing

Symbol	Parameter	Condition	Min	Max	Units
T_{FR}	Rise time	C_L = 50$_P$	4	20	ns
T_{FF}	Fall time	C_L = 50$_P$	4	20	ns
T_{FRFF}	Rise and fall time matching	T_{FRFF} =T_{FR} /T_{FF}	90	111.11	%

• EEPROM Interface Timing

Symbol	Parameter	Min	Max	Units
t_{EESK}	**EESK** Clock Frequency	0	1	MHz
T_{EECSS}	**EECS** Setup Time to **EESK**	0.2		μs
T_{EECSH}	**EECS** Hold Time from **EESK**	0		ns
T_{EEDOH}	**EEDO** Hold Time from **EESK**	70		ns
T_{EEDOP}	**EEDO** Output Delay to “1” or “0”		2	μs
t_{EEDIS}	**EEDI** Setup Time to **EESK**	0.4		μs
t_{EEDIH}	**EEDI** Hold Time from **EESK**	0.4		μs

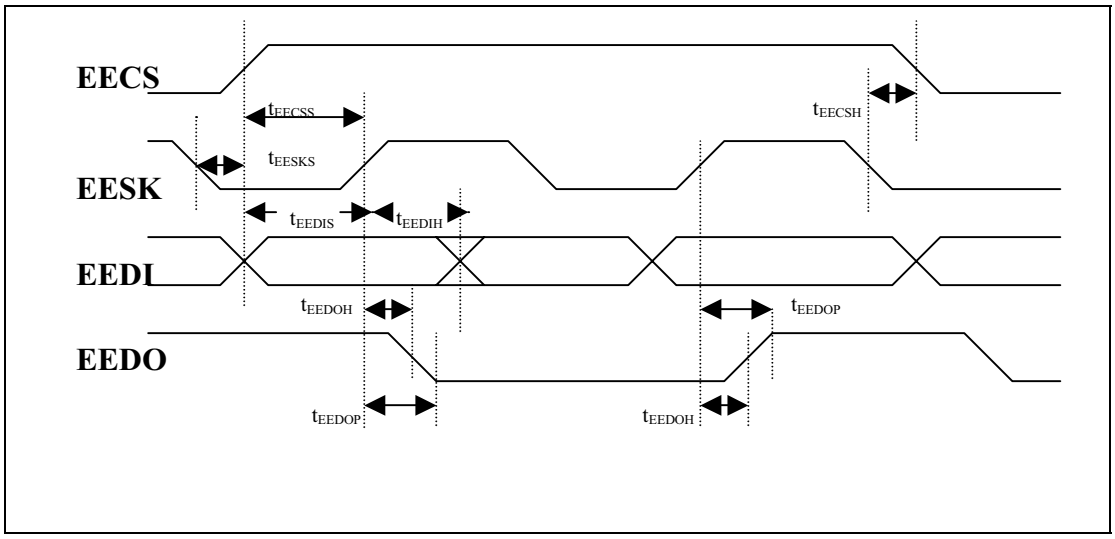


Fig. 1 EEPROM Interface Timings

❖ EEPROM Interface & Example

If the EEPROM contents from offset 0 to offset5 is "FF_FF_FF_FF_FF_FF", the EEPROM isn't programmed correctly. The default values for every field are used instead of loading from EEPROM.

Offset (byte)	Field	Description
00	node_id0	The 1st byte of Ethernet node ID.
01	node_id1	The 2nd byte of Ethernet node ID.
02	node_id2	The 3rd byte of Ethernet node ID.
03	node_id3	The 4th byte of Ethernet node ID.
04	node_id4	The 5th byte of Ethernet node ID.
05	node_id5	The 6th byte of Ethernet node ID.
06-07	reserved	
08	max_pwr	The maximum USB power consumption.
09	ep3_interval	The polling interval for endpoint 3. If this value is 0, EP3 is disabled.
0A[0]	reserved	
0A[1]	usb_sel	0A[1] = 1: select internal USB transceiver.
0A[4:2]	Phy MODE	0A[4:2]= 000
0B[0]	reserved	
0B[5:1]	reserved	
0B[7:6]	LED mode	Refer to Pin assignment
0C	Languageid_lo	The low byte of language ID.
0D	Languageid_hi	The high byte of language ID.
0E-0F	reserved	
10	manuid_lo	The low byte of manufacture ID.
11	manuid_hi	The high byte of manufacture ID.
12	proid_lo	The low byte of product ID.
13	proid_hi	The high byte of product ID.
14	manu_str_len	The length for manufacture string.
15	manu_str_offset	The word offset address of manufacture string.
16	pro_str_len	The length for product string.
17	pro_str_offset	The word offset address of product string.
18	seri_str_len	The length for serial number string.
19	seri_str_offset	The word offset address of serial number string.

Example

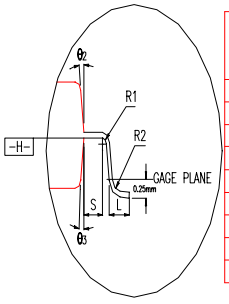
offset(byte)	value
0000h:	00, 00 E8 00 02 2C 00 00,
0008h:	50 01 02 00 09 04 00 00
0010h:	A6 07 13 85 0E 10 2A 20
0018h:	0A 38 00 00 00 00 00 00
0020h:	0E 03 41 00 44 00 4D 00
0028h:	74 00 65 00 6B 00 00 00
0030h:	1E 00 55 00 53 00 42 00
0038h:	20 00 31 00 30 00 2F 00
0040h:	2A 03 55 00 53 00 42 00
0048h:	-20 00 54 00 6F 00 20 00
0050h:	4C 00 41 00 4E 00 20 00
0058h:	43 00 6F 00 6E 00 76 00
0060h:	65 00 72 00 74 00 65 00
0068h:	72 00 00 00 00 00 00 00
0070h:	0A 03 30 00 30 00 30 00
0078h:	31 00 00 00 00 00 00 00

Offset(byte)	Value	Description
00-05	00_00_E8_10_46_02	NIC node ID
08	50	maximum power 160mA
09	01	interrupt endpoint 3 polling interval 1ms
0A	02	isochronous endpoint disable,select internal USB transceiver Use internal Ethernet PHY, Wake on Lan enable
0C-0D	0904	Language ID 0409
10-11	A607	manufacture ID 07A6
12-13	8511	product ID 8513
14	0E	manufacture string length 0E bytes
15	10	manufacture string starts from word offset 10h, thus byte offset 20h.
16	1E	product string length 1E bytes
17	18	product string starts from word offset 18h, thus byte offset 30h.
18	0A	serial number string length 0A bytes
19	38	serial number string starts from word offset 38h, thus byte offset 70h.
20-2E	0E 03 41 00 44 00 4D 00 74 00 65 00 6B 00	0E:descriptor size 14 bytes 03: string descriptor 41.....: UNICODE encoded string
30-4E	1E 03 55 00 53 00 42 00 20 00.....	1E:descriptor size 30 bytes 03: string descriptor 55.....: UNICODE encoded string
50-5A	0A 03 30 00 30 00 30 00 31 00	0A: descriptor size 10 bytes 03: string descriptor 30.....: UNICODE encoded string

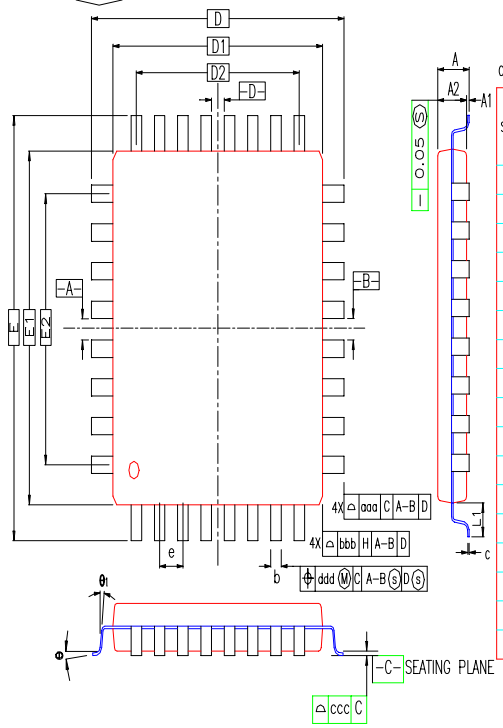
❖ Package

Note : This diagram has a 32pin. But, the relative parameters presents 48pin package data. So, please ignore the pin number and regard the diagram as 48pin.

Make an example : Parameter “E” (9mm) means the distance between the two opposite sides. Parameter “ e “ (0.8mm) means the distance between two adjacent pins. D&E1 means body size.



SYMBOL	32L						44L						48L					
	MILLIMETER			INCH			MILLIMETER			INCH			MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
b	0.30	0.35	0.45	0.012	0.014	0.018	0.17	0.20	0.27	0.007	0.008	0.011	0.17	0.20	0.27	0.007	0.008	0.011
e	0.80 BSC.			0.031 BSC.			0.50 BSC.			0.020 BSC.			0.50 BSC.			0.020 BSC.		
D2	5.60			0.220			5.00			0.197			5.50			0.217		
E2	5.60			0.220			5.00			0.197			5.50			0.217		
TOLERANCES OF FORM AND POSITION																		
aaa	0.20			0.008			0.20			0.008			0.20			0.008		
bbb	0.20			0.008			0.20			0.008			0.20			0.008		
ccc	0.10			0.003			0.08			0.003			0.08			0.003		
ddd	0.20			0.008			0.08			0.003			0.08			0.003		



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
D	9.00 BSC.			0.354 BSC.		
D1	7.00 BSC.			0.276 BSC.		
E	9.00 BSC.			0.354 BSC.		
E1	7.00 BSC.			0.276 BSC.		
R2	0.08	—	0.20	0.003	—	0.008
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
c	0.09	—	0.20	0.004	—	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
S	0.20	—	—	0.008	—	—

Appendix A Layout Guide

Rev. 1.0b

1.Placement :

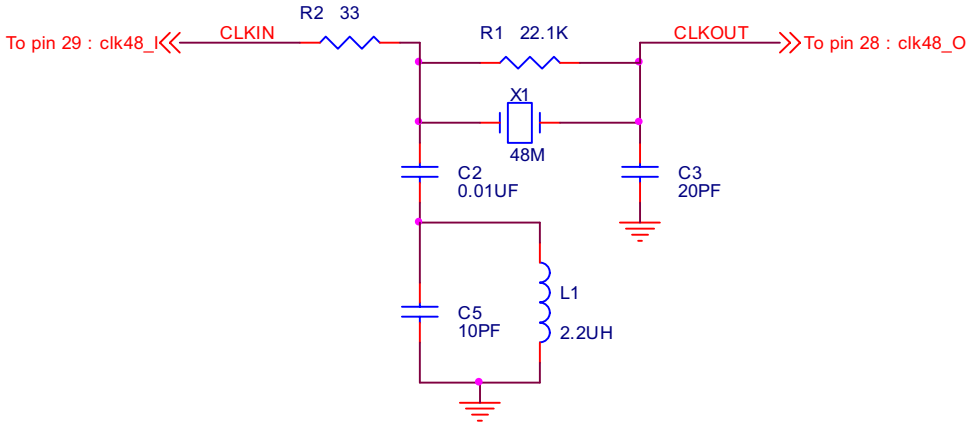
(1) At USB side, place ADM8513 and USB connector as close as possible.

(2) At Ethernet side, place ADM8513 , transformer and RJ45 as close as possible .

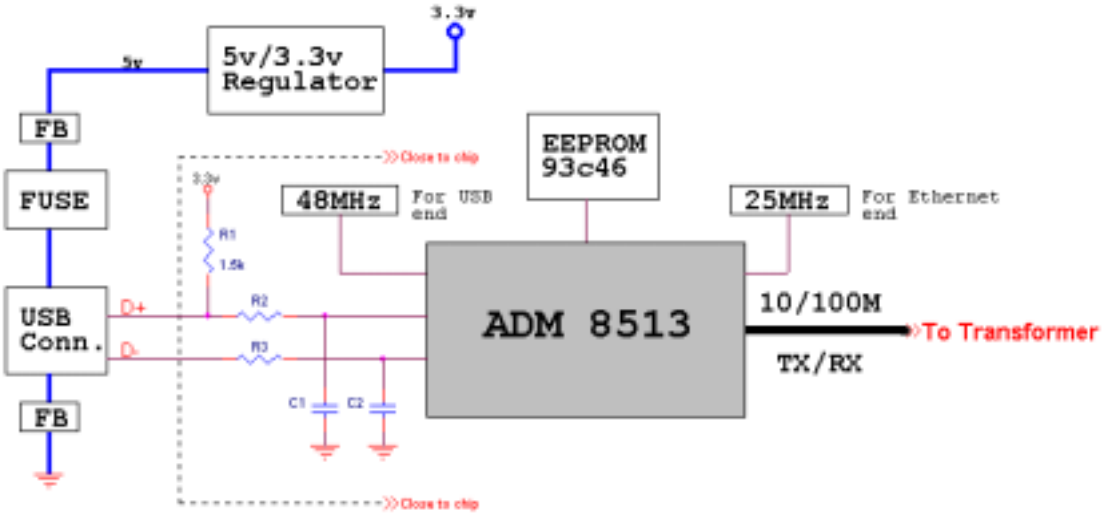
(3) The crystal or OSC device should be close to ADM8513 and away from the following items

- ●Any analog signal
- ●PCB edge
- ●Any other high frequency components and their associated traces.

If you can't avoid those designs, please add a Resistor between Crystal (or OSC) and ADM8513 chip clk48_I pin as figure show:



(4)Place the filtering capacitor as close as possible at the Vcc pin of ADM8513 and its trace must be short and wide.



2.Trace routing

(1)Keep USB differential pair data signal D+ and D-:

- ●Trace width should be as wide as possible.
- ●Make D+ and D- traces route at the same signal plane and doesn't pass through other plane.
- ●Inhibit crossover on D+ and D-
- ●The termination resistance (R2,R3) and decoupling capacitors (C1,C2) should be close to ADM8513.
- ●D+ and D- Signal trace length should be equal and as short as possible.

(2)Arrangement Tx and Rx trace

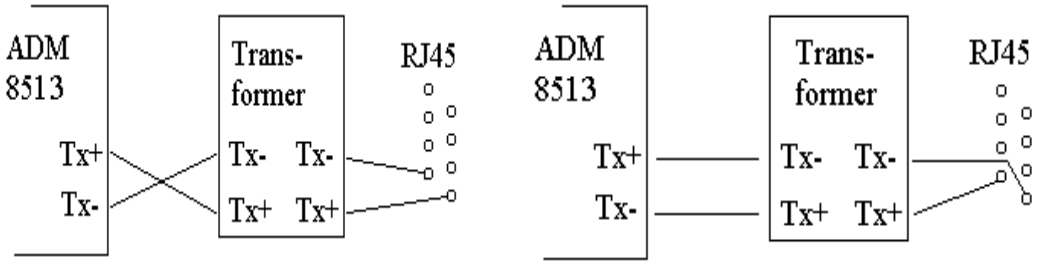
- ● Tx+/- and Rx+/- trace avoid right angle and round angle >90 degree, suggested.

Bad Good

- ●Trace width must be wide and should be wider than 8 mils.
- ●Signal trace length between Tx+/- differential pairs should be cross and have equal length .The total length should be no longer than 2 cm. The same requirement applies to Rx+/- also.
- ●Make Tx and Rx trace route at the same signal plane and doesn't

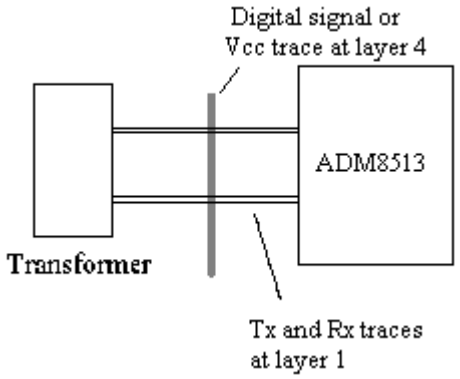
pass through other plane.

- ●Every differential pairs as cross as possible, but no less than 8 mils and space should be almost equal .
- ●Keep space large between Tx and Rx differential pairs,even separated ground planes underneath Tx and Rx signal pairs.
- ●Away from clock and power traces.
- ● If Tx routed trace must cross, the trace can be swapped between chip and transformer,and transformer to RJ45 ,too.



Origin Suggest

(3) Digital signal should be away from analog signal and Vcc traces .If you can't avoid this situation, analog siganl or Vcc trace should cross over 90 degree at other plane.



(4)Vcc trace should be short and prefer route in the format of the plane a special for GND.

3.Power and Ground

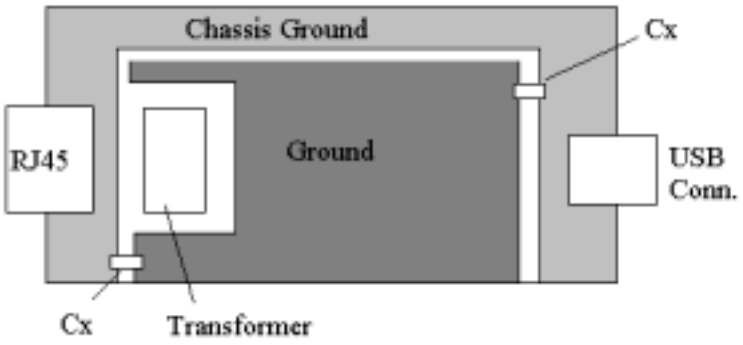
(1)All of the Vcc pin should be have a 0.1uF SMD capacitors which placed with it. To be effective, the capacitors should be place as close as possible at the pin.

(2)The chassis ground plane connected to the USB B type and

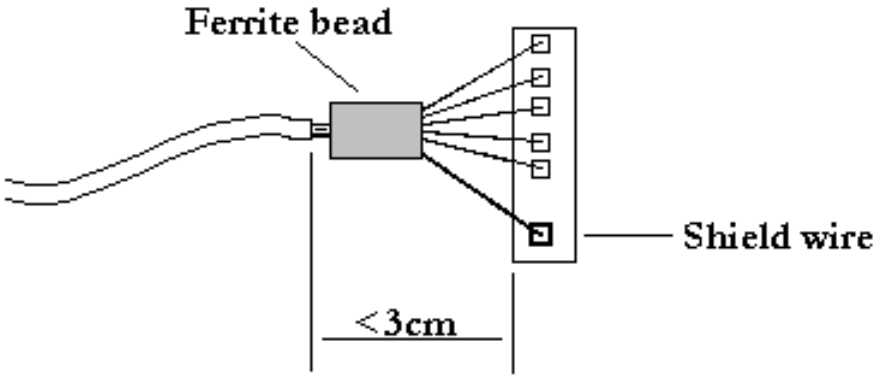
network connector chassis should be isolated from the signal plane with 0.1uF capacitors or bead to prevent any radiation from leaking and resulting in EMI failure.

(3)Right angle is recommend when partition Vcc as well as GND planes.

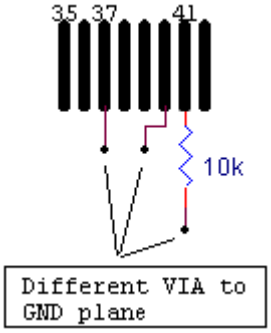
(4)Avoid Vcc and ground planes placing directly under the transformer.See the Figure as below.



(5)If you use a captive cable (plus the shield wire).it may require additional filtering for EMI test pass.and the length of unshielded cable should be limited to 3cm or less.



(6) Please connect 10K Ohm Ribb resistance gnd , pin40(GndRef) and pin37(GndR) first then use signal via to Gnd (Specially for 2 layers board design).



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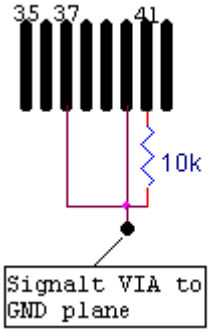

Good