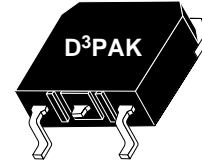
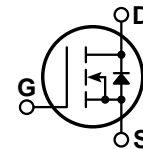


POWER MOS V®

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- **Faster Switching**
- **100% Avalanche Tested**
- **Lower Leakage**
- **Surface Mount D³PAK Package**



MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT10M19SVR	UNIT
V_{DSS}	Drain-Source Voltage	100	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$ ⑤	75	Amps
I_{DM}	Pulsed Drain Current ① ⑤	300	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	370	Watts
	Linear Derating Factor	2.96	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ① ⑤ (Repetitive and Non-Repetitive)	75	Amps
E_{AR}	Repetitive Avalanche Energy ①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ④	1500	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	100			Volts
$I_{D(on)}$	On State Drain Current ② ⑤ ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	75			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ② ($V_{GS} = 10V, 0.5 I_{D[Cont.]}$)			0.019	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1.0\text{mA}$)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

USA
405 S.W. Columbia Street

EUROPE
Avenue J.F. Kennedy Bât B4 Parc Cadéra Nord

APT Website - <http://www.advancedpower.com>

Bend, Oregon 97702-1035

F-33700 Merignac - France

Phone: (541) 382-8028

Phone: (33) 5 57 92 15 15

FAX: (541) 388-0364

FAX: (33) 5 56 47 97 61

DYNAMIC CHARACTERISTICS

APT10M19SVR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		5100	6120	pF
C_{oss}	Output Capacitance			1900	2660	
C_{rss}	Reverse Transfer Capacitance			800	1200	
Q_g	Total Gate Charge ^③	$V_{GS} = 10V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = 0.5 I_{D[Cont.]}$ @ 25°C		200	300	nC
Q_{gs}	Gate-Source Charge			40	60	
Q_{gd}	Gate-Drain ("Miller") Charge			92	180	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]}$ @ 25°C $R_G = 1.6\Omega$		16	32	ns
t_r	Rise Time			40	40	
$t_{d(off)}$	Turn-off Delay Time			50	75	
t_f	Fall Time			20	40	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

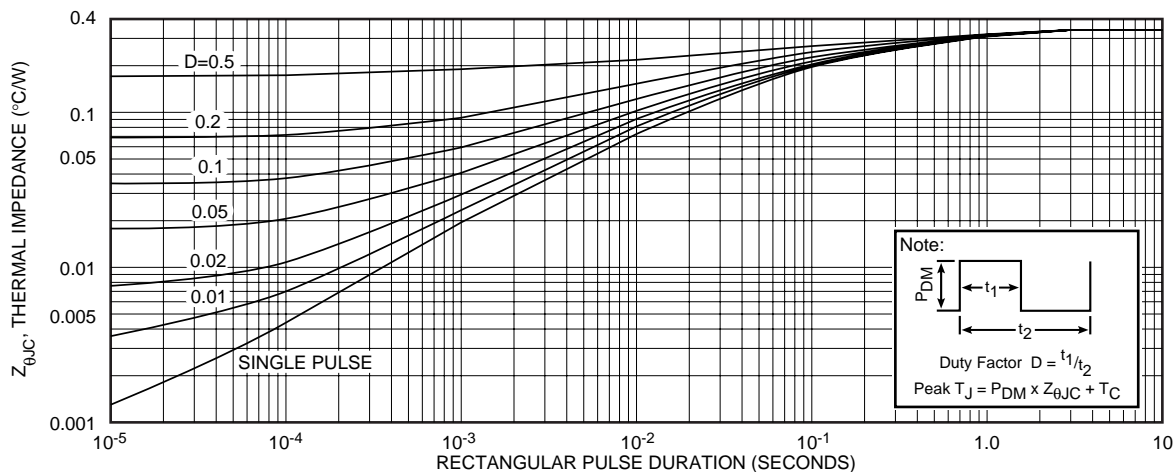
Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current ^⑤ (Body Diode)			75	Amps
I_{SM}	Pulsed Source Current ^{① ⑤} (Body Diode)			300	
V_{SD}	Diode Forward Voltage ^② ($V_{GS} = 0V, I_S = -I_{D[Cont.]}$)			1.3	Volts
t_{rr}	Reverse Recovery Time ($I_S = -I_{D[Cont.]}$, $di_S/dt = 100A/\mu s$)		200		ns
Q_{rr}	Reverse Recovery Charge ($I_S = -I_{D[Cont.]}$, $di_S/dt = 100A/\mu s$)		1.4		μC

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.34	$^{\circ}C/W$
$R_{\theta JA}$	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum T_j
- ② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%
- ③ See MIL-STD-750 Method 3471
- ④ Starting $T_j = +25^{\circ}C$, $L = 0.53mH$, $R_G = 25\Omega$, Peak $I_L = 75A$
- ⑤ The maximum current is limited by lead temperature.

APT Reserves the right to change, without notice, the specifications and information contained herein.



APT10M19SVR

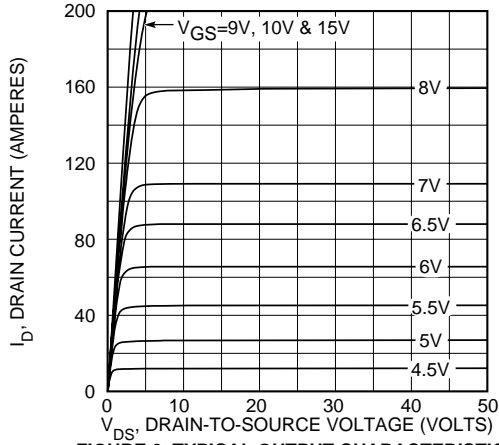


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

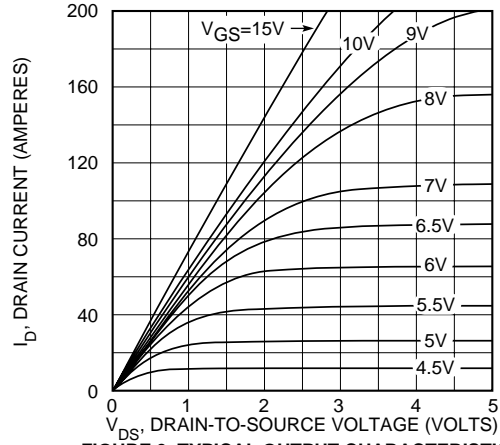


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

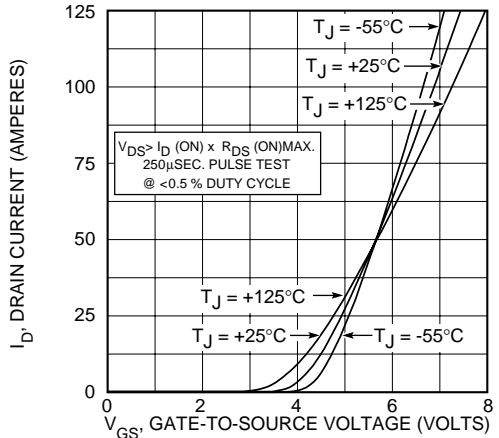


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

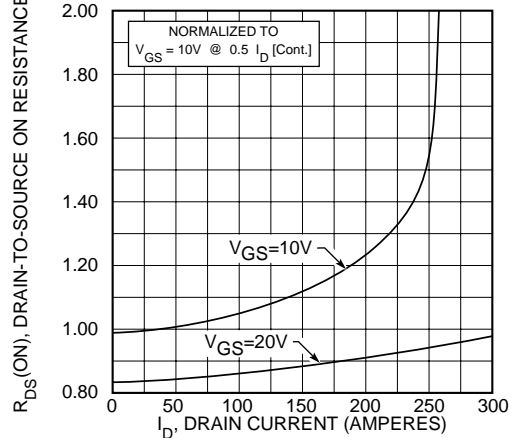


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

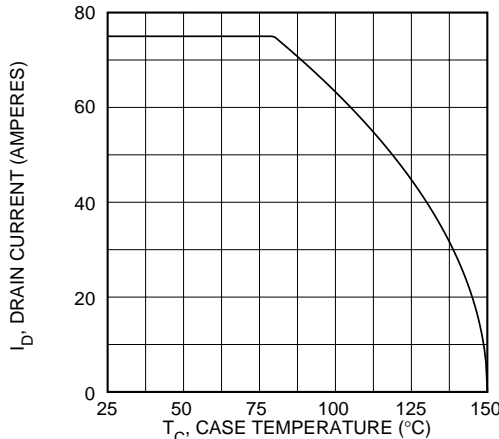


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

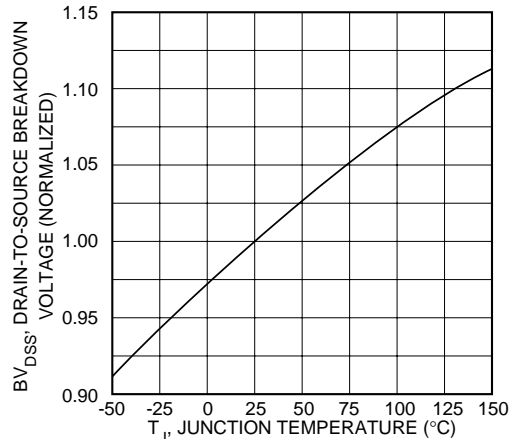


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

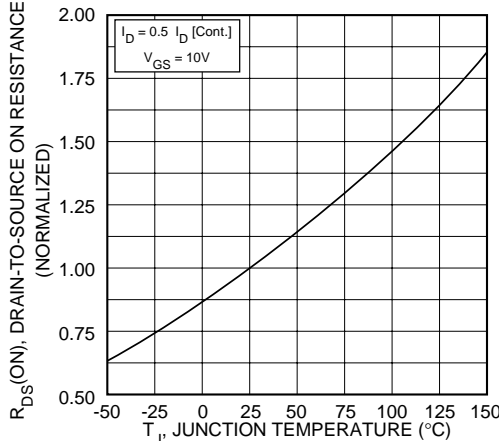


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

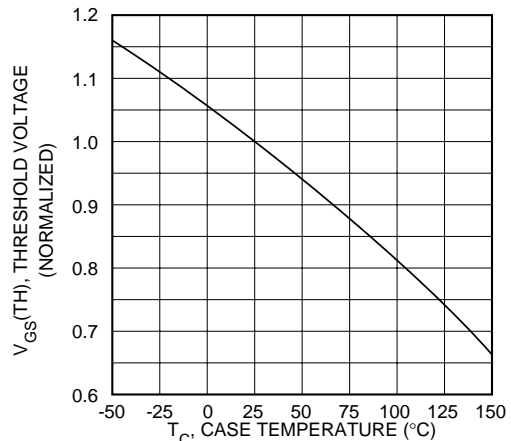


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

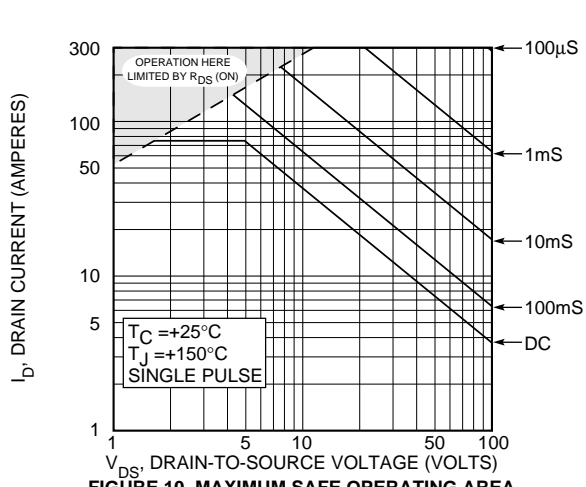


FIGURE 10, MAXIMUM SAFE OPERATING AREA

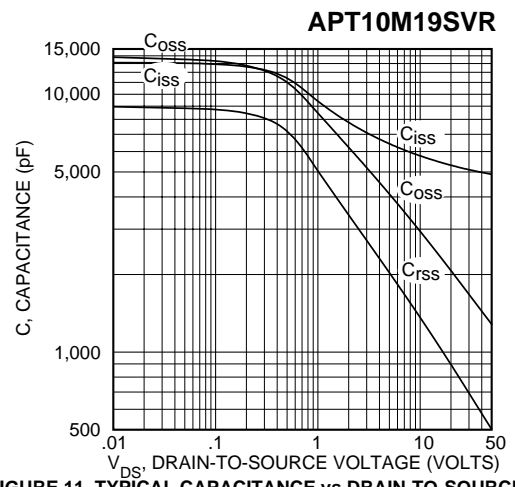


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

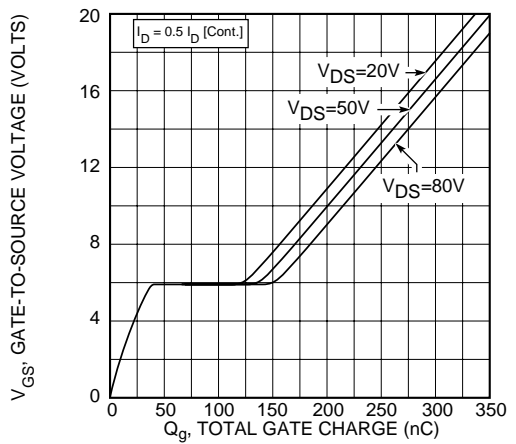


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

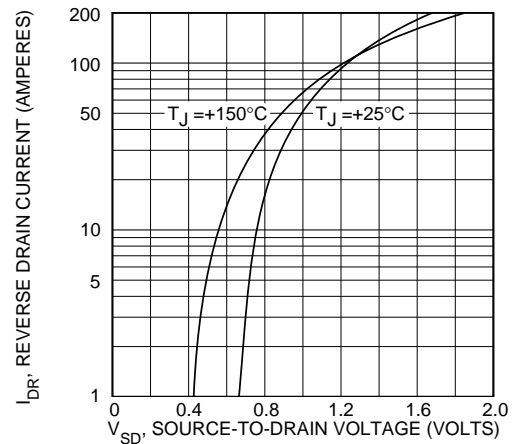


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

D³PAK Package Outline

