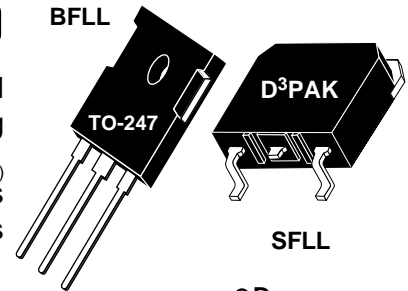
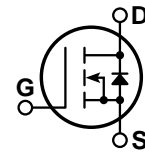


POWER MOS 7™
FREDFET
BFLL

SFLL


Power MOS 7™ is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7™ by significantly lowering $R_{DS(ON)}$ and Q_g . Power MOS 7™ combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with APT's patented metal gate structure.

- Lower Input Capacitance
- Lower Miller Capacitance
- Lower Gate Charge, Q_g
- Increased Power Dissipation
- Easier To Drive
- TO-247 or Surface Mount D³PAK Package
- **FAST RECOVERY BODY DIODE**

MAXIMUM RATINGS

 All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT5024	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	22	Amps
I_{DM}	Pulsed Drain Current ^①	88	
V_{GS}	Gate-Source Voltage Continuous	±30	Volts
V_{GSM}	Gate-Source Voltage Transient	±40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	265	Watts
	Linear Derating Factor	2.12	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	22	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	960	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	500			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	22			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D[Cont.]}$)			0.240	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1\text{mA}$)	3		5	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

APT Website - <http://www.advancedpower.com>

DYNAMIC CHARACTERISTICS

APT5024 BFL - SFL

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C _{iss}	Input Capacitance	V _{GS} = 0V		1910		pF
C _{oss}	Output Capacitance	V _{DS} = 25V		390		
C _{rss}	Reverse Transfer Capacitance	f = 1 MHz		30		
Q _g	Total Gate Charge ^③	V _{GS} = 10V		48		nC
Q _{gs}	Gate-Source Charge	V _{DD} = 0.5 V _{DSS}		13		
Q _{gd}	Gate-Drain ("Miller") Charge	I _D = I _D [Cont.] @ 25°C		22		
t _{d(on)}	Turn-on Delay Time	V _{GS} = 15V		12		ns
t _r	Rise Time	V _{DD} = 0.5 V _{DSS}		10		
t _{d(off)}	Turn-off Delay Time	I _D = I _D [Cont.] @ 25°C		30		
t _f	Fall Time	R _G = 1.6Ω		7		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I _S	Continuous Source Current (Body Diode)			22	Amps
I _{SM}	Pulsed Source Current ^① (Body Diode)			88	
V _{SD}	Diode Forward Voltage ^② (V _{GS} = 0V, I _S = -I _D [Cont.])			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ^⑤			15	V/ns
t _{rr}	Reverse Recovery Time (I _S = -I _D [Cont.], di/dt = 100A/μs)	T _j = 25°C		250	ns
		T _j = 125°C		400	
Q _{rr}	Reverse Recovery Charge (I _S = -I _D [Cont.], di/dt = 100A/μs)	T _j = 25°C		1.9	μC
		T _j = 125°C		6	
I _{RRM}	Peak Recovery Current (I _S = -I _D [Cont.], di/dt = 100A/μs)	T _j = 25°C		15	Amps
		T _j = 125°C		26	

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
R _{θJC}	Junction to Case			0.47	°C/W
R _{θJA}	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 μs, Duty Cycle < 2%

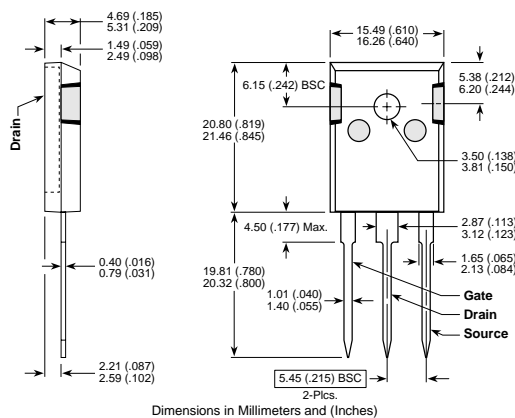
③ See MIL-STD-750 Method 3471

④ Starting T_j = +25°C, L = 3.97mH, R_G = 25Ω, Peak I_L = 22A

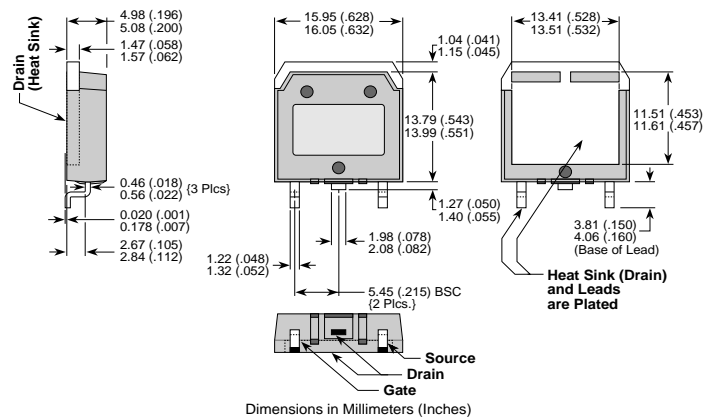
⑤ dv/dt numbers reflect the limitations of the test circuit rather than the device itself. I_S ≤ -I_D[Cont.] di/dt ≤ 700A/μs V_R ≤ V_{DSS} T_J ≤ 150°C

APT Reserves the right to change, without notice, the specifications and information contained herein.

TO-247 Package Outline



D³PAK Package Outline



050-7131 Rev - 10-2001

APT's devices are covered by one or more of the following U.S. patents: 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336
5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058