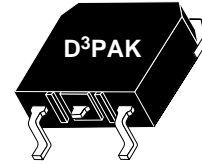
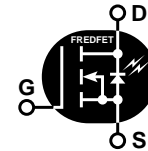


POWER MOS V®
FREDFET


Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.

- Fast Recovery Body Diode
- Lower Leakage
- Faster Switching
- 100% Avalanche Tested
- Surface Mount D³PAK Package


MAXIMUM RATINGS

 All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT5020SVFR	UNIT
V_{DSS}	Drain-Source Voltage	500	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	26	Amps
I_{DM}	Pulsed Drain Current ^①	104	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	300	Watts
	Linear Derating Factor	2.4	W/°C
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	°C
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	26	Amps
E_{AR}	Repetitive Avalanche Energy ^①	30	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	1300	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	500			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	26			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D[Cont.]}$)			0.20	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			250	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			1000	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1.0\text{mA}$)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

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DYNAMIC CHARACTERISTICS

APT5020SVFR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$		3700	4440	pF
C_{oss}	Output Capacitance	$V_{DS} = 25V$		510	715	
C_{rss}	Reverse Transfer Capacitance	$f = 1\text{ MHz}$		200	300	
Q_g	Total Gate Charge ^③	$V_{GS} = 10V$		150	225	nC
Q_{gs}	Gate-Source Charge	$V_{DD} = 0.5 V_{DSS}$		25	37	
Q_{gd}	Gate-Drain ("Miller") Charge	$I_D = I_D [\text{Cont.}] @ 25^\circ\text{C}$		70	105	
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$		12	25	ns
t_r	Rise Time	$V_{DD} = 0.5 V_{DSS}$		10	20	
$t_{d(off)}$	Turn-off Delay Time	$I_D = I_D [\text{Cont.}] @ 25^\circ\text{C}$		50	75	
t_f	Fall Time	$R_G = 1.8\Omega$		8	15	

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			26	Amps
I_{SM}	Pulsed Source Current ^① (Body Diode)			104	
V_{SD}	Diode Forward Voltage ^② ($V_{GS} = 0V, I_S = -I_D [\text{Cont.}]$)			1.3	Volts
dv/dt	Peak Diode Recovery dv/dt ^⑤			5	V/ns
t_{rr}	Reverse Recovery Time ($I_S = -I_D [\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		250	ns
		$T_j = 125^\circ\text{C}$		500	
Q_{rr}	Reverse Recovery Charge ($I_S = -I_D [\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		1.3	μC
		$T_j = 125^\circ\text{C}$		4.5	
I_{RRM}	Peak Recovery Current ($I_S = -I_D [\text{Cont.}], di/dt = 100A/\mu s$)	$T_j = 25^\circ\text{C}$		12	Amps
		$T_j = 125^\circ\text{C}$		18	

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.42	$^\circ\text{C/W}$
$R_{\theta JA}$	Junction to Ambient			40	

① Repetitive Rating: Pulse width limited by maximum junction temperature.

② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%

③ See MIL-STD-750 Method 3471

④ Starting $T_j = +25^\circ\text{C}$, $L = 3.85\text{mH}$, $R_G = 25\Omega$, Peak $I_L = 26\text{A}$

⑤ $I_S \leq -I_D [\text{Cont.}], di/dt = 100\text{A}/\mu\text{s}$, $V_{DD} \leq V_{DSS}$, $T_j \leq 150^\circ\text{C}$, $R_G = 2.0\Omega$, $V_R = 200\text{V}$.

APT Reserves the right to change, without notice, the specifications and information contained herein.

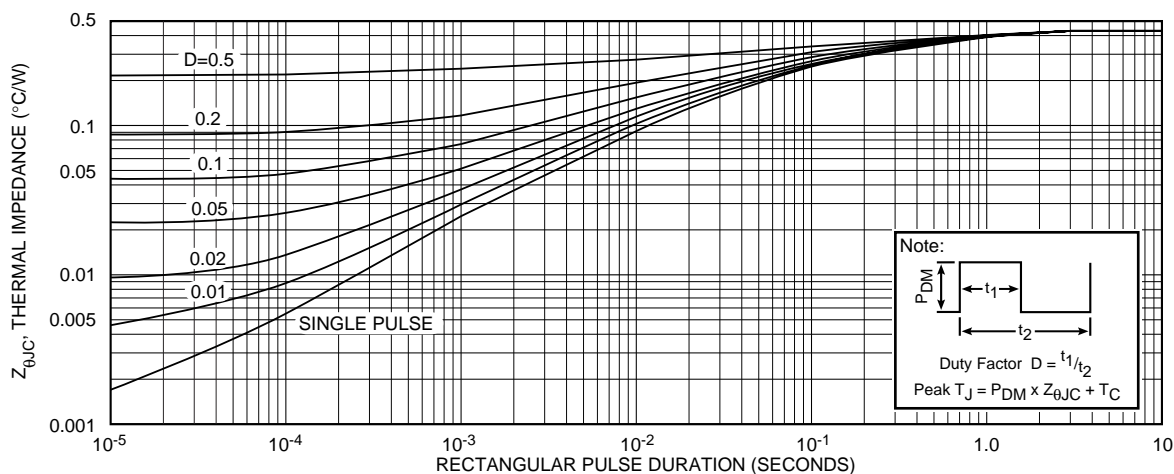


FIGURE 1, MAXIMUM EFFECTIVE TRANSIENT THERMAL IMPEDANCE, JUNCTION-TO-CASE vs PULSE DURATION

APT5020SVFR

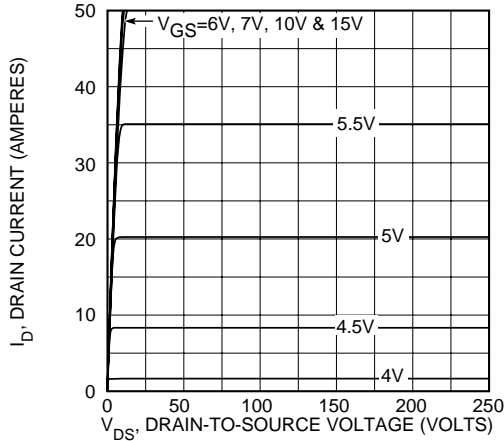


FIGURE 2, TYPICAL OUTPUT CHARACTERISTICS

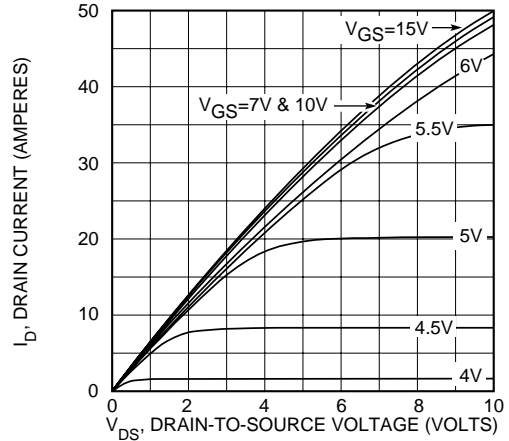


FIGURE 3, TYPICAL OUTPUT CHARACTERISTICS

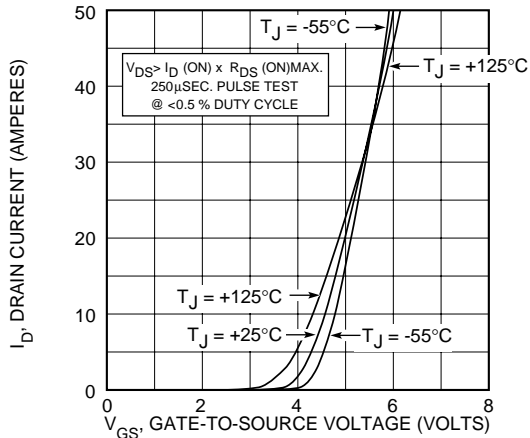


FIGURE 4, TYPICAL TRANSFER CHARACTERISTICS

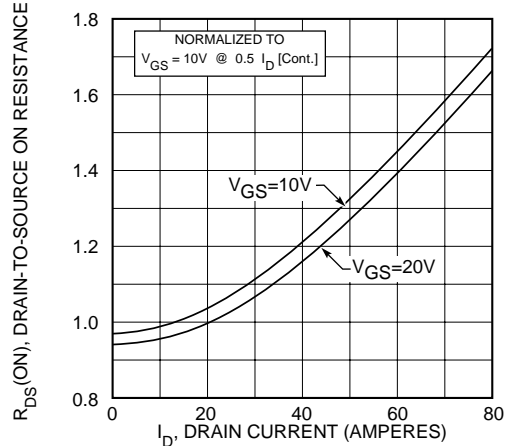


FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT

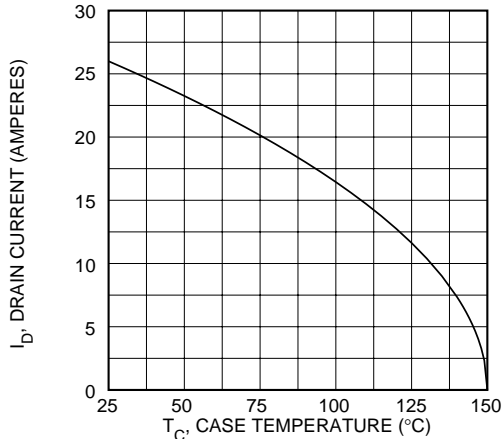


FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE

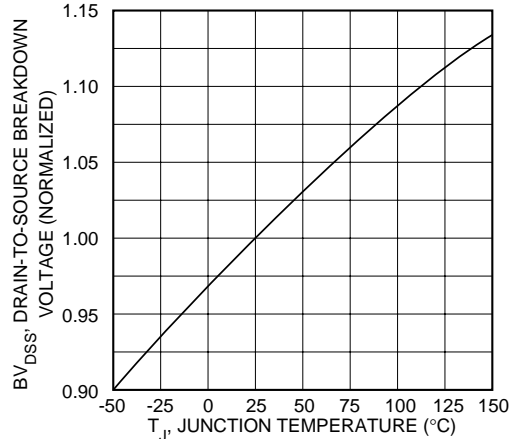


FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE

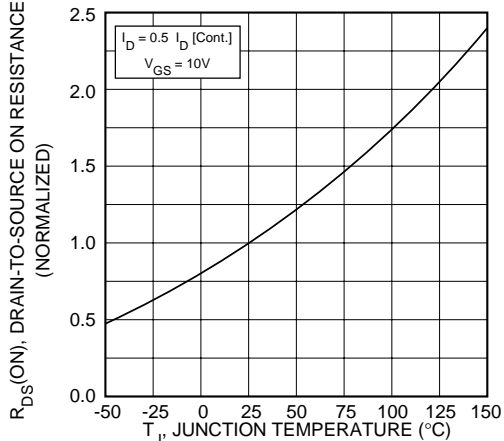


FIGURE 8, ON-RESISTANCE vs. TEMPERATURE

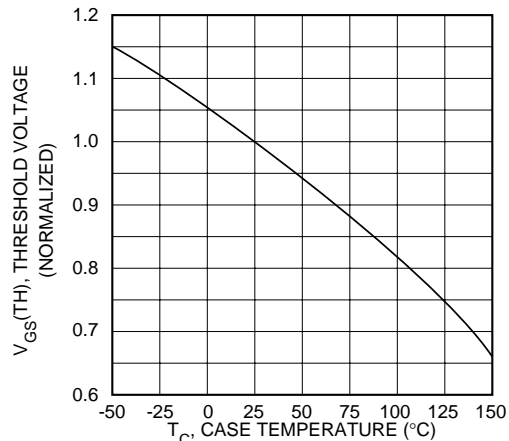


FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE

APT5020SVFR

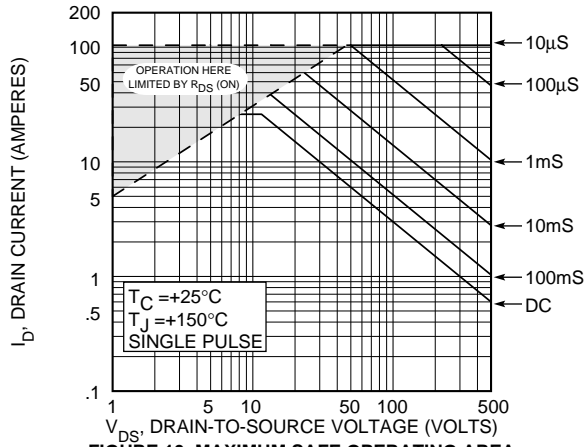


FIGURE 10, MAXIMUM SAFE OPERATING AREA

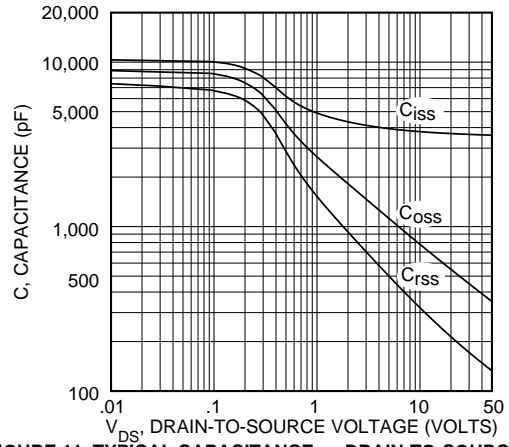


FIGURE 11, TYPICAL CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

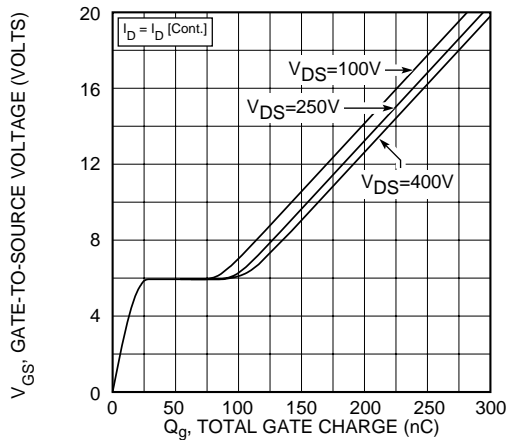


FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

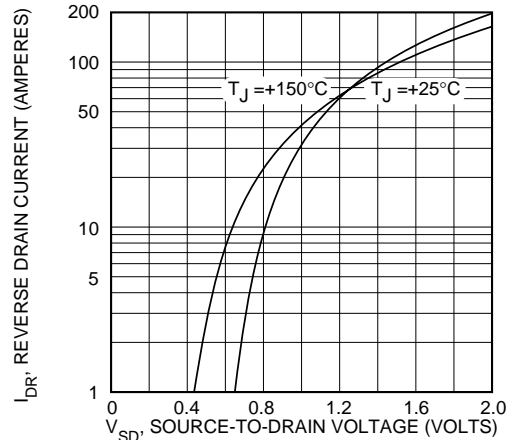


FIGURE 13, TYPICAL SOURCE-DRAIN DIODE FORWARD VOLTAGE

D³PAK Package Outline

