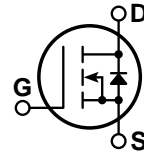
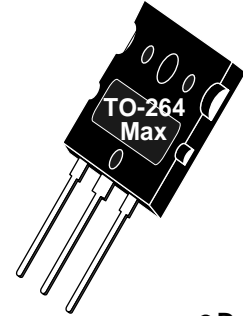


POWER MOS V®

Power MOS V® is a new generation of high voltage N-Channel enhancement mode power MOSFETs. This new technology minimizes the JFET effect, increases packing density and reduces the on-resistance. Power MOS V® also achieves faster switching speeds through optimized gate layout.



- TO-264 MAX Package
- 100% Avalanche Tested
- Faster Switching
- Lower Leakage

MAXIMUM RATINGS

All Ratings: $T_C = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	APT8018L2VR	UNIT
V_{DSS}	Drain-Source Voltage	800	Volts
I_D	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	43	Amps
I_{DM}	Pulsed Drain Current ^①	172	
V_{GS}	Gate-Source Voltage Continuous	± 30	Volts
V_{GSM}	Gate-Source Voltage Transient	± 40	
P_D	Total Power Dissipation @ $T_C = 25^\circ\text{C}$	830	Watts
	Linear Derating Factor	6.64	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to 150	$^\circ\text{C}$
T_L	Lead Temperature: 0.063" from Case for 10 Sec.	300	
I_{AR}	Avalanche Current ^① (Repetitive and Non-Repetitive)	43	Amps
E_{AR}	Repetitive Avalanche Energy ^①	50	mJ
E_{AS}	Single Pulse Avalanche Energy ^④	3200	

STATIC ELECTRICAL CHARACTERISTICS

Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-Source Breakdown Voltage ($V_{GS} = 0V, I_D = 250\mu\text{A}$)	800			Volts
$I_{D(on)}$	On State Drain Current ^② ($V_{DS} > I_{D(on)} \times R_{DS(on)}$ Max, $V_{GS} = 10V$)	43			Amps
$R_{DS(on)}$	Drain-Source On-State Resistance ^② ($V_{GS} = 10V, 0.5 I_{D(Cont.)}$)			0.180	Ohms
I_{DSS}	Zero Gate Voltage Drain Current ($V_{DS} = V_{DSS}, V_{GS} = 0V$)			25	μA
	Zero Gate Voltage Drain Current ($V_{DS} = 0.8 V_{DSS}, V_{GS} = 0V, T_C = 125^\circ\text{C}$)			250	
I_{GSS}	Gate-Source Leakage Current ($V_{GS} = \pm 30V, V_{DS} = 0V$)			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 5mA$)	2		4	Volts

 **CAUTION:** These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.

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DYNAMIC CHARACTERISTICS

APT8018L2VR

Symbol	Characteristic	Test Conditions	MIN	TYP	MAX	UNIT
C_{iss}	Input Capacitance	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1\text{ MHz}$		11020		pF
C_{oss}	Output Capacitance			1090		
C_{rss}	Reverse Transfer Capacitance			580		
Q_g	Total Gate Charge ③	$V_{GS} = 10V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = 0.5 I_{D[Cont.]}$ @ 25°C		530		nC
Q_{gs}	Gate-Source Charge			55		
Q_{gd}	Gate-Drain ("Miller") Charge			230		
$t_{d(on)}$	Turn-on Delay Time	$V_{GS} = 15V$ $V_{DD} = 0.5 V_{DSS}$ $I_D = I_{D[Cont.]}$ @ 25°C $R_G = 0.6\Omega$		19		ns
t_r	Rise Time			17		
$t_{d(off)}$	Turn-off Delay Time			80		
t_f	Fall Time			12		

SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS

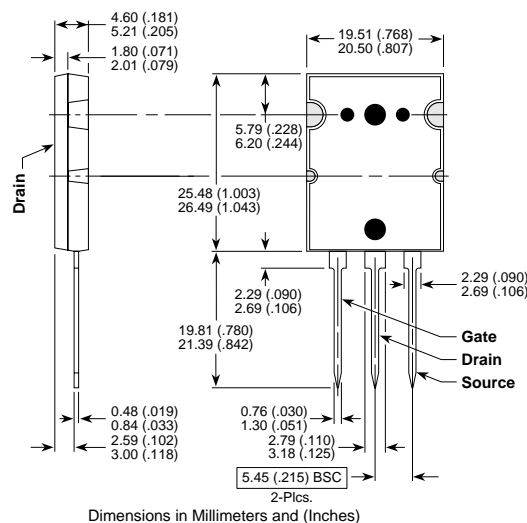
Symbol	Characteristic / Test Conditions	MIN	TYP	MAX	UNIT
I_S	Continuous Source Current (Body Diode)			43	Amps
I_{SM}	Pulsed Source Current ① (Body Diode)			172	
V_{SD}	Diode Forward Voltage ② ($V_{GS} = 0V, I_S = -I_{D[Cont.]}$)			1.3	Volts
t_{rr}	Reverse Recovery Time ($I_S = -I_{D[Cont.]}, di_S/dt = 100A/\mu s$)		930		ns
Q_{rr}	Reverse Recovery Charge ($I_S = -I_{D[Cont.]}, di_S/dt = 100A/\mu s$)		29		μC

THERMAL CHARACTERISTICS

Symbol	Characteristic	MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction to Case			0.15	$^{\circ}C/W$
$R_{\theta JA}$	Junction to Ambient			40	

- ① Repetitive Rating: Pulse width limited by maximum junction temperature.
 - ② Pulse Test: Pulse width < 380 μs , Duty Cycle < 2%
 - ③ See MIL-STD-750 Method 3471
 - ④ Starting $T_j = +25^{\circ}C, L = 3.46mH, R_G = 25\Omega, \text{Peak } I_L = 43A$
- APT Reserves the right to change, without notice, the specifications and information contained herein.**

TO-264 MAX™(L2) Package Outline



050-5992 rev- 2-2001

APT's devices are covered by one or more of the following U.S.patents: 4,895,810 5,045,903 5,089,434 5,182,234 5,019,522 5,262,336
5,256,583 4,748,103 5,283,202 5,231,474 5,434,095 5,528,058