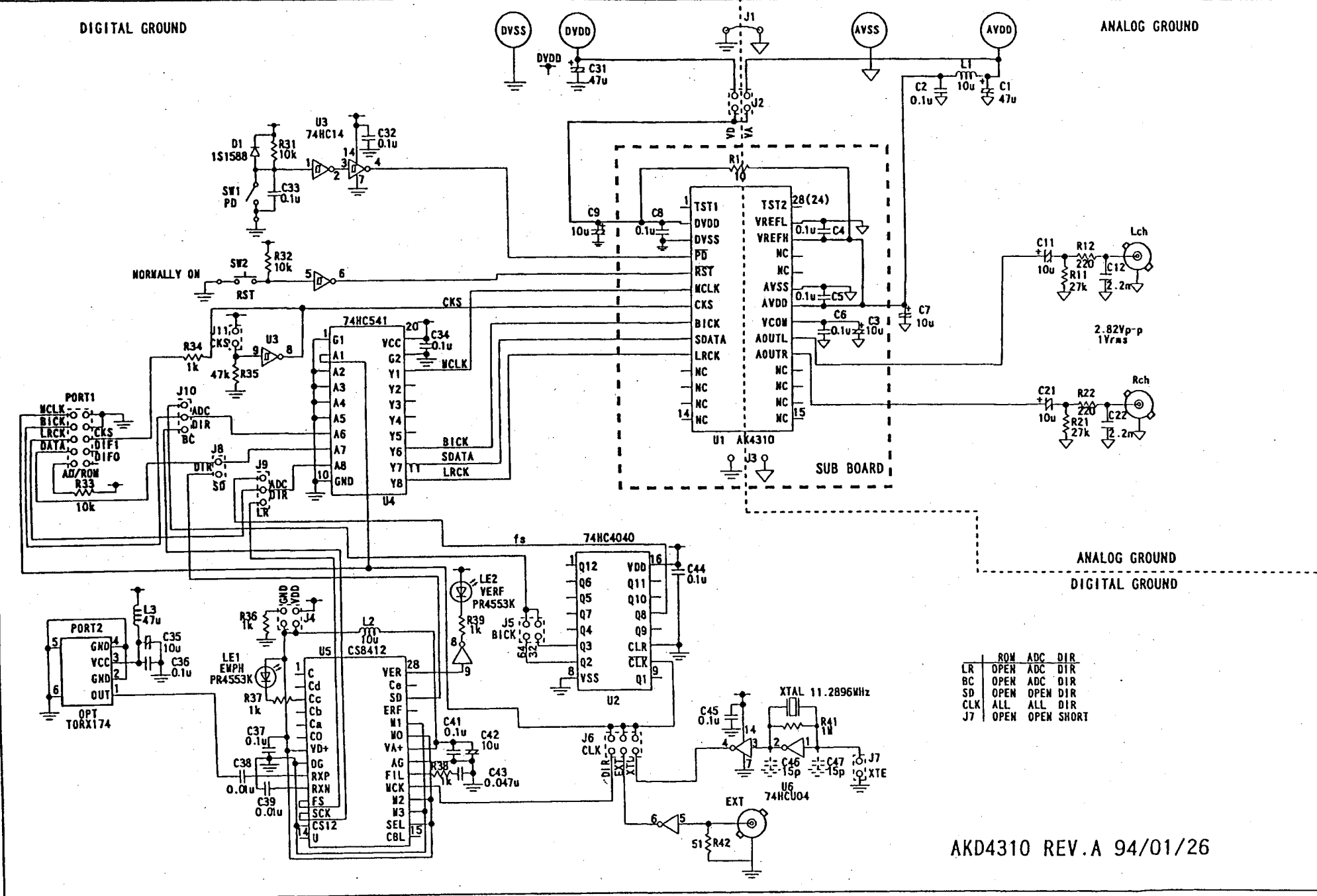




DIGITAL GROUND

ANALOG GROUND



	ROW	ADC	DIR
LR	OPEN	ADC	DIR
BC	OPEN	ADC	DIR
SD	OPEN	OPEN	DIR
CLK	ALL	ALL	DIR
J7	OPEN	OPEN	SHORT

AKD4310 REV.A 94/01/26

■ External Analog Filter

The AK4309B includes the successive of single-ended outputs, so it does not require any external components. The BNC connectors on the board supplies the analog outputs of AK4309B directly. The output level of AK4309B is about 1Vrms(AVDD=5V).

■ Power Supply and its Decoupling

AVDD and DVDD to the AK4309B are decoupled separately in order to minimize the effect of the digital noise. A system analog supply is fed to AVDD and it is also fed to DVDD by way 10 Ω resistor from AVDD. Decoupling capacitors should be connected to AK4309B as near as possible, particularly with the ceramic capacitor to the VREF pin.

■ Operation Sequence

- ① Set up the power supply lines.  
 AVDD=DVDD= +4.5 ~ 5.5 V,  
 AVSS=DVSS= 0 V  
 The evaluation board shorts J1, and it is used a common AVDD and DVDD.
- ② Set up the evaluation modes and jumper pins (See next item).  
 Be careful for the operating voltage when use DIR or ROM board.
- ③ Power on, and push reset switch after that.
- ※ SW2 resets the AK4309B during operation.

■ Set-up of the Evaluation Modes and Jumper Pins

1. Evaluation Mode

Applicable Evaluation Mode

\* Be careful for the operating voltage when use DIR or ROM board.

- ① DIR (Optical link)
- ② Ideal sine wave generated by ROM data
- ③ Using AD converted data
- ④ All interface signals including master clock are fed externally

① DIR(CS8412)

PORT2 is used. DIR generates CLK, BICK and LRCK from the received data through optical connector (TORX174). Used for the evaluation using CD test disk. Nothing should be connected to PORT1.

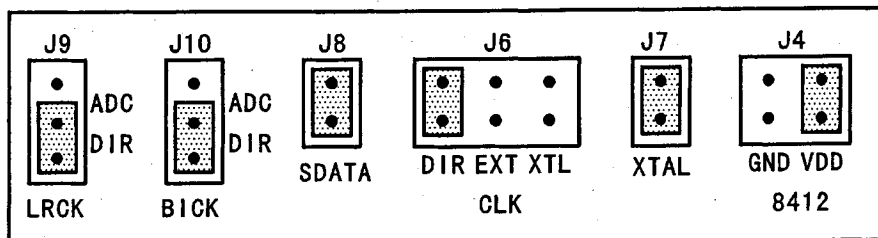


Figure 2. Jumper Set Up(DIR)

② Ideal sine wave generated by ROM data

Digital signals generated by AKD43XX are used. PORT1 is used for the interface with AKD43XX. Master clock is sent from AKD4309B to AKD43XX and LRCK, BICK, SDATA are done from AKD43XX to AKD4309B. In case of using external clock through a BNC connector, selects EXT on J6(CLK) and shorts J7.

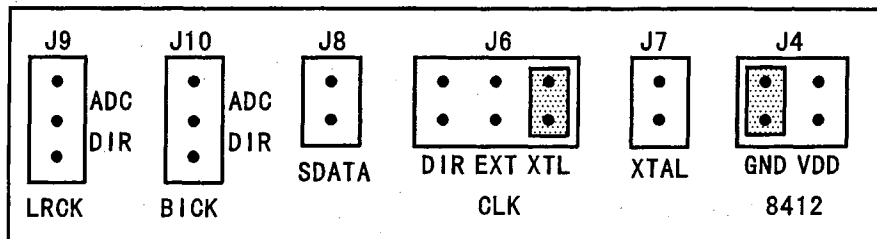


Figure 3. Jumper Set Up(ROM)

③ Using AD converted data

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards (AKD5391, AKD5390, AKD5352/1, AKD5350 and AKD5330) with PORT1. In case of using external clock through a BNC connector, select EXT on J6(CLK) and short J7.

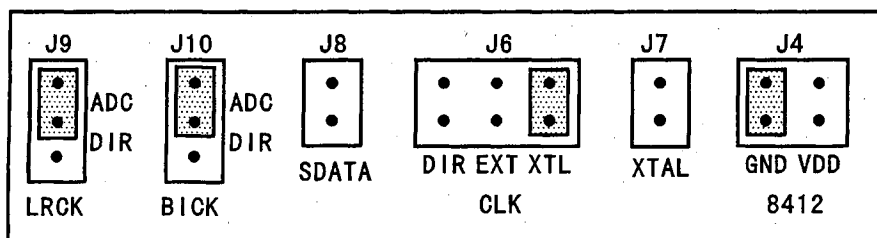


Figure 4. Jumper Set Up(A/D)

④ All interface signals including master clock are fed external

Under the following set-up, all external signals could be fed through PORT1.

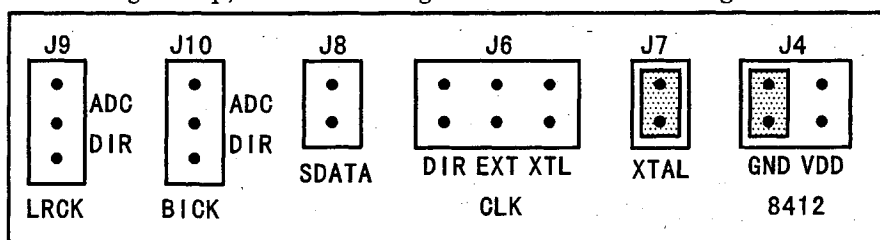
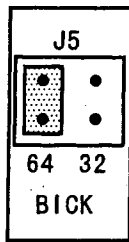


Figure 5. Jumper Set Up

## 2. BIT CLK ( BICK ) Set-up

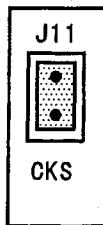
Figure 6



Either 32fs or 64fs could be selected.  
Figure shows 64fs example.

## 3. CKS Set-up

Figure 7



Either 256fs or 384fs could be selected.  
Figure shows 256fs example.

\* ① and ③ of evaluation mode correspond to only 256fs.

### ■ The Function of the Others

- (SW1) It is not needed for evaluation of AK4309B.
- [SW2] It resets the AKD4309B. Put the down position during conversion.
- [LE1] It indicates whether the input data is pre-emphasized or not.  
LED turns on when the data is pre-emphasized.
- [LE2] It monitors VREF pin of the CS8412. LED turns on when some error has occurred to CS8412.

■ AK4309B Measurement example

Table 1. AK4309B(Use 24pin SSOP socket) Measurement results

		Measurement Filter
THD+N	-86.0dB	20kLPF
DR(-60dB)	86.9dB	20kLPF
	90.2dB	20kLPF + A-Weight
S/N	87.6dB	20kLPF
	91.0dB	20kLPF + A-Weight

[Conditions]

Measurement unit : ROHDE&SCHWARZ UPD04  
 Device : 20pinSSOP  
 Interface : DIR  
 MCLK : 256fs  
 Digital input data : 16bit  
 fin : 1kHz  
 Temperature : Room temperature

(FFT plot)

Points : 8192  
 Averaging : 16

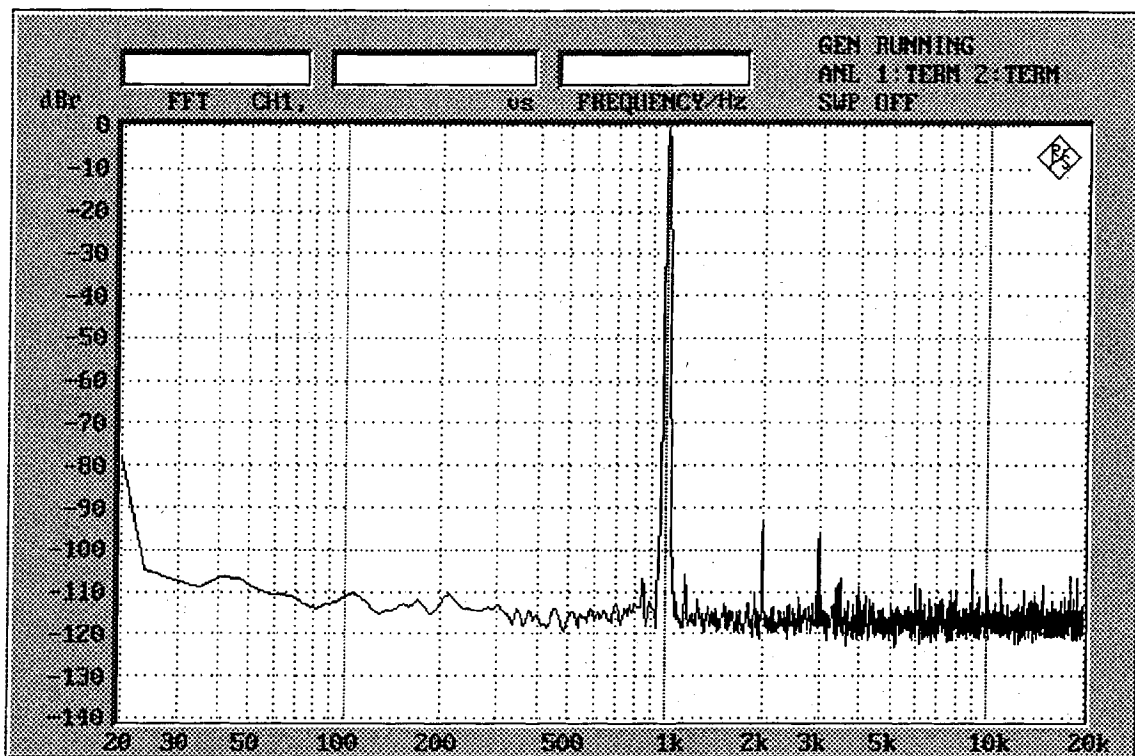


Fig.1 FFT(0dB)

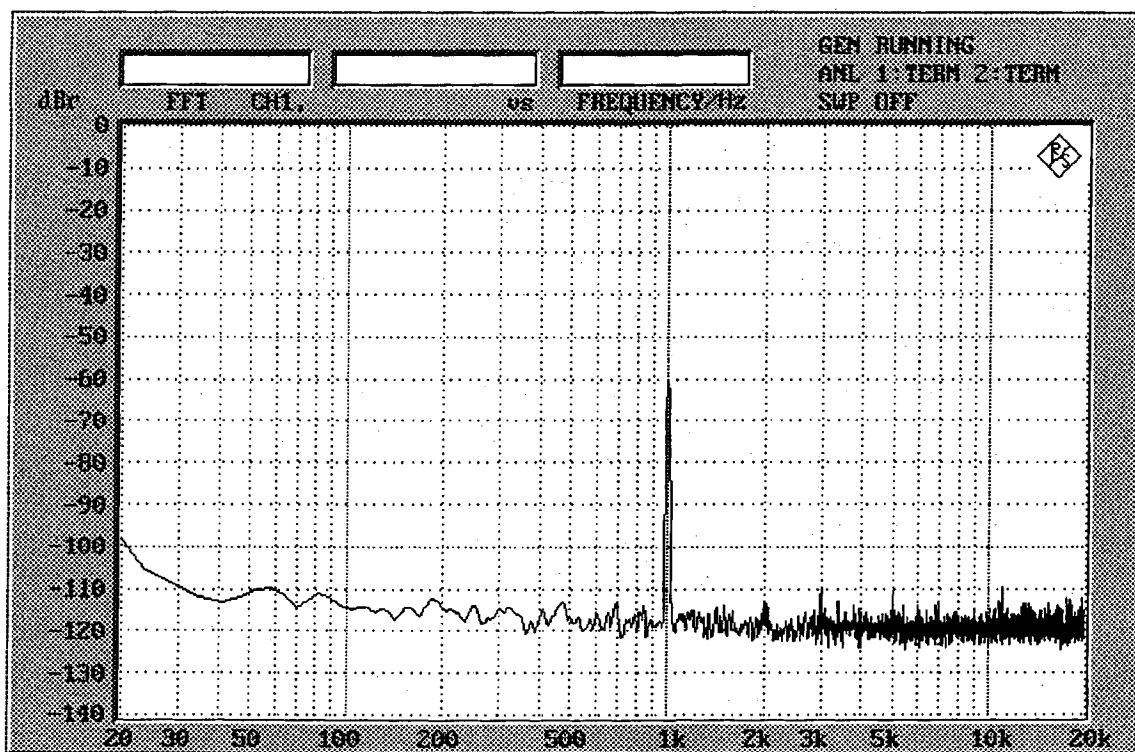


Fig.2 FFT(-60dB)

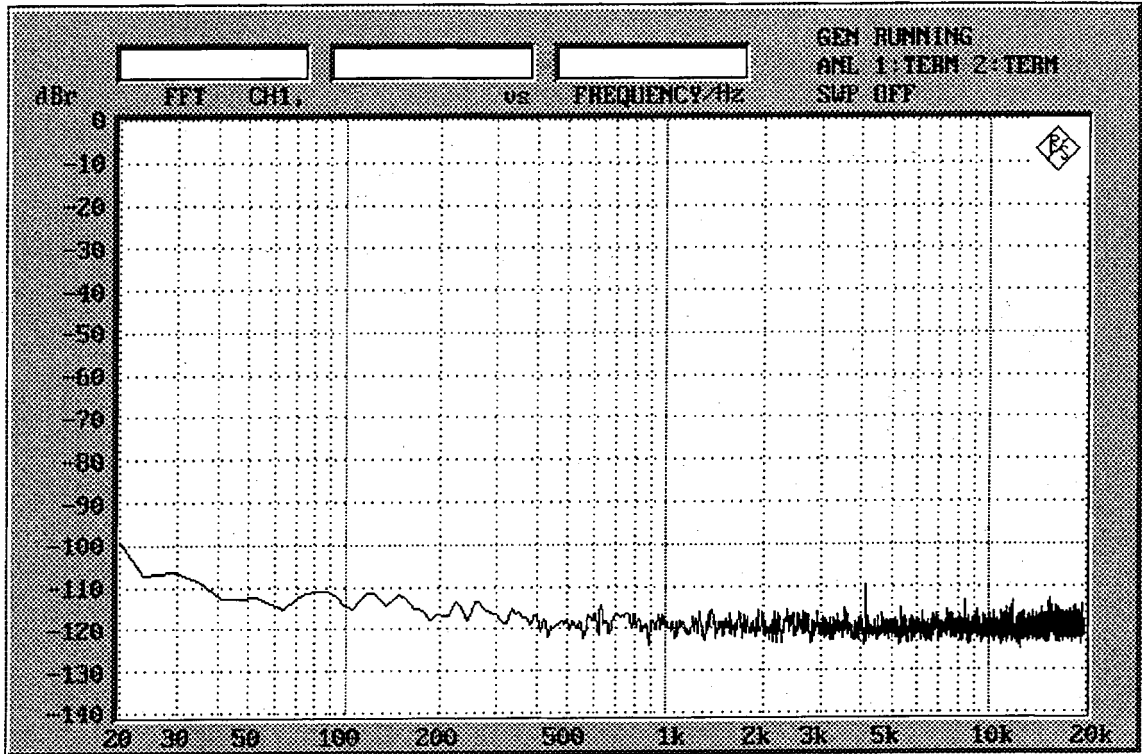


Fig.3 FFT(noise floor)

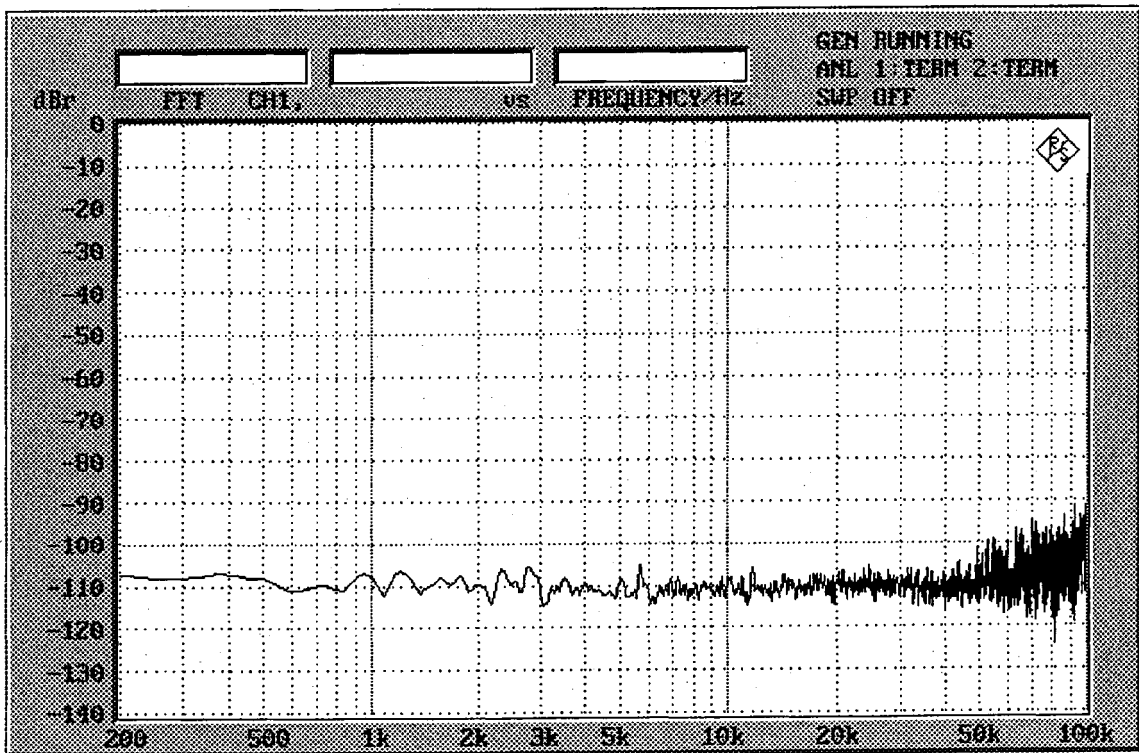


Fig.4 FFT(noise floor : ~100kHz)



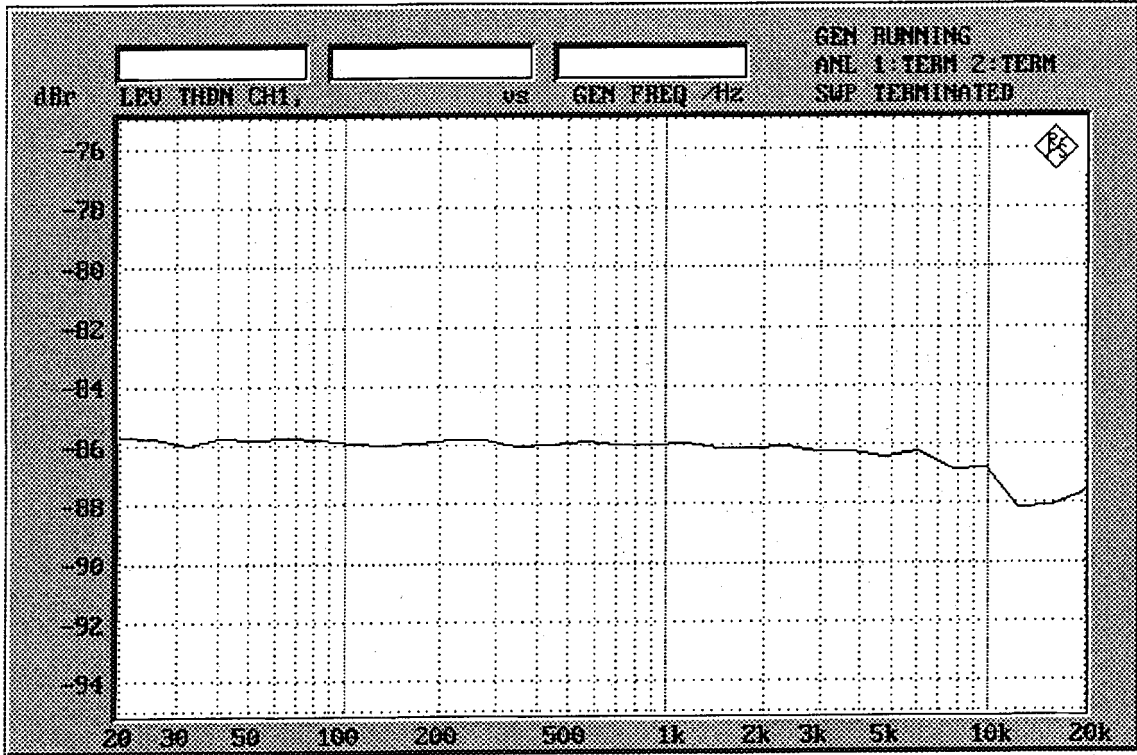


Fig.5 THD+N vs Frequency

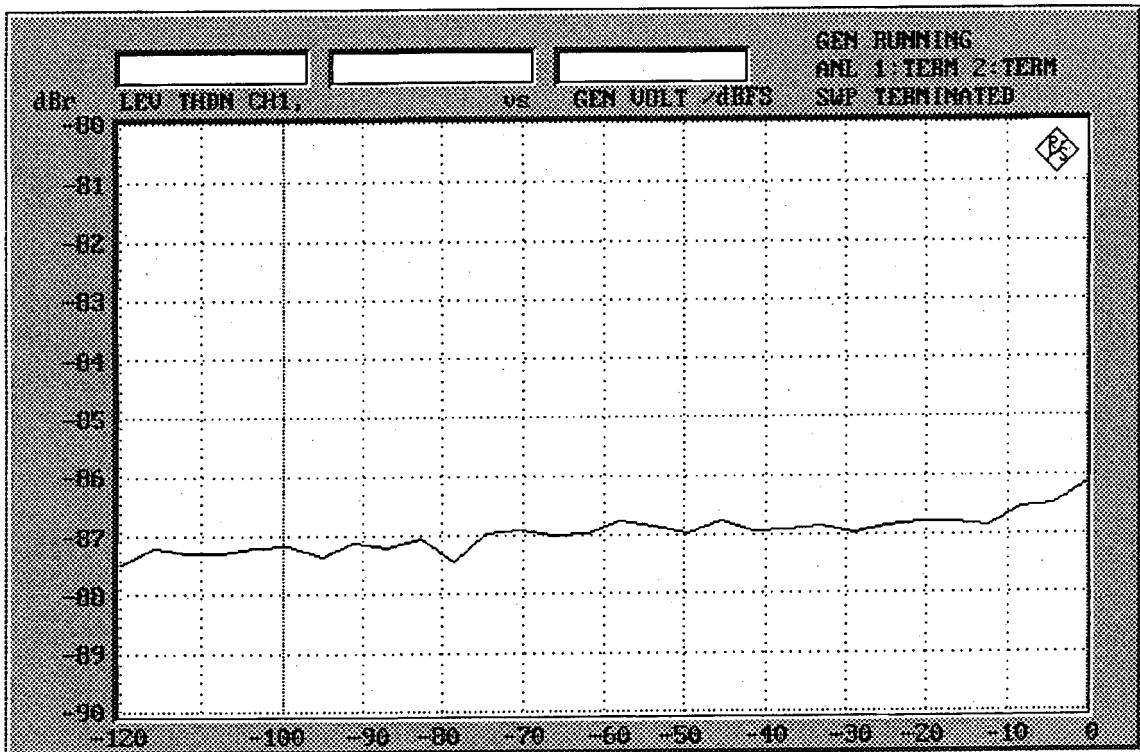


Fig.6 THD+N vs Input Level

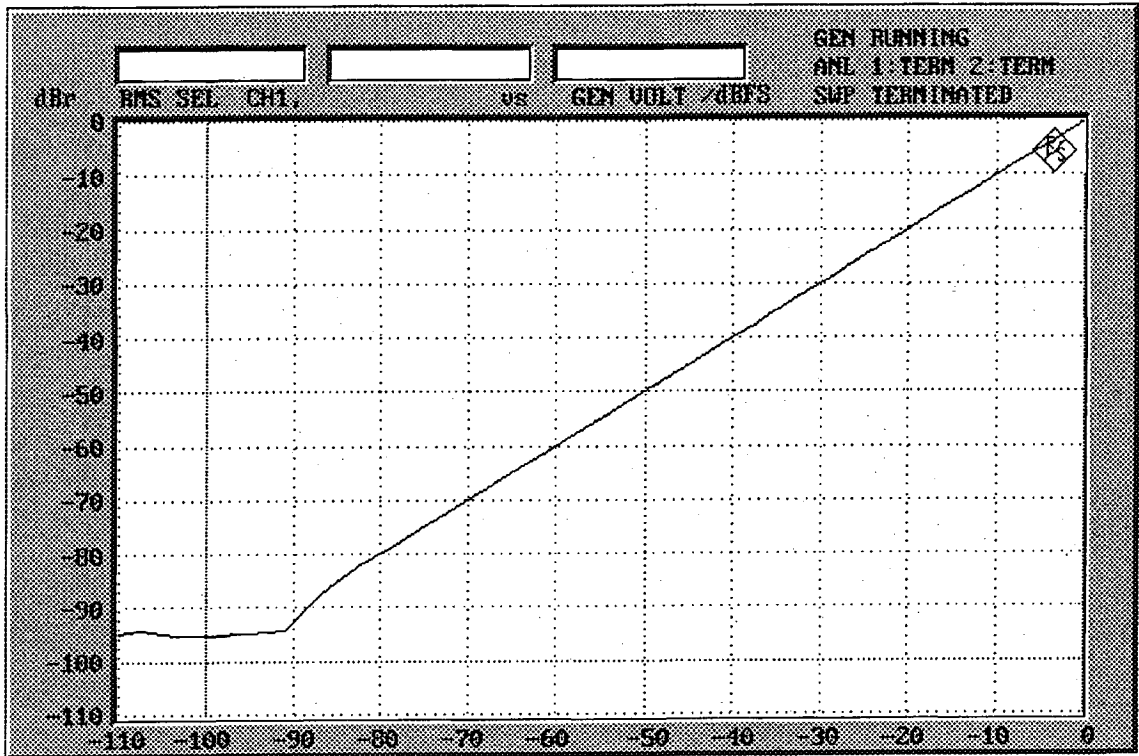


Fig.7 Linearity

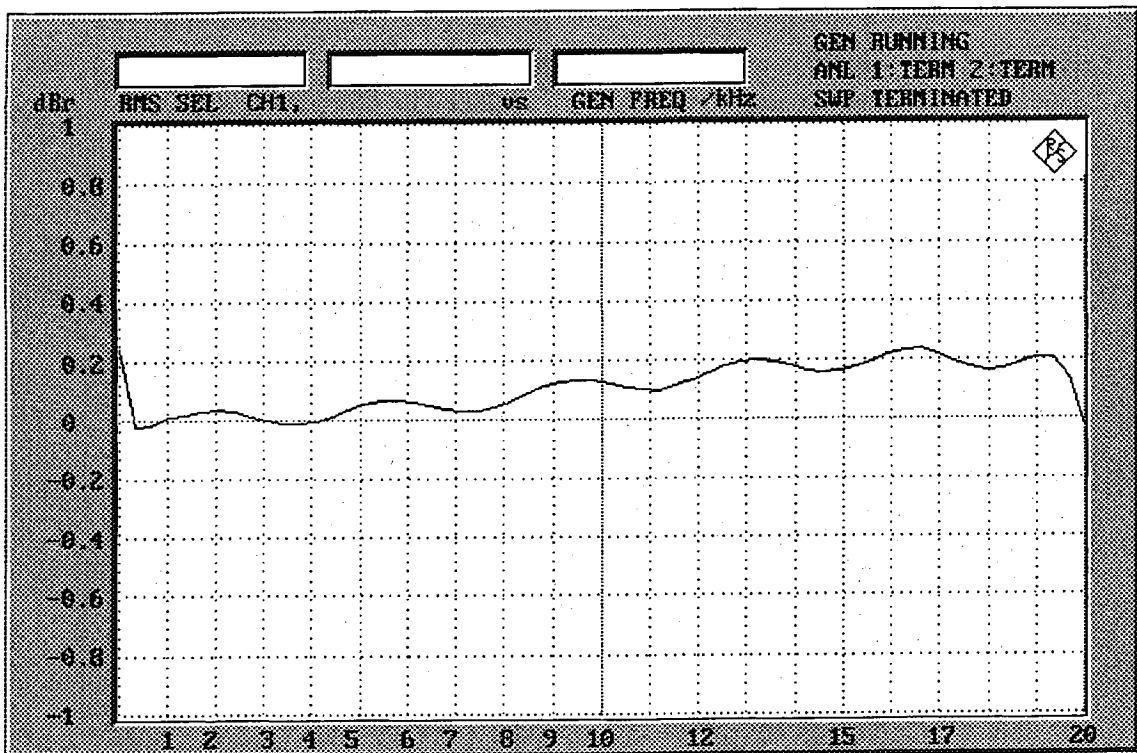


Fig.8 Frequency Response

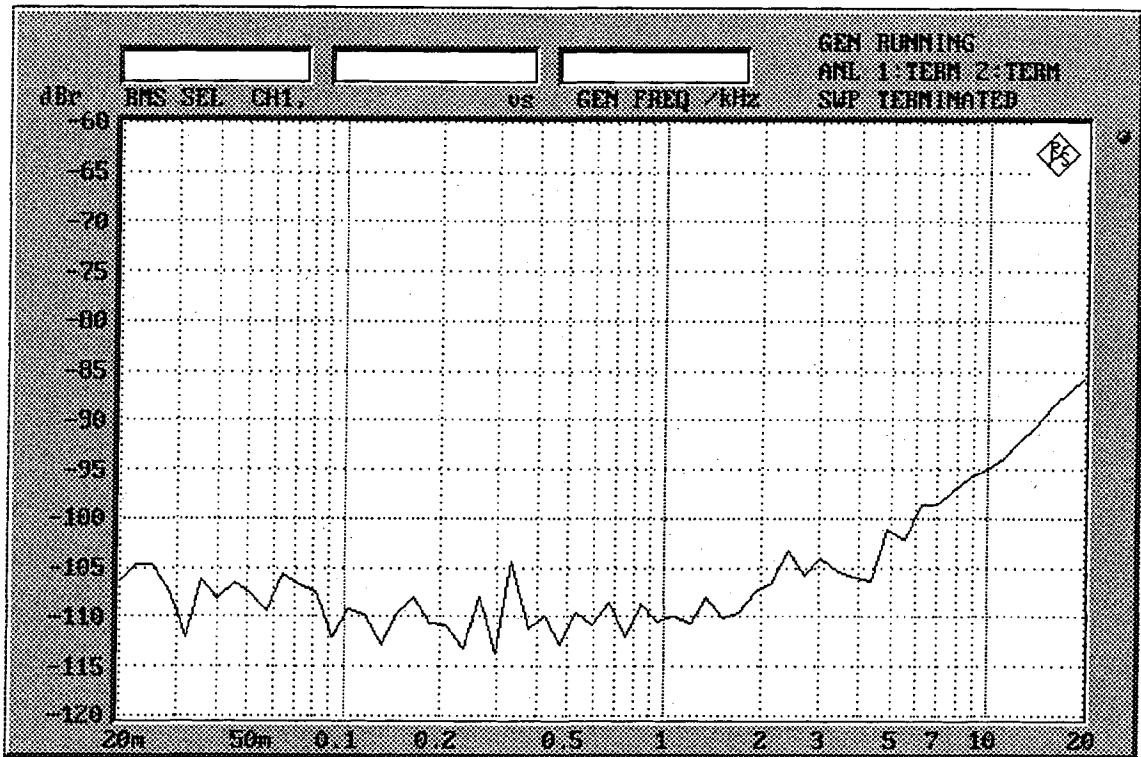
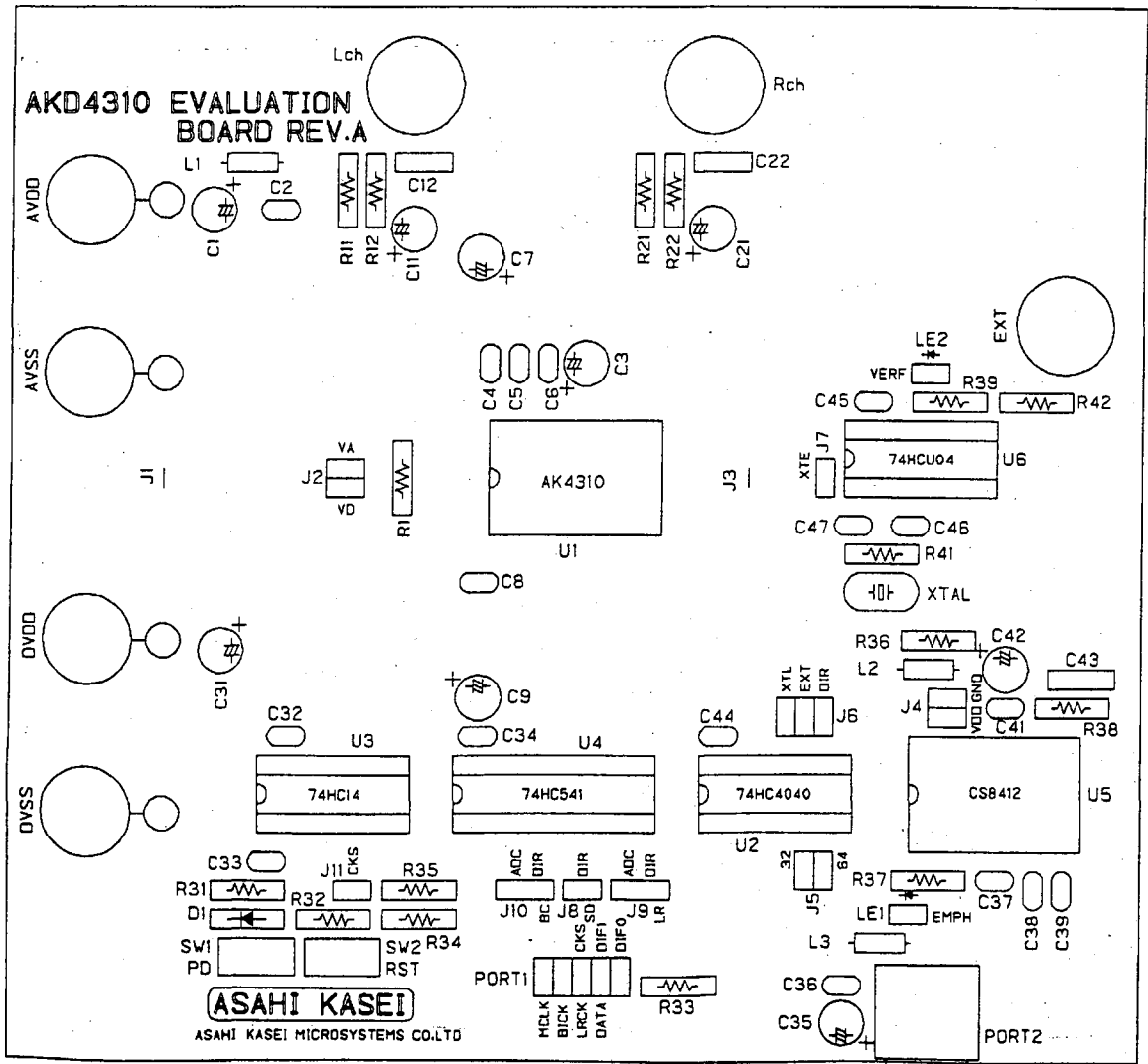
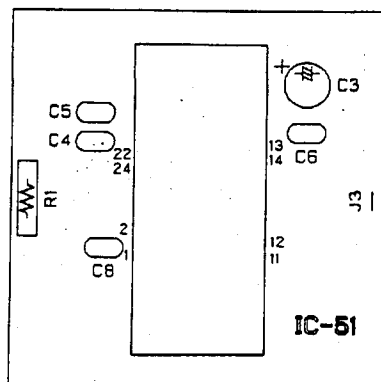
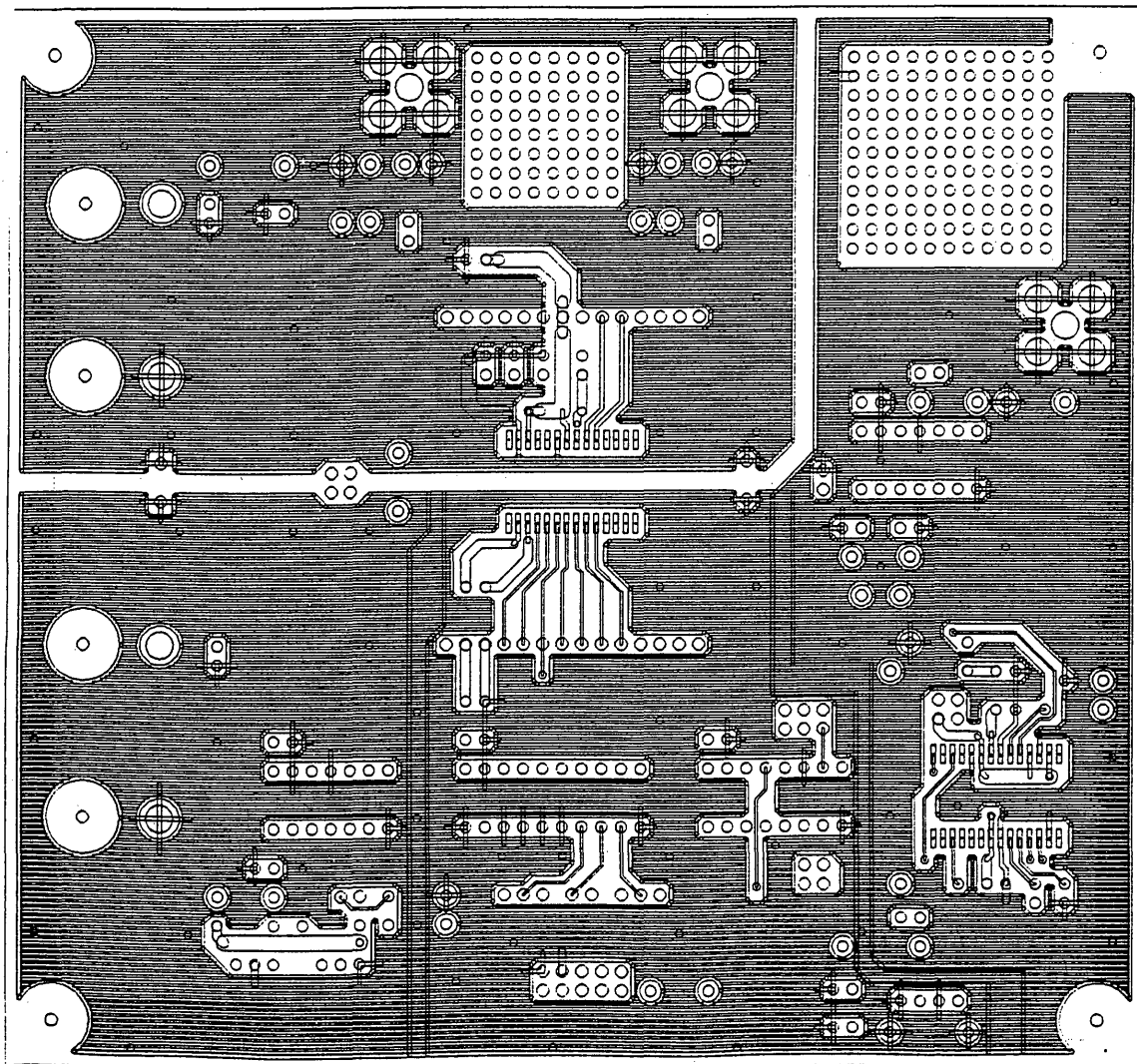


Fig.9 Crosstalk

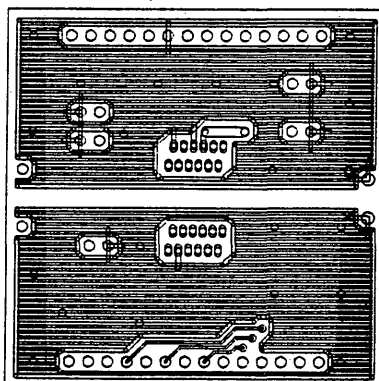


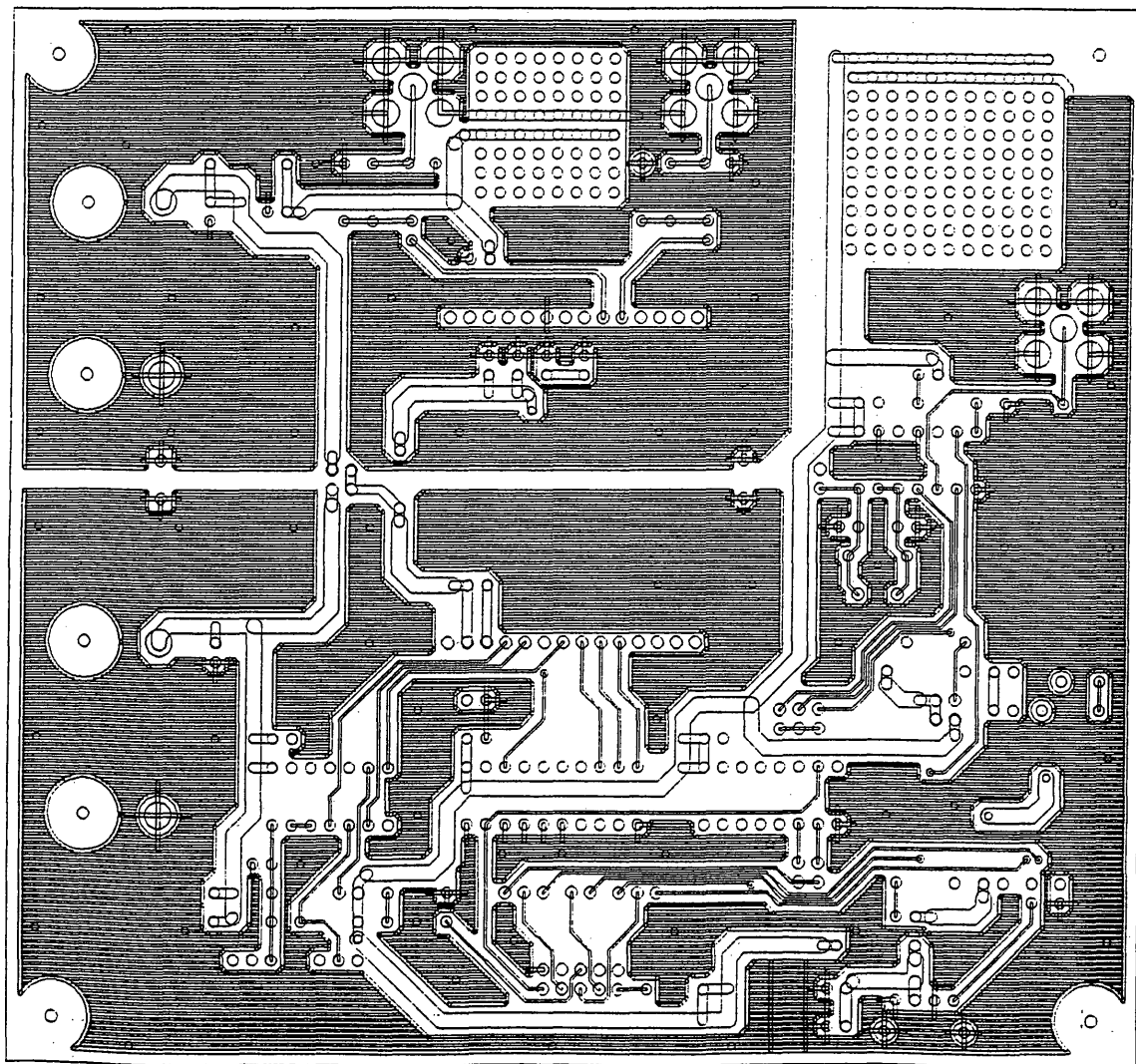
AKD4310 parts layout



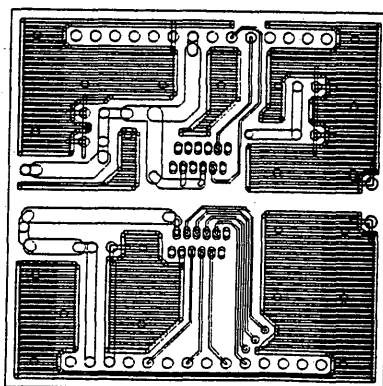


AKD4310 solder plane





AKD4310 ground plane



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