

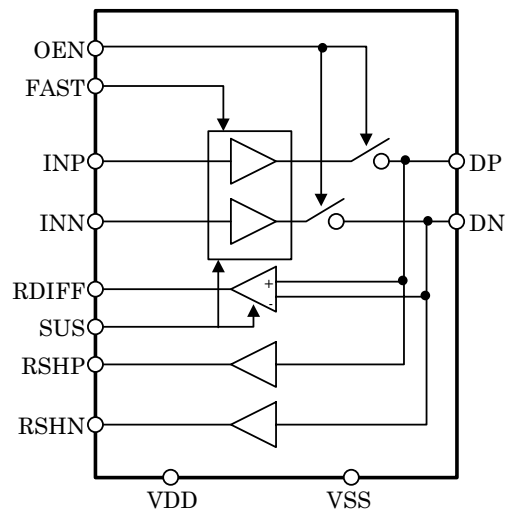


AK4170

USB Transceiver

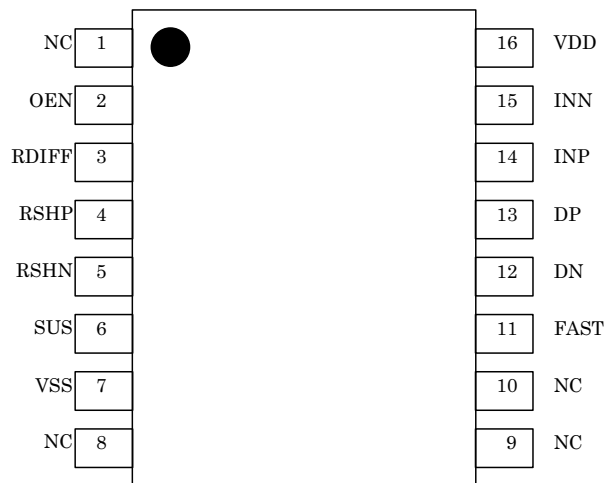
Features

- Ultra smooth output waveform
- Support full speed(12Mbps) and low speed(1.5Mbps)
- Single Power Supply 3.3 volts ± 10%
- 16pin TSSOP package
- Functionally compatible to Philips PDIUSBP11
- Support suspend mode



AK4170 Block Diagram

■ Pin Layout



Pin/Function			
No.	Signal Name	I/O	Description
1	NC	-	Not Connected
2	OEN	I	Output Enable Pin (CMOS level digital input) Low input enables transmit data, it is that both INP and INN output onto DP and DN pins. High input enable receive mode, which disables the outputs of DP and DN, and the buffer goes into high-z state.
3	RDIFF	O	Differential Receiver Output (CMOS level digital output) When DP > DN, the output is "H". When DP < DN, the output is "L". When both DP and DN are "L", the output is not guaranteed. this pin also outputs correctly regardless of the OEN input.
4	RSHP	O	Schmitt Hysteresis Receiver Output for DP (D+) input (CMOS level digital output) When DP is high level, RSHP is high. When DP is low level, RSHP is low this pin also outputs correctly regardless of the OEN input.
5	RSHN	O	Schmitt Hysteresis Receiver Output for DN (D-) input (CMOS level digital output) When DN is high level, RSHN is high. When DN is low level, RSHN is low this pin also outputs correctly regardless of the OEN input.
6	SUS	I	Suspend Mode Control Pin (CMOS level) High input forces the RDIFF output to low level, and the AK4170 goes into low power consumption mode regardless of OEN pin.
7	VSS	P	Ground Pin
8	NC	-	Not Connected
9	NC	-	Not Connected
10	NC	-	Not Connected
11	FAST	I	Full Speed/Low Speed Control Input (CMOS digital input) Low input activates the AK4170 to Low Speed (1.5Mbps) mode. High input activates the AK4170 to Full Speed (12Mbps) mode.
12	DN	I/O	Transmitter/Receiver Negative Data Output/Input Pin DN outputs the data of INN logic level when OEN is low DN disable the output, and goes to high-z state when OEN is high.
13	DP	I/O	Transmitter/Receiver Positive Data Output/Input Pin DP outputs the data of INP logic level when OEN is low DP disable the output, and goes to high-z state when OEN is high.
14	INP	I	Transmitter Positive Data Input Pin (CMOS digital input) When OEN is low, DP outputs INP logic level. When OEN is high, INP does not influence output pins.
15	INN	I	Transmitter Negative Data Input Pin (CMOS digital input) When OEN is low, DN outputs INN logic level. When OEN is high, INN does not influence output pins.
16	VDD	-	Power Supply Pin Connected to VSS with a 0.1uF capacitor.

Absolute Maximum Rating

VSS=0V

Parameter	Symbol	min	max	Units
Power Supplies	VDD		4.5	V
Digital Input Voltage	VIN	VSS-0.3	VDD+0.3	V
Digital Output Voltage	VO	VSS-0.3	VDD+0.3	V
Ambient Temperature	Ta	-40	+125	°C

Note 1. All voltages with respect to ground

Warning: Operation at or beyond these limits may results in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Recommended Operating Condition
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VSS=0V

Parameter	Symbol	min	typ	max	Units
Power Supplies	VDD	3.0	3.3	3.6	V
Operating Temperature	Ta	0		70	°C

All voltages with respect to ground.

Digital DC Characteristics					
Ta=25°C; VDD=3.0 - 3.6V; VSS=0V Measurement under static state					
Parameter	Symbol	min	typ	max	Units
“H” level input voltage	VIH	70%VDD			V
“L” level input voltage	VIL			30%VDD	V
“H” level output voltage	IOH=-1.5mA VOH	2.4			V
“L” level output voltage	IOL= 3.0mA VOL		-	0.6	V
“H” level Input Current	VIH=VDD IIH			10	μA
“L” level Input Current	VIL=0V IIL	10	-		μA

Transmitter Characteristics							
Ta=25°C; VDD=3.0 - 3.6V; VSS=0V							
Parameter	Symbol	Pins	Conditions	min	typ	max	Units
Output Impedance(Hi)	Roh	DP, DN	DP, DN="H"		40		Ω
Output Impedance (Lo)	Rol	DP, DN	DP, DN="L"		40		Ω
“H” level Output Voltage	Vohd	DP, DN	IOH=-200uA	2.8			V
“L” level Output Voltage	Vold	DP, DN	IOH=2.2mA			0.3	V
Tri-state Leakage Current	Iolk	DP, DN	OEN="H" 0 < DP, DN < 3.3V	-10		10	μA
Low Speed Propagation Delay (INP/INN to DP, DN)	Tpds	DP, DN, INP, INN	FAST="L"		170	300	ns
Full Speed Propagation Delay (INP/INN to DP, DN)	Tpdf	DP, DN, INP, INN	FAST="H"		15	20	ns
Low Speed Rise/Fall Time *)	Trs/Tfs	DP, DN	FAST="L"	75	180	300	ns
Full Speed Rise/Fall Time **)	Trf/Tff	DP, DN	FAST="H"	4	12	20	ns
Rise/Fall Time Matching	Trfm	DP, DN	FAST="L"		100		%
Rise/Fall Time Matching	Trfm	DP, DN	FAST="H"		100		%
Crossover Point	Vcrs	DP, DN			1.6		V
OEN Mode Change Delay	Tomcd	DP, DN	from OEN		10		ns
SUS Mode Change Delay	Tsmcd	DP, DN	from SUS		10		ns

*) CL=50pF for min, CL=350pF max

**) CL=50pF

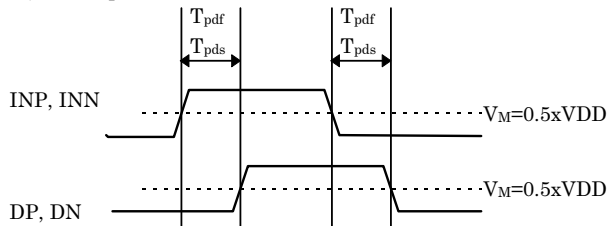


Figure Propagation Delay

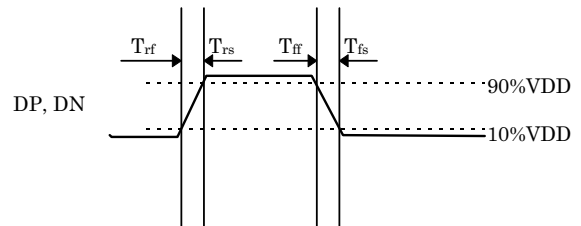


Figure Rise/Fall Time

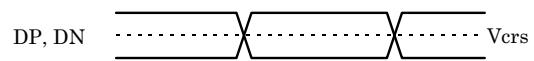


Figure Crossover Point

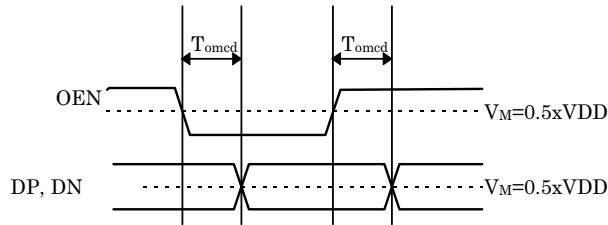


Figure OEN Mode Change Delay

Receiver Characteristics							
Ta=25°C; VDD=3.0 – 3.6V; VSS=0V							
Parameter	Symbol	Pins	Conditions	min	typ	max	Units
Common Mode Range(CMR)	CMR	DP, DN		0.8		2.5	V
Differential Input Sensitivity	DIS	DP, DN	within CMR			200	mV
Differential Receiver Delay	Tdrd	DP/DN to RDIFF	CL@RDIFF =50pF		14	25	ns
Schmitt Buffer Delay	Tsbd	DP/DN to RSHP, RSHN	CL@RSHP, RSHN=50pF		7	15	ns
Schmitt High Level Voltage	Vihs	DP, DN		2.0			V
Schmitt Low Level Voltage	Vils	DP, DN				0.8	V

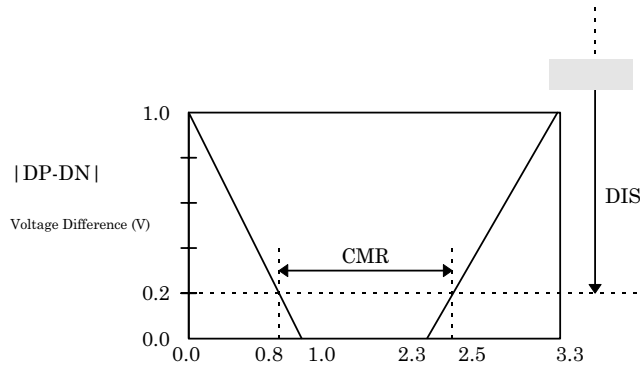


Figure Differential Input Sensitivity

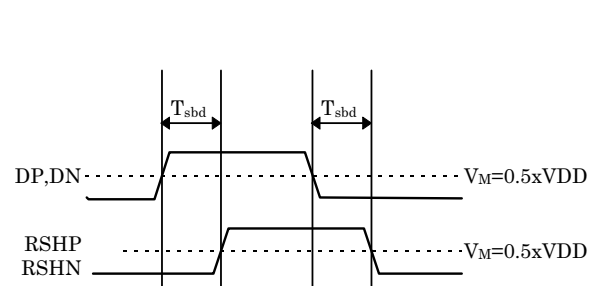


Figure Schmitt Buffer Delay

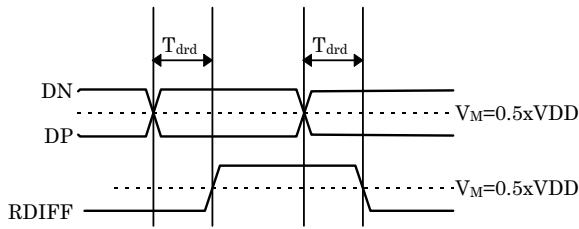


Figure Differential Receiver Delay

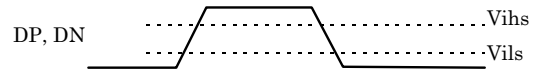
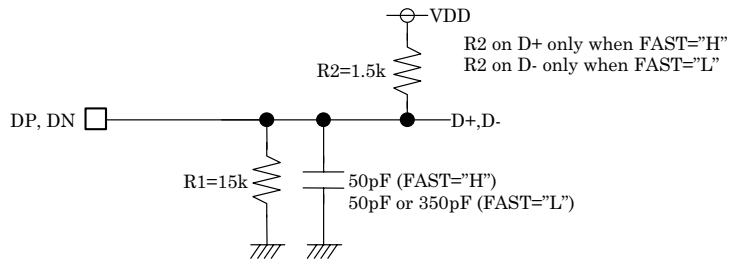


Figure Schmitt Level Voltage

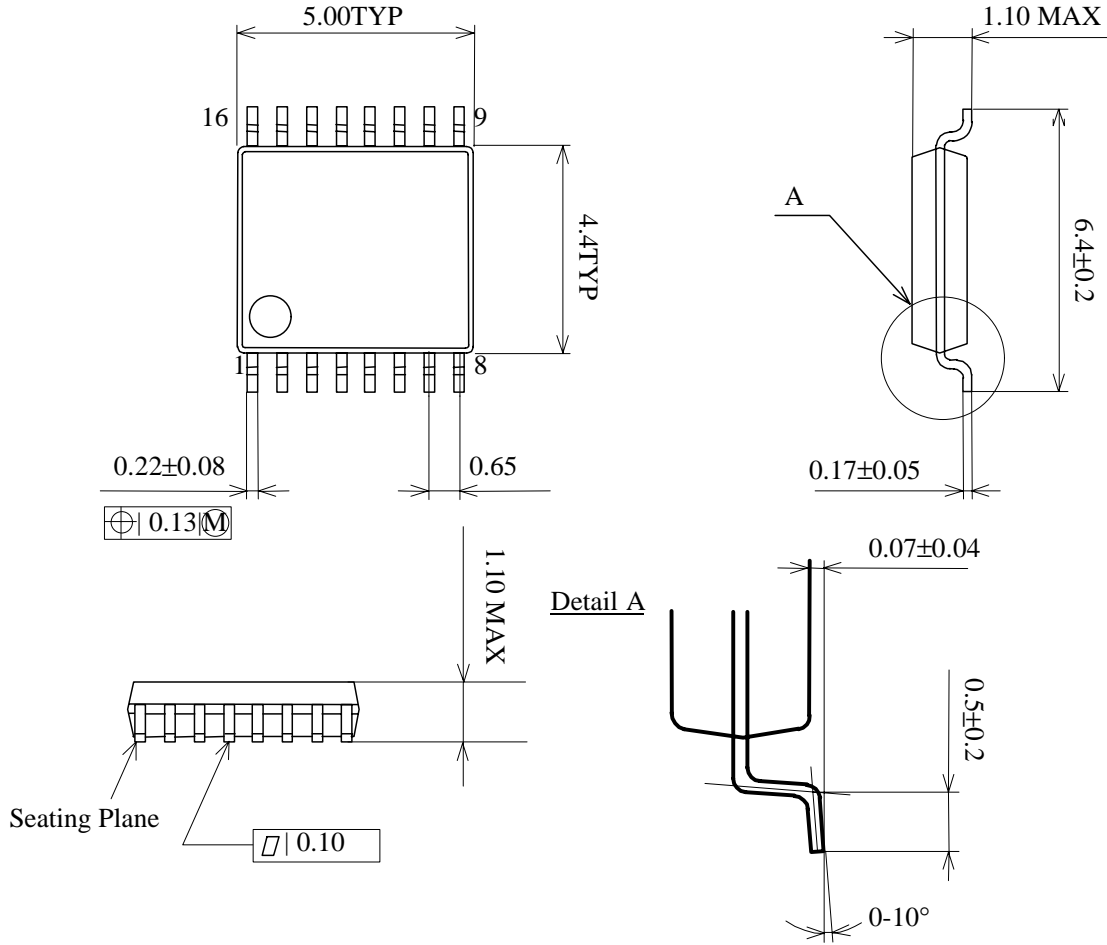
Power Dissipation						
Ta=25°C; VDD=3.0 - 3.6V ; VSS=0V						
Parameter	Symbol	Conditions	min	typ	max	Units
Operational Current (FAST="H",OEN="L")	Iddf	6MHz toggle input to INP,INN		16	30	mA
Operational Current (FAST="L",OEN="L")	Idds	750KHz toggle input to INP,INN		9	15	mA
Quiescent Current 1	Iddq1	Inputs idle state OEN="L", SUS="L"		5	10.0	mA
Quiescent Current 2	Iddq2	Input Idle State OEN="H", SUS="L"		450	900	μA
Suspend Current	Iddsus	Inputs idle state SUS="H"		4.0	80	μA



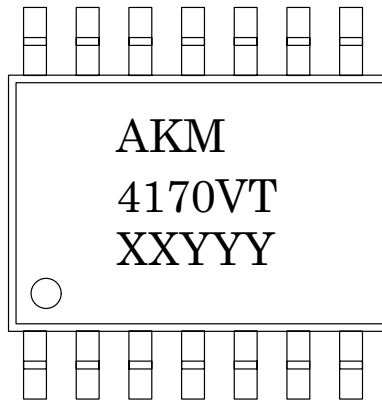
DP, DN are the AK4170 side, while D+,D- are the USB bus

Package

16pin TSSOP (Unit: mm)



Marking



Contents of XXYYY
XX: Lot #
YYY: Date Code

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