AKD4516A

Evaluation board Rev.A for AK4516A

General description

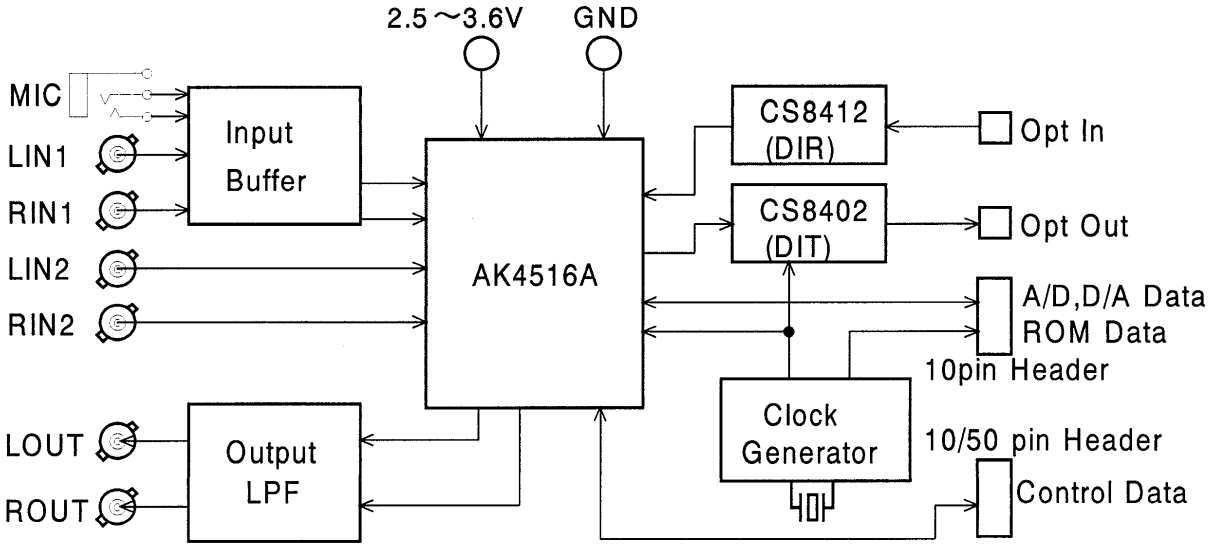
AKD4516A is an evaluation board for the digital stereo audio 16bit A/D and D/A converter, AK4516A. The A/D converter section includes the MIC circuit, the D/A converter section includes the 2nd order LPF. The AKD4516A can evaluate A/D converter and D/A converter separately in addition to loopback mode(A/D → D/A). The A/D converter section can be evaluated by interfacing with AKM's DAC evaluation boards (AKD4324, AKD4321, AKD4320, AKD4319) directly. The AKD4516A has the interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards (AKD5392, AKD5391, AKD5351 and AKD5351). Therefore, it is easy to evaluate the D/A section, The AKD4516A also has the digital audio interface and can achieve the interface with digital audio system via opt-connector.
The AK4516A is supplied by a 24pin VSOP. When shipping, the AKD4516A attaches the directly AK4516A to the AKD4516A. But the AKD4516A supplies a 24pin VSOP socket in the Sub-Board by request. Therefore, enables easier evaluation of other AK4516A devices.

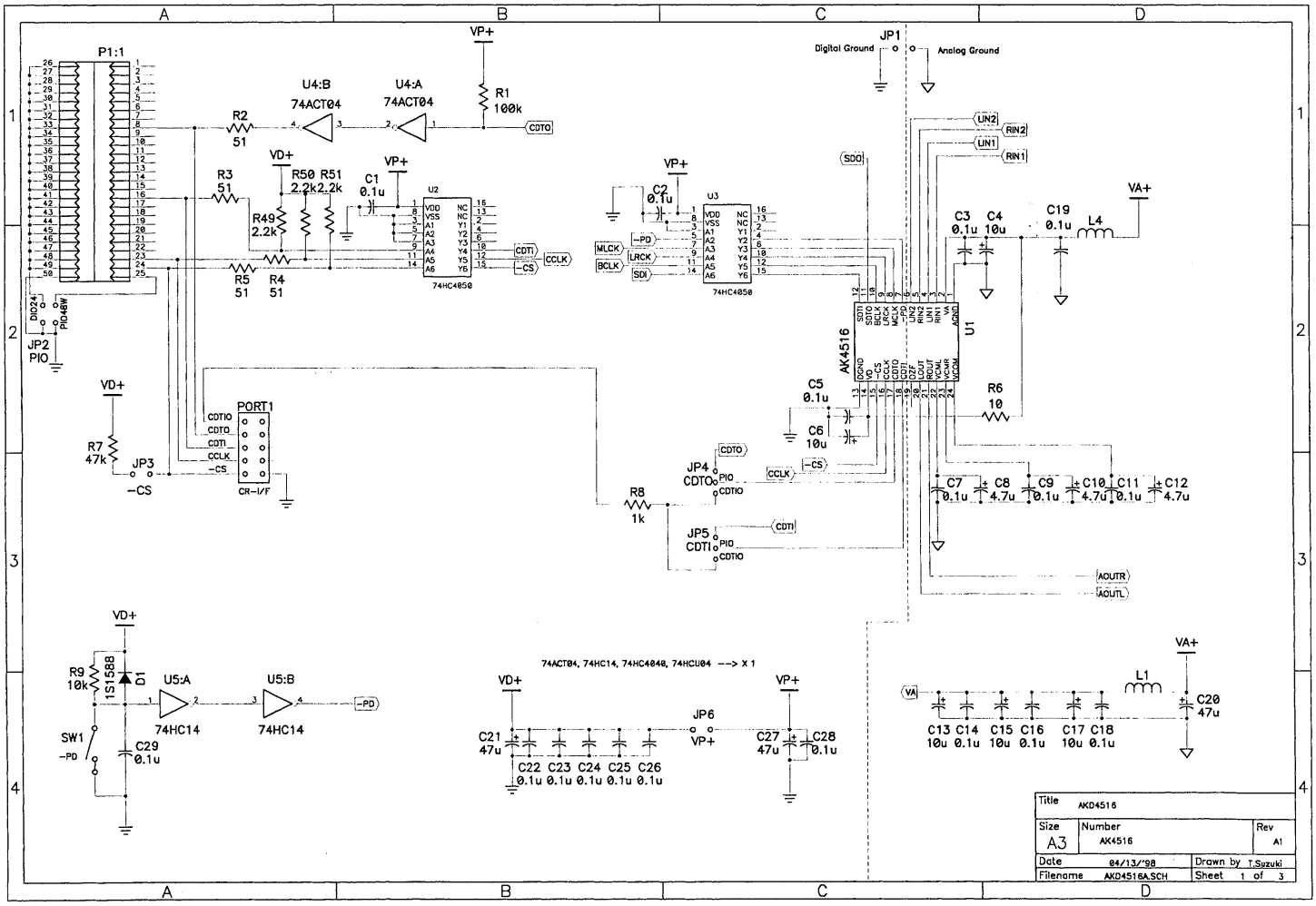
■ Ordering Guide

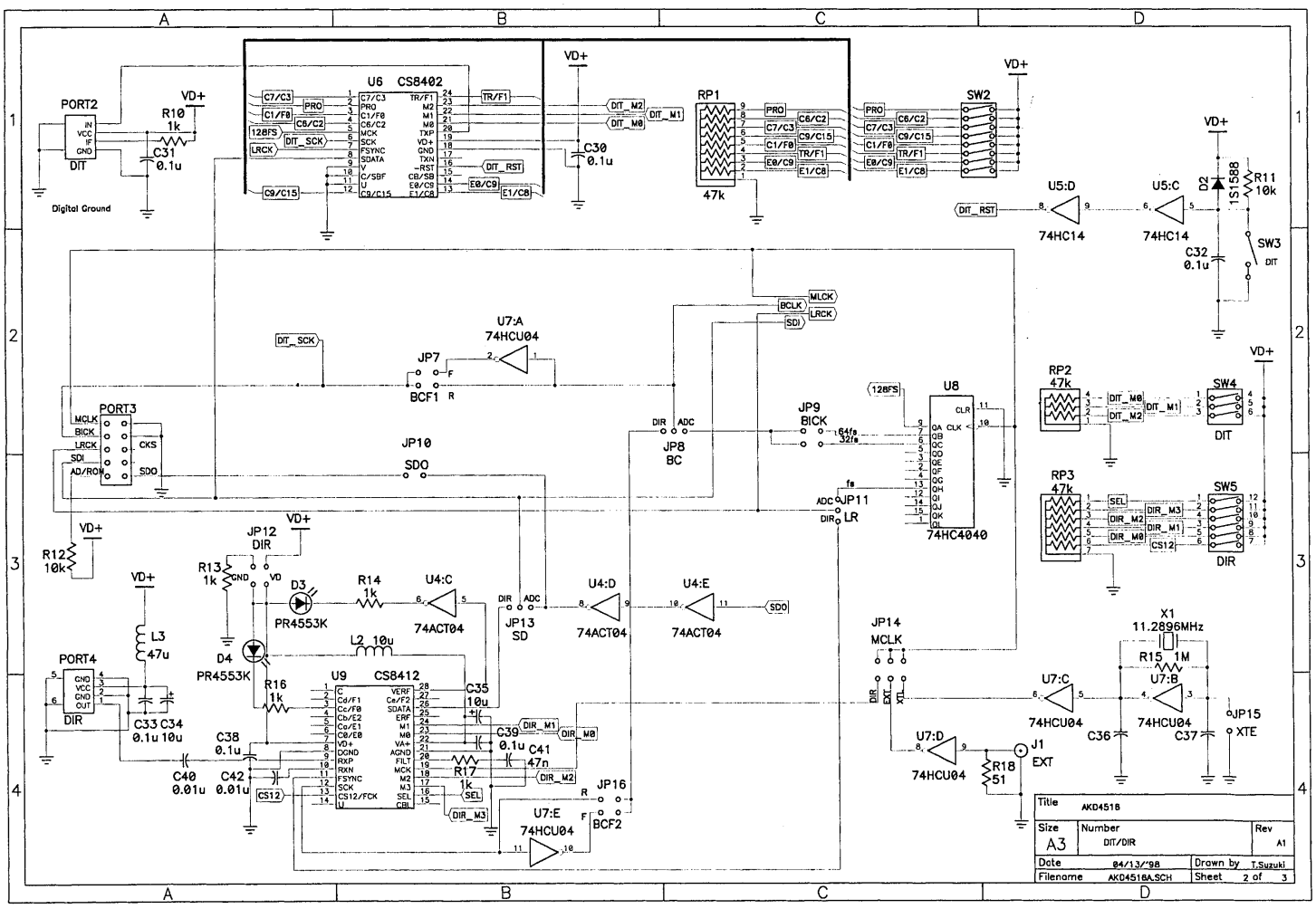
AKD4516A --- Evaluation board for AK4516A
AKD4516A Sub-Board --- Evaluation Sub-board for AK4516A

Function

- ☐ On-board MIC Input Buffer Circuit
- ☐ On-board 2nd order LPF for Analog Output
- ☐ On-board clock generator
- ☐ Compatible with following 2 types of interface
  - 1)Direct interface with AKM's A/D and D/A converter, and direct interface with a signal generator(AKD43XX) by 10pin Header
  - 2) DIT/DIR with optical input/output
- ☐ A BNC connector for an external clock input




P1:1
U4:B
74ACT04
U4:A
74ACT04
VP+
R1
100k
R2
51
CDTO
VD+
R3
51
R50 R51
2.2k2.2k
R49
2.2k
C1
0.1u
U2
74HC4050
CDTI
CCLK
R5
51
R4
51
DIO24
PIO48W
JP2
PIO
VD+
R7
47k
JP3
-CS
PORT1
CDTIO
CDTO
CDTI
CCLK
-CS
CR-I/F
U3
74HC4050
C2
0.1u
-PD
MLCK
LRCK
BCLK
SDI
SDO
JP1
Digital Ground
Analog Ground
LIN2
RIN2
LIN1
RIN1
C3
0.1u
C4
10u
C19
0.1u
L4
VA+
U1
AK4516
C5
0.1u
C6
10u
R6
10
JP4
CDTO
PIO
CDTIO
R8
1k
JP5
CDTI
PIO
CDTIO
C7
0.1u
C8
4.7u
C9
0.1u
C10
4.7u
C11
0.1u
C12
4.7u
AOUTR
AOUTL
R9
10k
1S1588
D1
U5:A
74HC14
U5:B
74HC14
-PD
SW1
-PD
C29
0.1u
74ACT04, 74HC14, 74HC4848, 74HCU04 --> X 1
VD+
VP+
JP6
VP+
C21
47u
C22
0.1u
C23
0.1u
C24
0.1u
C25
0.1u
C26
0.1u
C27
47u
C28
0.1u
VA
L1
VA+
C13
10u
C14
0.1u
C15
10u
C16
0.1u
C17
10u
C18
0.1u
C20
47u
Title
AKD4516
Size
A3
Number
AK4516
Rev
A1
Date
04/13/'98
Drawn by
T.Suzuki
Filename
AKD4516A.SCH
Sheet
1 of 3


A
B
C
D
1
2
3
4
PORT2
DIT
Digital Ground
R10 1k
C31 0.1u
VD+
U6 CS8402
C7/C3
PRO
C1/F0
C6/C2
128FS
DIT_SCK
LRCK
C9/C15
TR/F1
DIT_M2
DIT_M0
DIT_M1
DIT_RST
E0/C9
E1/C8
C30 0.1u
RP1
47k
SW2
U5:D
U5:C
74HC14
D2
1S1588
R11 10k
SW3
DIT
C32 0.1u
U7:A
74HCU04
JP7
BCF1
MLCK
BCLK
LRCK
SDI
PORT3
MCLK
BICK
LRCK
SDI
AD/ROM
CKS
SDO
JP10
SDO
JP8
BC
JP9
BICK
64fs
32fs
U8
74HC4040
JP11
LR
fs
RP2
47k
SW4
DIT
RP3
47k
SW5
DIR
SEL
DIR_M3
DIR_M2
DIR_M1
DIR_M0
CS12
R12 10k
JP12
DIR
R13 1k
GND
VD
D3
PR4553K
D4
PR4553K
R14 1k
U4:C
74ACT04
JP13
SD
U4:D
74ACT04
U4:E
74ACT04
SDO
L3 47u
L2 10u
PORT4
DIR
C33 0.1u
C34 10u
R16 1k
U9 CS8412
C35 10u
C39 0.1u
C41 47n
R17 1k
C38 0.1u
C40 0.01u
C42 0.01u
CS12
SEL
JP16
R
F
BCF2
U7:E
74HCU04
JP14
MCLK
X1
11.2896MHz
R15 1M
U7:C
U7:B
74HCU04
C36
C37
JP15
XTE
U7:D
74HCU04
J1
EXT
R18 51
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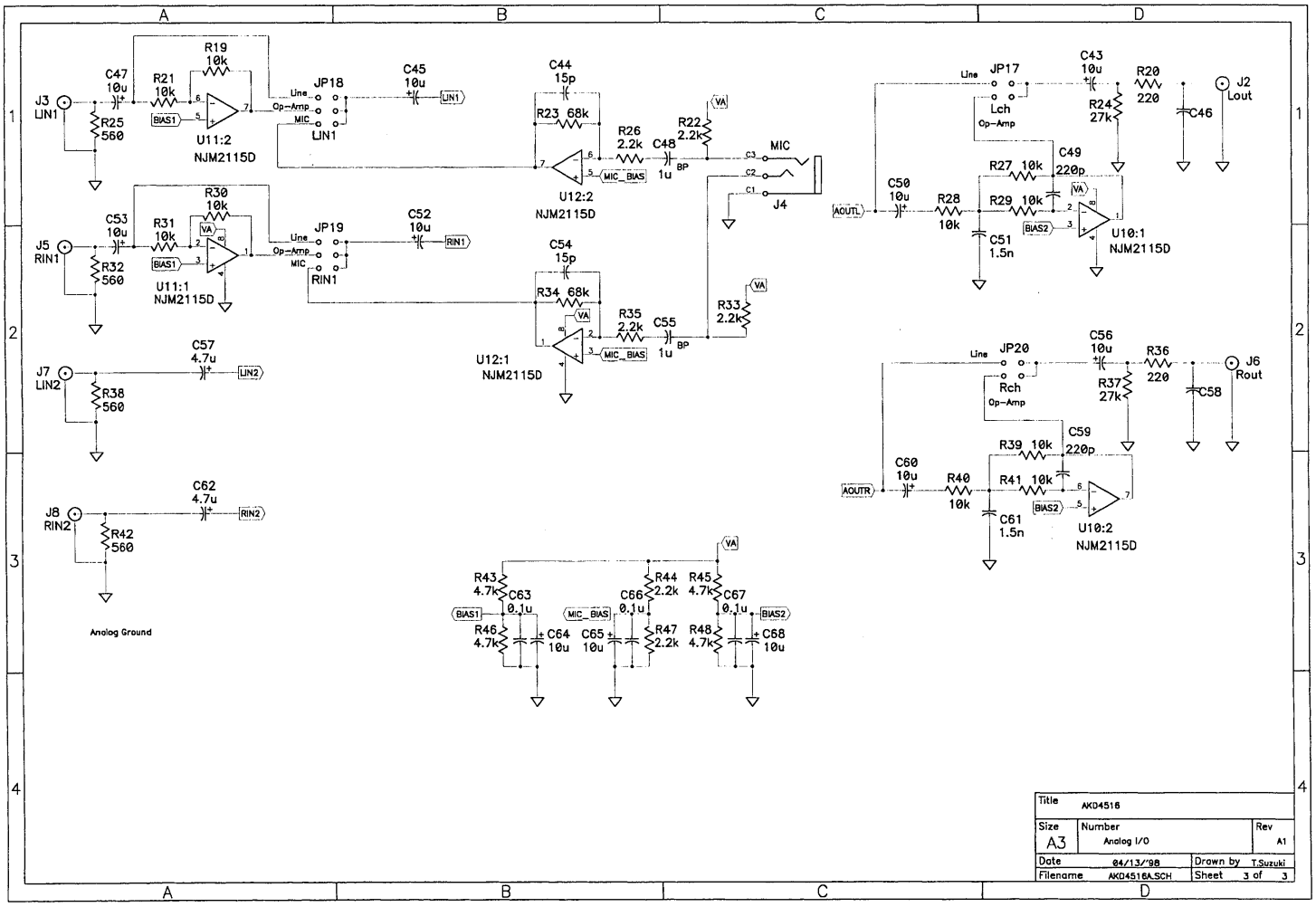
Size A3
Number DIT/DIR
Rev A1
Date 04/13/98
Drawn by T.Suzuki
Filename AKD4518A.SCH
Sheet 2 of 3



Title	AKD4516		
Size A3	Number Analog I/O		Rev A1
Date	04/13/'98	Drawn by	T.Suzuki
Filename	AKD4516A.SCH	Sheet	3 of 3

■ Input Buffer Circuit

External analog signal fed through the BNC connector is terminated by a resistor of 560 ohms. The resistor value should be properly selected in order to meet the output impedance of the signal source.

The input buffer circuit of LIN1 and RIN1 include inverted-amp of gain1(=0dB) or MIC circuit (inverted-amp of gain 30dB) with mini-jack, and the input buffer circuit can be selected by jumper pins(JP18 and JP19).

* Please take care of selecting JP18 and JP19 because of a difference in the order of LINE, MIC and OP-AMP.

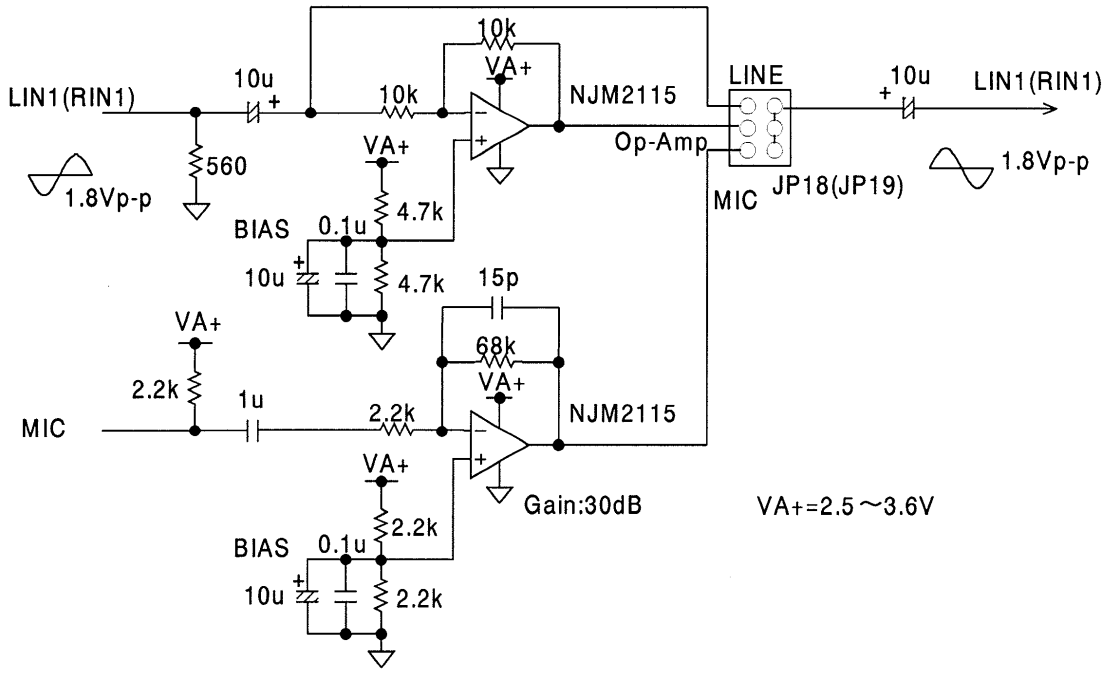


Figure 1. Input Buffer Circuit on board

※ AKM assumes no responsibility for the trouble when using the circuit examples.

■ Analog Output Circuit

The AK4516A includes a combination of switched-capacitor filter(SCF) and continuous-time filter(CTF) of single-ended output, so any external filters are not required.
Analog signals are output through BNC connectors on the board and the typical output level are about 1.8Vp-p.
When the attenuation of the out-of-band noise is needed, the 2nd order LPF(fc=27.7kHz, Q=0.87) with inverted-amp on the board should be used.

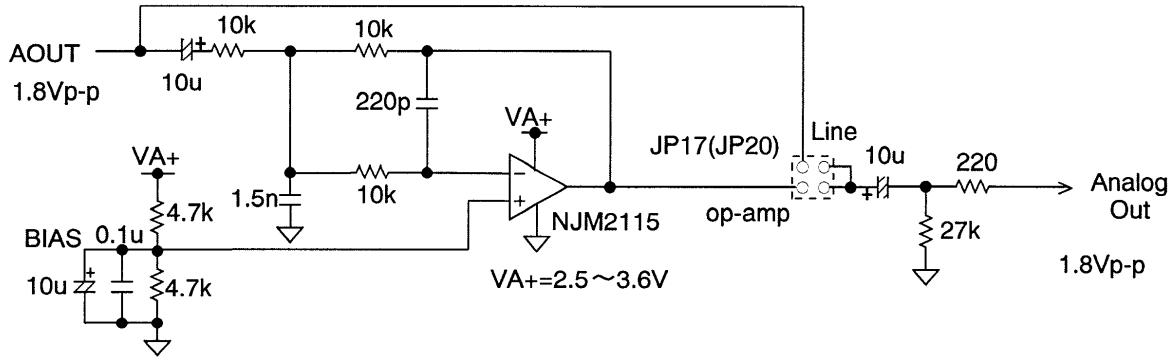


Figure 2. Analog filter on board

※ AKM assumes no responsibility for the trouble when using the circuit examples.

■ Grounding and Power Supplies Decoupling

To minimize the coupling by digital noise, decoupling capacitors should be connected to VD and VA respectively. The VA is supplied from analog supply in system and the VD is supplies from VA via 10 ohms. Decoupling capacitors should be connected to AK4516A as near as possible, with the low value ceramic capacitor for VCML, VCMR, VCOM, VA and VD pins being the nearest.

■ Operation sequence

① Set up the power supply lines
VA+=VP+=2.5 ~ 3.6V, VD+=2.5 ~ 5V, AGND=DGND=0V
Each supply line should be distributed from the power unit.
The only CS8402 and CS8412 on the board needs VD+ ≧ 3.4V.
When changing the voltage of VP+ and VD+, JP6 should be open.
VA+ should be powered at the same time or earlier than VP+.

② Set up the evaluation modes and jumper pins. (See the next item)
There are many jumper pins to cover many evaluation mode.
Please tale care of setting.

③ Set up the DIP switch (See the next item)
Set up the AK4516A and DIT.
Please tale care of setting.

④ Power on
The AK4516A should be reset once by bringing SW1="L" upon power-up.

⑤ AK4516A can be reset by SW1 during operation.
"L" position resets the device, and the "H" position is for normal operation.

■ The evaluation modes and corresponding jumper pin settings.

1. Evaluation Mode

Applicable Evaluation Mode

① Loopback mode (Default)
② Using A/D converted data from ideal sine wave generated by ROM data
③ Using A/D converted data
④ DIR (Optical Link)
⑤ Using D/A converted data
⑥ DIT (Optical Link)
⑦ All interface signals including master clock are fed externally.

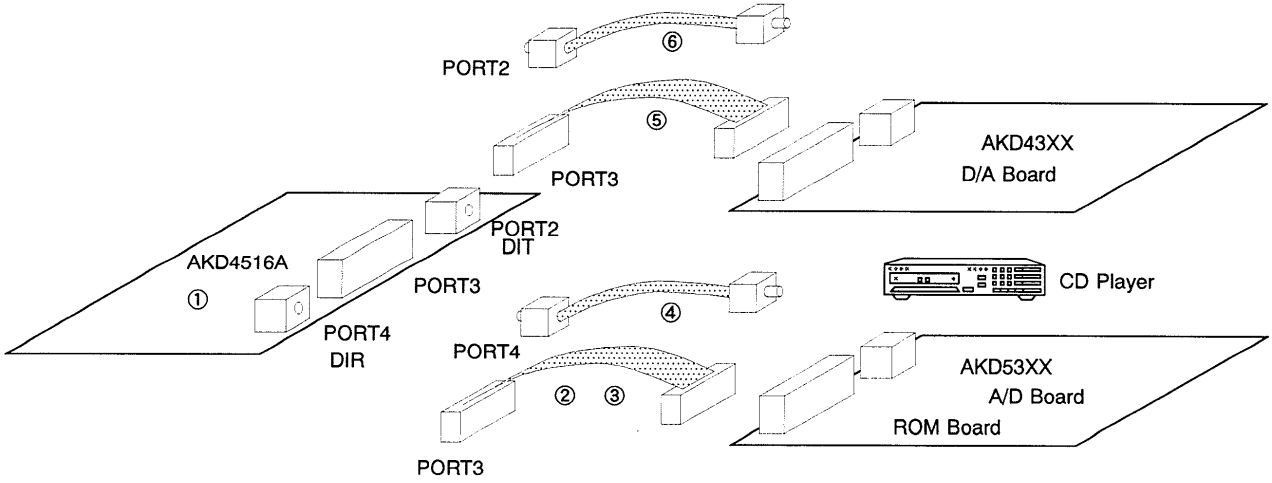


Figure 3. Wiring cables corresponded some evaluation modes

① Loopback mode(Default)

Don't connect any one to PORT3 and PORT4. In case of using external clock through a BNC connector, select EXT on JP14(MCLK) and short JP15(XTE).
Corresponding Audio I/F format changes depending on the frequency of BICK
a. BICK=32fs
BICK=32fs corresponds to No.0, No.2, No.3 of Audio I/F format.
b. BICK=64fs
BICK=64fs corresponds to No.1, No.2, No.3 of Audio I/F format.

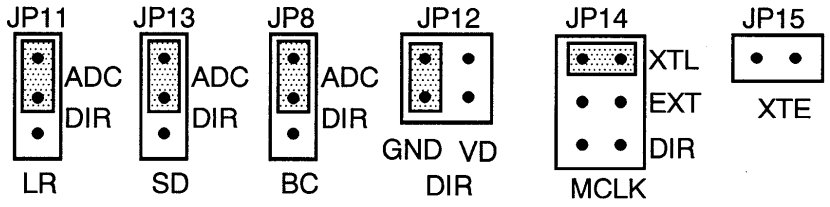


Figure 4. Jumper Set up (Loopback mode)

② Using A/D converted data from ideal sine wave generated by ROM data

Digital signals generated by AKD43XX are used. PORT3 is used for the interface with AKD43XX. Master clock is sent from AKD4516A to AKD43XX and LRCK, BCLK, SDTI are done from AKD43XX to AKD4516A. In case of using external clock through a BNC connector, select EXT on JP14(MCLK), short JP15(XTE) and opens JP10(SDO).

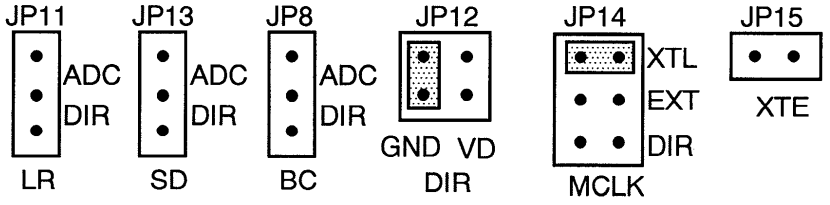


Figure 5. Jumper Set up (ROM)

③ Using A/D converted data

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards (AKD5392, AKD5391, AKD5352, AKD5351) with PORT3. In case of using external clock through a BNC connector, select EXT on JP14(MCLK) and short JP15(XTE). Then JP10(SDO) should be open.

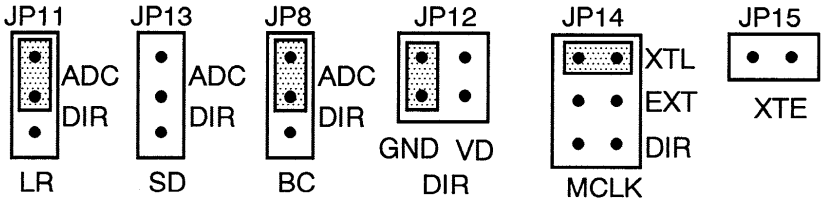


Figure 6. Jumper Set up (A/D)

④ DIR (Optical Link)

PORT4 is used. DIR generates MCLK, BICK and LRCK from the received data through optical connector(TORX176). Used for the evaluation using CD test disk. Nothing should be connected to PORT2 and PORT3. CS8412(DIR) needs the operating voltage of VD+ ≧ 3.4V.

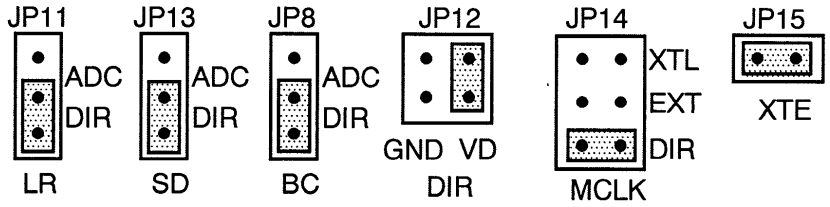


Figure 7. Jumper Set up (DIR)

⑤ Using D/A converted data

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's D/A evaluation boards (AKD4324, AKD4321, AKD4320, AKD4319) with PORT3. Then JP10(SDO) should be open.

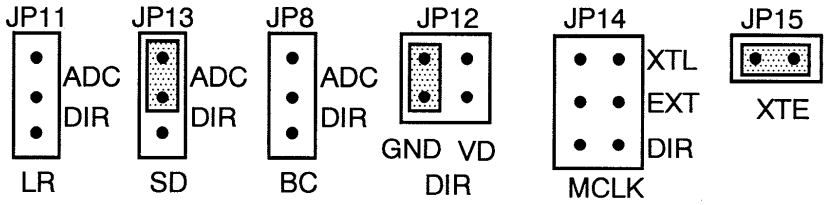


Figure 8. Jumper Set up (D/A)

⑥ DIT (Optical Link)

PORT2 is used. DIT generated SDATA from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's evaluation boards (AKD4324, AKD4321, AKD4320, AKD4319) , digital-amplifier and etc. Nothing should be connected to PORT3 and PORT4. This set-up is the same as ① as it. CS8402(DIT) needs the operating VD+ ≧ 3.4V. SW2 is kept the "H" during normal operation.

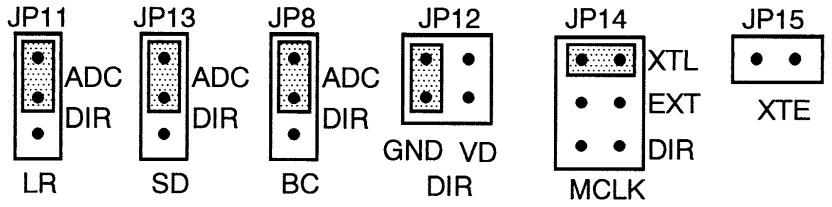


Figure 9. Jumper Set up (DIT)

⑦ All interfacing signals including master clock are fed externally.

Under the following set-up, all external signals needed for the AK4516A to operate could be fed through PORT3. In case of interfacing external sources to D/A converter, JP13(SD) should be open. And in case of using A/D data to externally, JP13(SD) is set ADC position. When JP13(SD) is open, the A/D data can be output from the PORT3 at the same time if JP10(SDO) is shortened.

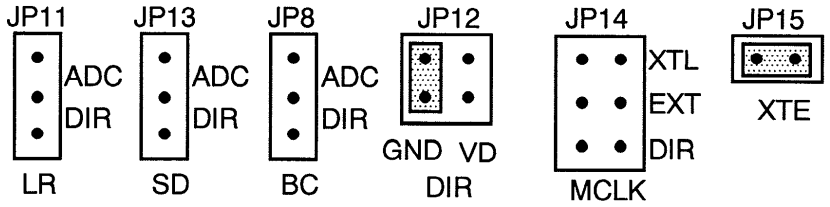
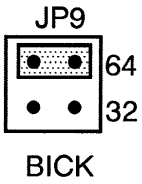


Figure 10. Jumper Set up (EXT)

2. BIT CLOCK(BCLK) set up



[JP9] The bit clock (BCLK) sets up
32: 32fs, 64: 64fs
Figure shows 64fs examples.

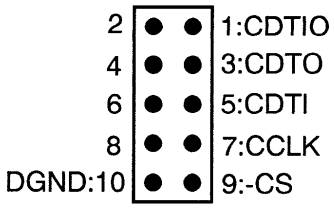
3. Interface circuit for control registers

The control registers in the AK4516A can be controlled by external uP, printer port of PC via PORT1 (10pin-Header) .

① In case of using printer port for PC

The control registers can be controlled by connecting between PORT1 on the AKD4516A and printer-port of personal computer by using a special cable(10pin Header − 25pin D-Sub). In this case, an interface of 3-wires(connected CDTO to CDTI) can not be done.

The following figure is pin-assignment of the 10pin-Header. Please take care of connecting a cable as there is a sign indicating 1-pin of connector.



The jumper setting is as follows.
[JP2]: Don't care
[JP3]: Open
[JP4][JP5]: PIO

[JP2] Don't care

[JP3] Short: $\overline{CS}$ pin is pulled-up by a resistor of 47k ohms.
This mode is only used to evaluate analog characteristics of the AK4516A.
Then the AKD4516A can not be controlled by external uP or personal computer.
Open: $\overline{CS}$ pin can be controlled by PORT1 or P1.

[JP4] PIO: A data of CDTO pin is output from PORT1 and P1.
CDTIO: 3-wires interface can be controlled by connecting CDTI pin to CDTO pin.
In this case, only PORT1 can be input/output.

[JP5] PIO: A data of CDTI pin is input to PORT1 and P1.
CDTIO: 3-wires interface can be controlled by connecting CDTI pin to CDTO pin.
In this case, only PORT1 can be input/output.

4. Jumper set up and explanation

[JP6] Short VD+ and VP+.
In case of separating VD+ and VP+ supplies, JP6 should be open.

■ The function of the toggle SW

[SW1] Reset the AK4516A. In case of "L" position, AK4516A becomes power-down status. In case of "H" position, AK4516A becomes normal operation.
[SW3] Reset the CS8402. "L" position resets the internal counter of CS8402, then Bi-phase signal is not output. Keep "H" position during normal operation.

■ The indication content for LED

[D3] Monitor VERF pin of the CS8412. LED turns on when some error has occurred to CS8412.
[D4] Indicates whether the input data is pre-emphasized or not. LED turns on when the data is pre-emphasized.

■ DIP switch set up

Confirm the set up of the DIP-SW before evaluation starts. ON means "1", OFF, "0".

1. SW5: Set up the operation modes of the CS8412
Set up the CS8412's(DIR) data format corresponding the serial data interface of the AK4516A.
Don't forget that JP16(BCF2) should be set up.

No.	PIN	ON	OFF	
1	CS12	Rch	Lch	*2
2	M0	Refer to Table 2.		*Be careful of a row of M0-3.
3	M2			
4	M1			
5	M3			
6	SEL	Normally ON *1		

*1 When "ON", it shows pre-emphasis on EMPH. (LED turns on)
*2 Select the channel whose status is represented.

Table 1. DIP SW set up of the CS8412.
(Refer to the CS8412 data sheet.)

No.	AK4516A's DIF0 bit	AK4516A's DIF1 bit	AK4516A's SDI(DAC)	SW5-5 M3	SW5-4 M1	SW5-3 M2	SW5-2 M0	JP16 BCF2	
0	0	0	LSB, justified	0	0	1	1	R	*3
1	1	0	LSB, justified	0	0	1	1	R	
2	0	1	MSB, justified	0	0	0	0	F	
3	1	1	IIS compatible	0	1	0	0	R	

*3 Default

Table 2. Set up Audio Data Format of DIR
(DIF1 and DIF0 bits are changed by the internal register of the AK4516A.)

[JP16:BCF2]: Define the polarity of BICK from outputting CS8412(DIR).
F: BCLK is inverted.
R: BCLK coincides with AK4516A

2. SW4: Set up the operation mode of CS8402(DIT)
Set up the CS8402's(DIT) data format corresponding the serial data interface of the AK4516A.
Don't forget that JP7(BCF1) should be set up.

No.	AK4516A's DIF0 bit	AK4516A's DIF1 bit	AK4516A's SDI(ADC)	SW4-1 M2	SW- 2 M1	SW4-3 M0	JP7 BCF1	
0	0	0	MSB, justified	0	0	1	F	*4
1	1	0	LSB, justified	1	0	1	R	*5
2	0	1	MSB, justified	0	0	1	F	
3	1	1	IIS compatible	1	0	0	R	

*4 Defalut
*5 JP9(BICK):64fs

Table 3. DIP SW set up of the CS8402(DIT)
(DIF1 and DIF0 bits are changed by the internal register of the AK4516A.)
(Refer to the CS8402 data sheet.)

[JP7:BCF1]: Define the polarity of BCLK from outputting CS8402(DIT).
F: BCLK is inverted.
R: BCLK coincides with AK4516A

3. SW2: This switch sets the C-bit of CS8402. (Default is the consumer mode)

This set up does not affect the evaluation of the AK4516A. In case of using DIT, need to set it up correctly. For more detailed configurations, please refer to the CS8402 data-sheet.

Switch	OFF=0,ON=1	Contents
8	$\overline{PRO}$=0	Professional mode, C0=1
6,7	$\overline{C6}$,$\overline{C7}$	C6,C7 - Sampling frequency
	1 1 1 0 0 1 0 0	00 - Not indicated. Receiver default to 48kHz. 01 - 48kHz 10 - 44.1kHz 11 - 32kHz
5	$\overline{C9}$	C8,C9,C10,C11 - 1bit of channel mode
	1 0	0000 - Mode not indicated. Receiver default to 2-channel mode. 0100 - Stereophonic.
4	$\overline{C1}$	C1 - Audio mode
	1 0	0 - Normal audio 1 - Not audio
3	TRNPT	Transparent mode *CS8402 is CRE
	0 1	Normal mode Transparent mode
1,2	EM1,EM0	C2,C3,C4 - Encoded audio signal emphasis
	1 1 1 0 0 1 0 0	000 - Emphasis not indicated. Receiver defaults to no emphasis with manual override enable. 100 - None 110 - 50/15usec 111 - CCITT J.17

Table 4. DIP switch set up of CS8402 (Professional mode)

Switch	OFF=0,ON=1	Contents
8	$\overline{PRO}$=1	Consumer mode, C0=0 (Default)
7	$\overline{C2}$	C2 - Copy
	1	0 - Copy inhibited
Default	0	1 - Copy permitted
6	$\overline{C3}$	C3,C4,C5 - Pre-emphasis
Default	1	000 - None
	0	100 - 50/15usec
5	$\overline{C15}$	C15 - Generation Status
	1	0 - See the standard
Default	0	1 - See the standard
3,4	FC1,FC0	C24,C25,C26,C27- Sampling frequency
	0 0	0000 - 44.1kHz
Default	0 1	0100 - 48kHz
	1 0	1100 - 32kHz
	1 1	0000 - 44.1kHz, CD mode
1,2	$\overline{C8}$,$\overline{C9}$	C8-C14 - Category code
Default	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - CD
	0 0	1100000 - DAT

Table 5. DIP switch set up of CS8402(Consumer mode)

AK4516A Measurement Result Examples

■ Dynamic Characteristics

[Measurement conditions]

- Measurement Unit : Audio Precision, System One
- Sampling frequency(fs) : 44.1kHz
- BCLK : 64fs
- Power Supply : VA+=VP+=3.0V, VD+=4.0V
- Interface : DIT/DIR
- Temperature : Room temperature
- Response : RMS mode

1. Analog through mode (PM3-0:09H)

Parameter	Input signal	Measurement Filter	Results
S/(N+D)	1kHz,0dB	20kHzLPF	89.4dB
DR	1kHz,-60dB	20kHzLPF	89.7dB
	1kHz,-60dB	22kHzLPF + A-weight	92.8dB
S/N	1kHz,0dB/GND IN	20kHzLPF	89.7dB
	1kHz,0dB/GND IN	22kHzLPF + A-weight	92.8dB

* 0dB is full scale of ADC input.

2. IPGA + ADC Output

- Bandwidth : 20 ~ 20kHz

Parameter	Input signal	Additional Filter	Results
S/(N+D)	1kHz,-2dB		85.4dB
DR	1kHz,-60dB		86.2dB
S/N	1kHz,0dB/GND IN		86.3dB
	1kHz,0dB/GND IN	A-weight	90.2dB

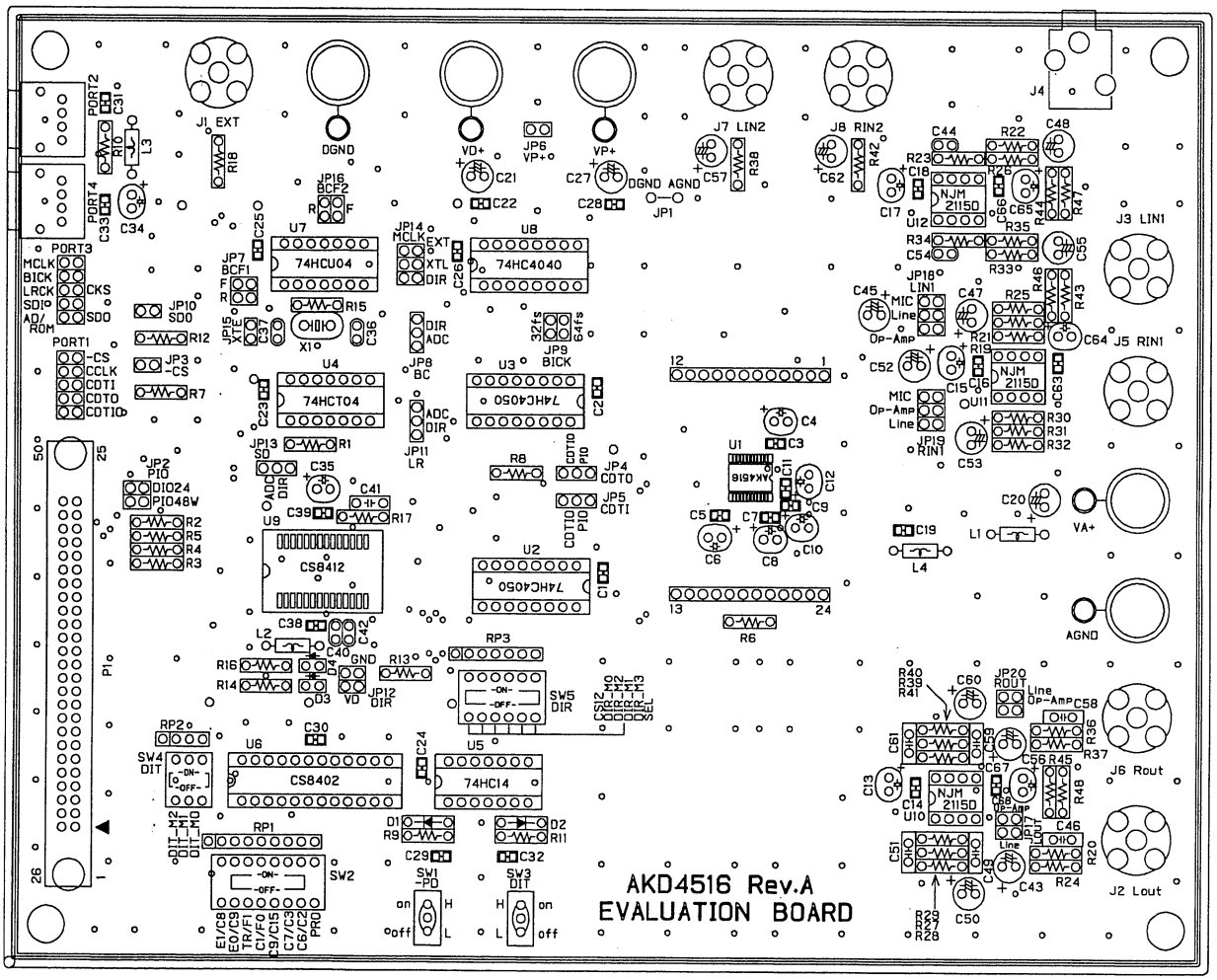
* 0dB is full scale of ADC input.

3. DAC Output (External filter none)

Parameter	Input signal	Measurement Filter	Results
S/(N+D)	1kHz,0dB	20kHzLPF	86.5dB
DR	1kHz,-60dB	20kHzLPF	87.2dB
	1kHz,-60dB	22kHzLPF + A-weight	89.7dB
S/N	1kHz,0dB/GND IN	20kHzLPF	87.4dB
	1kHz,0dB/GND IN	22kHzLPF + A-weight	90.5dB

4. IPGA + ADC → DAC Loopback (External filter none)

Parameter	Input signal	Measurement Filter	Results
S/(N+D)	1kHz,-2dB	20kHzLPF	82.8dB
DR	1kHz,-60dB	20kHzLPF	83.9dB
	1kHz,-60dB	22kHzLPF + A-weight	86.7dB
S/N	1kHz,0dB/GND IN	20kHzLPF	83.4dB
	1kHz,0dB/GND IN	22kHzLPF + A-weight	86.3dB



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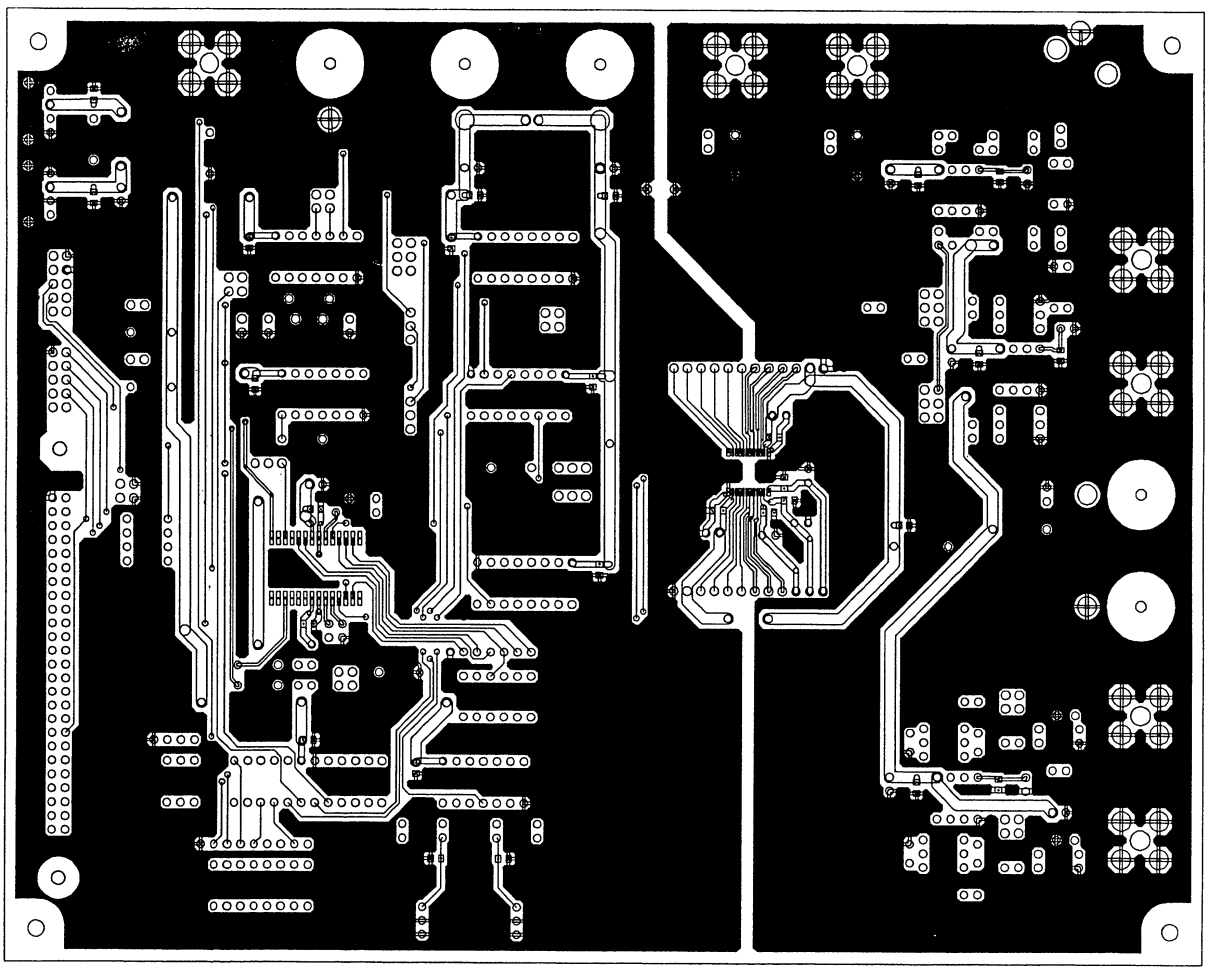

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