AKD4551
Evaluation board Rev.C for AK4551

GENERAL DESCRIPTION

AKD4551 is an evaluation board for the portable digital audio 20bit A/D and D/A converter, AK4551. The AKD4551 can evaluate A/D converter and D/A converter separately in addition to loopback mode (A/D → D/A). The A/D section can be evaluated by interfacing with AKM's DAC evaluation boards directly. The AKD4551 has the interface with AKM's wave generator using ROM data and AKM's ADC evaluation boards. Therefore, it's easy to evaluate the D/A section. The AKD4551 also has the digital audio interface and can achieve the interface with digital audio systems via opt-connector.

■ Ordering guide

AKD4551 --- Evaluation board for AK4551

FUNCTION

- **Compatible with 2 types of interface**
  - **Direct interface with AKM's A/D & D/A converter evaluation boards**
  - **DIT/DIR with optical input/output**
- **BNC connector for an external clock input**

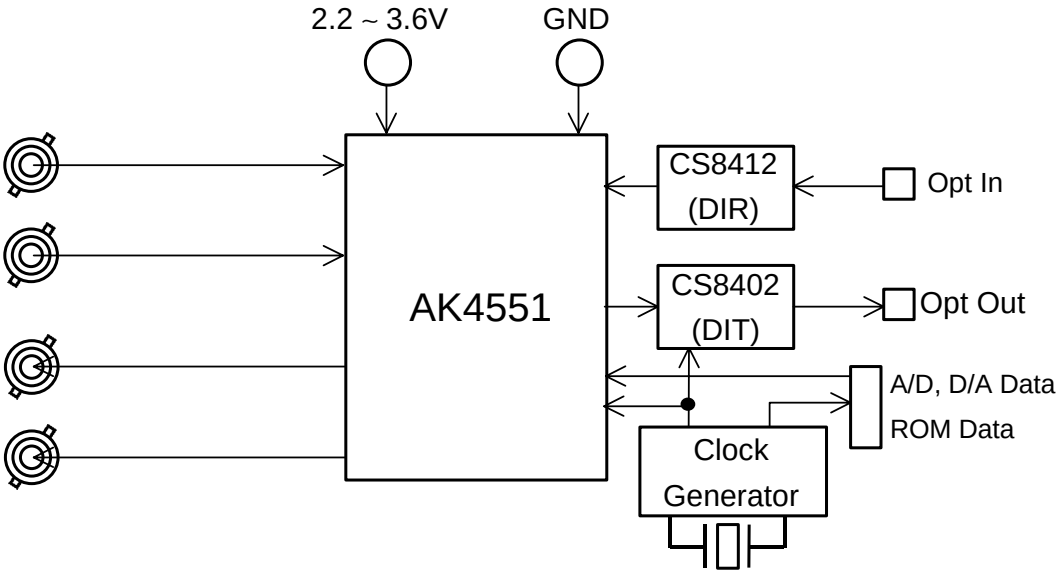


Figure 1. AKD4551 Block Diagram

* Circuit diagram is attached at the end of this manual.

■ Input Circuit

External analog signal fed through the BNC connector is terminated by a resistor of 560 ohms. The resistor value should be properly selected in order to meet the output impedance of the signal source.

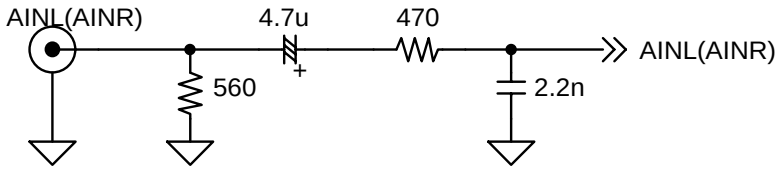


Figure 2. Input buffer circuit on board

* AKM assumes no responsibility for the trouble when using the circuit examples.

■ Analog Output Circuit

The AK4551 includes a combination of switched-capacitor filter (SCF) and continuous-time filter (CTF), so any external filters are not required.

■ Grounding and Power Supply Decoupling

To minimize the coupling by digital noise, VDD pin should be supplied from analog power supply in system. Decouling capacitors should be connected to AK4551 as near as possible. Especially, the capacitor between VDD and VSS pins should be connected nearest.

■ Operation sequence

1) Set up the power supply lines.

[VA] (orange)	= 2.2 ~ 3.6V	: for VDD of AK4551
[VP] (orange)	= 2.2 ~ 3.6V	: for VP of 74HC4050
[VD] (red)	= 3.6 ~ 5.0V	: for logic
[AGND] (black)	= 0V	: for analog ground (including VSS of AK4551)
[DGND] (black)	= 0V	: for logic ground

Each supply line should be distributed from the power supply unit.
VP and VA must be same voltage level.

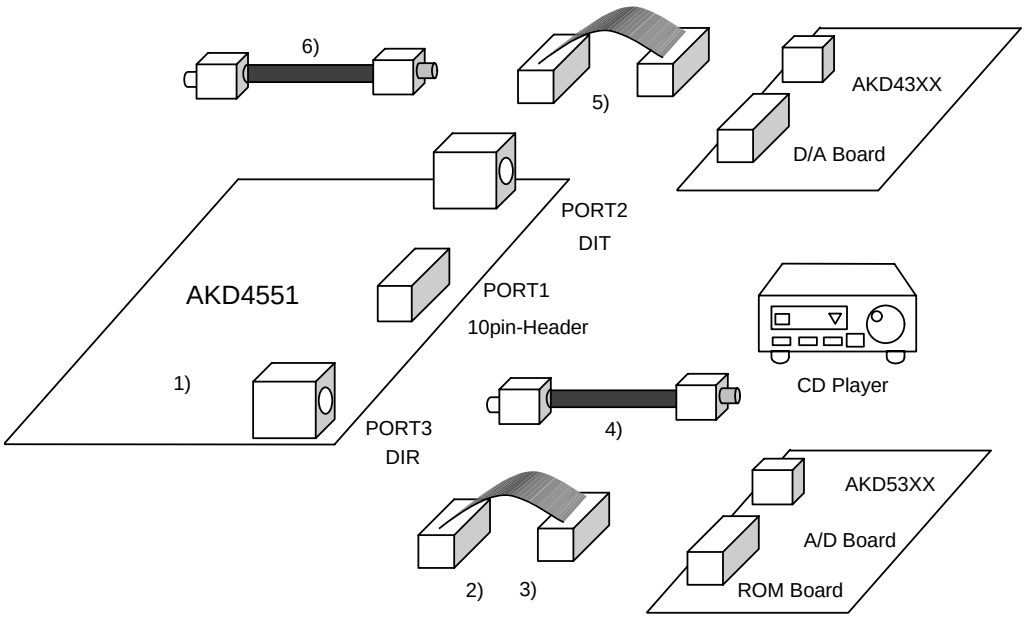
2) Set up the evaluation mode, jumper pins and DIP switches. (See the followings.)

3) Power on.
The AK4551 should be reset once bringing SW1,2 ($\overline{\text{PWAD}}$, $\overline{\text{PWDA}}$) “OFF” upon power-up.

■ Evaluation mode

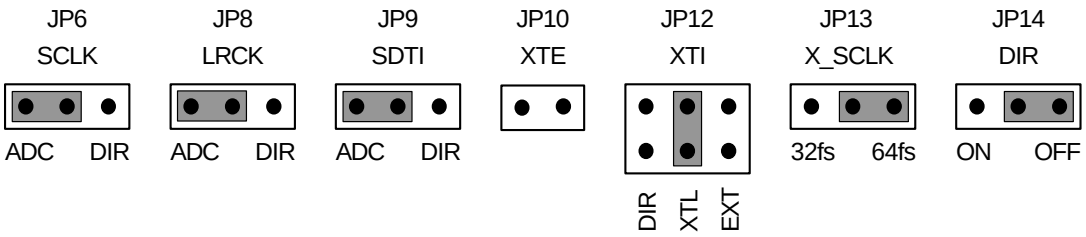
Applicable Evaluation Mode

1) Evaluation of loopback mode (default)
2) Evaluation of D/A using ideal sin wave generated by ROM data
3) Evaluation of D/A using A/D converted data
4) Evaluation of D/A using DIR (Optical Link)
5) Evaluation of A/D using D/A converted data
6) Evaluation of A/D using DIT (Optical Link)
7) All interface signals including master clock are fed externally.



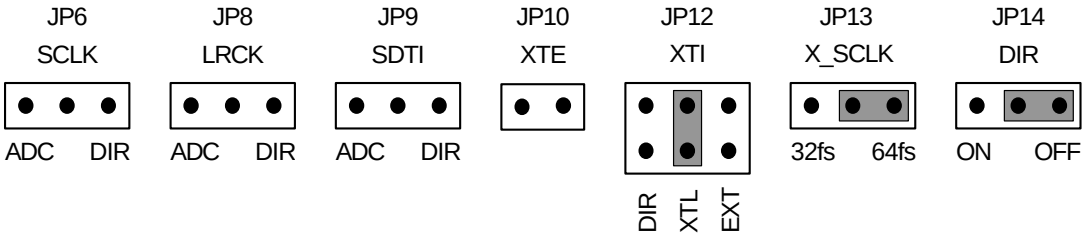
1) Evaluation of loopback mode. (default)

Nothing should be connected to PORT1/PORT3. In case of using external clock through a BNC connector (J5), select EXT on JP12 (XTI) and short JP10 (XTE).This mode corresponds to only JP13 (X_SCLK) 64fs.



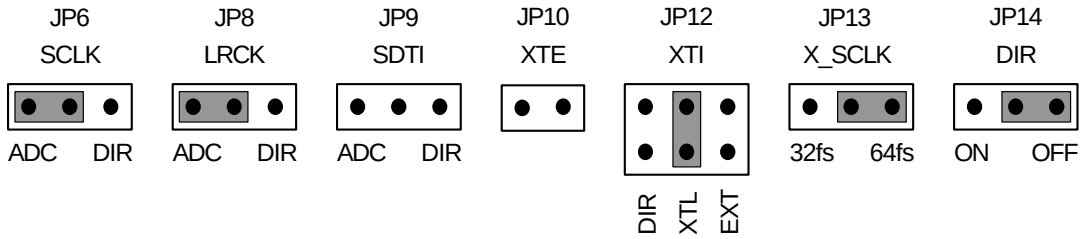
2) Evaluation of D/A using A/D converted data from ideal sine wave generated by ROM data.

Digital signals generated by AKD43XX are used. PORT1 is used for the interface with AKD43XX. Master clock is sent from AKD4551 to AKD43XX and SCLK, LRCK, SDTI are sent from AKD43XX to AKD4551. Nothing should be connected to PORT3. In case of using external clock through a BNC connector (J5), select EXT on JP12 (XTI) and short JP10 (XTE).



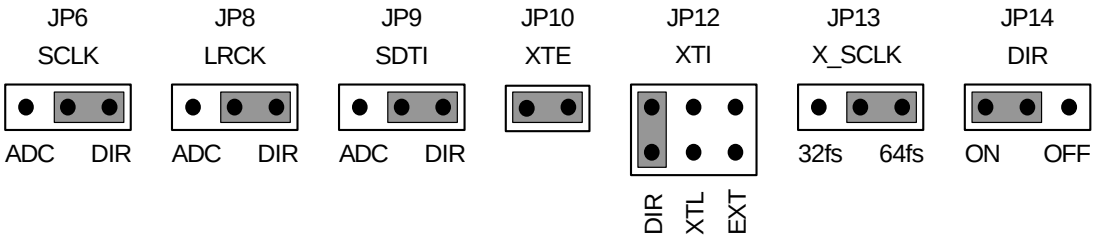
3) Evaluation of D/A using A/D converted data.

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's A/D evaluation boards with PORT1. Nothing should be connected to PORT3. In case of using external clock through a BNC connector (J5), select EXT on JP12 (XTI) and short JP10 (XTE).



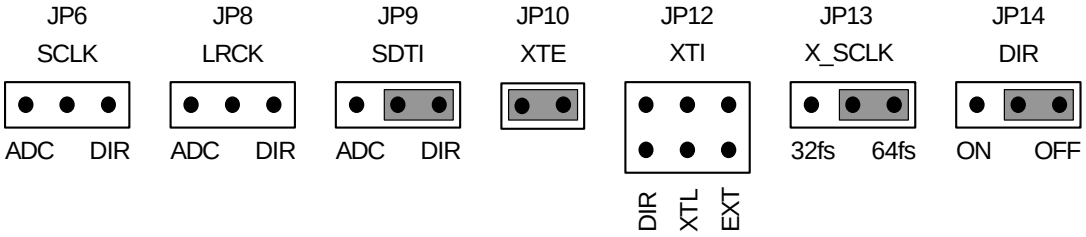
4) Evaluation of D/A using DIR. (Optical link)

PORT3 (TORX176) is used. DIR generates MCLK, SCLK, LRCK and SDATA from the received data through optical connector (TORX176). Used for the evaluation using CD test disk. Nothing should be connected to PORT1/PORT2.



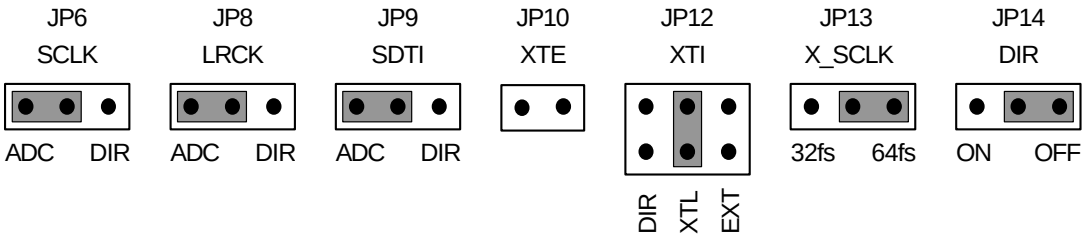
5) Evaluation of A/D using D/A converted data.

It is possible to make evaluation in the form of analog inputs and analog outputs by interfacing with various AKM's D/A evaluation boards with PORT1. Nothing should be connected to PORT3.



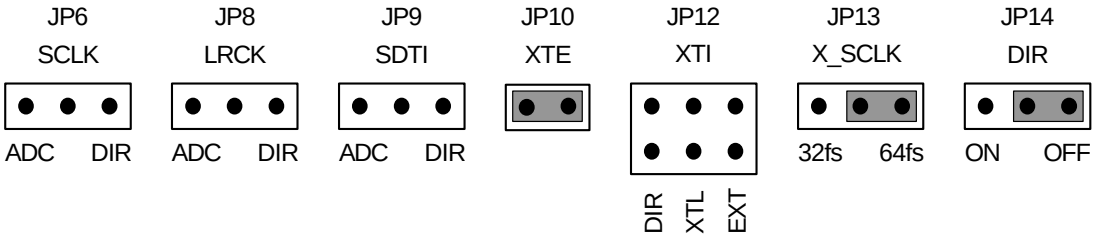
6) Evaluation of A/D using DIT. (Optical link)

PORT2 (TOTX176) is used. DIT generates audio bi-phase signal from received data and which is output through optical connector (TOTX176). It is possible to connect AKM's D/A converter evaluation boards on the digital-amplifier which equips DIR input. In case of using external clock through a BNC connector (J5), select EXT on JP12 (XTI) and short JP10 (XTE).



7) All interfacing signals (MCLK, SCLK, LRCK) are fed from the external circuit through PORT1.

Under the following set-up, all external signals needed for the AK4551 to operate could be fed through PORT1. In case of interfacing external sources to D/A converter, JP9 (SDTI) should be open. And in case of using A/D data to externally, JP9 (SDTI) is set ADC side. When JP9 (SDTI) is open, the A/D data can be output from the SDTO pin of PORT1 at the same time if JP7 (SDTO) is short.



■ DIP switch set up

Upper-side is “ON” (“H”) and lower-side is “OFF” (“L”).

[SW3]: Sets the C-bit of CS8402. (Default is the consumer mode.)
This set up does not affect the evaluation of the AK4551. In case of using DIT, need to set it up correctly. For more detailed configurations, please refer to the CS8402 data sheet.

Switch	OFF=0, ON=1	Contents
8	$\overline{\text{PRO}}$ = 0	Professional mode, C0=1
7, 6	$\overline{\text{C6}}$, $\overline{\text{C7}}$	C6,C7 – Sampling frequency
	11	00 – Not indicated. Receiver default to 48kHz.
	10	01 – 48kHz
	01	10 – 44.1kHz
	00	11 – 32kHz
5	$\overline{\text{C9}}$	C8,C9,C10,C11 – 1bit of channel mode
	1	0000 – Mode not indicated. Receiver default to 2-channel mode.
	0	0100 – Stereophonic.
4	$\overline{\text{C1}}$	C1 – Audio mode
	1	0 – Normal audio
	0	1 – Non-audio
3	TRNPT	Transparent mode *CS8402 is CRE
	0	Normal mode
	1	Transparent mode
2, 1	EM1, EM0	C2,C3,C4 – Encoded audio signal emphasis
	11	000 – Emphasis not indicated. Receiver defaults to no emphasis with manual override enabled.
	10	100 – None
	01	110 – 50/15usec
	00	111 – CCITT J.17

Table 1. DIP switch set-up of CS8402 (Professional mode)

Switch	OFF=0, ON=1	Contents
8	$\overline{\text{PRO}}$ = 1	Consumer mode, C0=1 <Default>
7	$\overline{\text{C2}}$	C2 – Copy
	1	0 – Copy inhibited
Default	0	1 – Copy permitted
6	$\overline{\text{C3}}$	C3,C4,C5 – Pre-emphasis
Default	1	000 – None
	0	100 – 50/15usec
5	$\overline{\text{C15}}$	C15 – General Status
	1	0 – See the standard
Default	0	1 – See the standard
4, 3	FC1,FC0	C24,C25,C26,C27 – Sampling frequency
	00	0000 – 44.1kHz
	01	0100 – 48kHz
Default	10	1100 – 32kHz
	11	0000 – 44.1kHz, CD mode
2, 1	$\overline{\text{C8}}$, $\overline{\text{C9}}$	C8-C14 – Category code
Default	11	0000000 – General
	10	0100000 – PCM encoder/decoder
	01	1000000 – CD
	00	1100000 – DAT

Table 2. DIP switch set-up of CS8402 (Consumer mode; default)

■ Other jumper pins set up

[JP1] (GND): Analog ground and digital ground
open: separated <default>
AGND and DGND are connected near to AK4551 on the board.

[JP2] (VP-VD): VP and VD
open: separated <default>
short: common (The connector "VP" can be open.)

[JP3, 4] (DEM0, DEM1): Set up the de-emphasis of AK4551

DEM1 (JP3)	DEM0 (JP4)	Mode
open	open	44.1kHz
open	short	OFF
short	open	48kHz
short	short	32kHz

Table 3. Set up the de-emphasis of AK4551

[JP5] (SCLK2): Phase of SCLK
THR: SCLK is coincides with AK4551. <default>
INV: SCLK is inverted.

[JP7] (SDTO): SDTO of AK4551
Always open. It is possible to short for evaluation mode 7.

[JP11] (SPEED): Select of MCLK
NORMAL: 256fs <default>
DOUBLE: 512fs

■ The function of the toggle SW.

Upper-side is "ON" and lower-side is "OFF".

[SW1] ($\overline{\text{PWDA}}$): Resets the D/A of AK4551. Keep "ON" during normal operation.
[SW2] ($\overline{\text{PWAD}}$): Resets the A/D of AK4551. Keep "ON" during normal operation.
[SW4] (DIT_RST): Resets the CS8402. "OFF" resets the internal counter of CS8402, then Bi-phase signal is not output. Keep "ON" during normal operation.

■ Indication for LED

[LED1]: Indicate whether the input data of CS8412 is pre-emphasized or not.
[LED2] (VERF): Monitor VERF pin of the CS8412. LED turns on when some error has occurred to CS8412.

MEASUREMENT RESULTS

[Measurement condition]

- Measurement unit : Audio Precision, System two
- MCLK : 256fs
- SCLK : 64fs (ADC, DAC)
- fs : 32kHz, 44.1kHz, 48kHz
- Bit : 20bit
- Power Supply : VDD = VP = 2.5V, VD = 4.0V
- Interface : DIT/DIR
- Temperature : Room

1. ADC

VDD	Parameter	Measured Filter	fs = 32kHz	fs = 44.1kHz	fs = 48kHz
2.5V	S/(N+D) (-0.5dBFS)	20kHz LPF	84.3 dB	79.5 dB	79.5 dB
	D-Range (-60dBFS)	20kLPF + A-weighted	88.5 dB	89.3 dB	89.4 dB
	S/N (0 data)	20kLPF + A-weighted	88.5 dB	89.3 dB	89.4 dB

2. DAC

VDD	Parameter	Measured Filter	fs = 32kHz	fs = 44.1kHz	fs = 48kHz
2.5V	S/(N+D) (0dBFS)	20kHz LPF	88.6 dB	87.9 dB	87.5 dB
	D-Range (-60dBFS)	22kLPF + A-weighted	92.5 dB	92.8 dB	92.9 dB
	S/N (0 data)	22kLPF + A-weighted	92.5 dB	93.0 dB	93.0 dB

3. Graph

(1) ADC

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AK4551 ADC THD+N vs. Input Level
VDD=2.5V, fs=44.1kHz, fin=1kHz

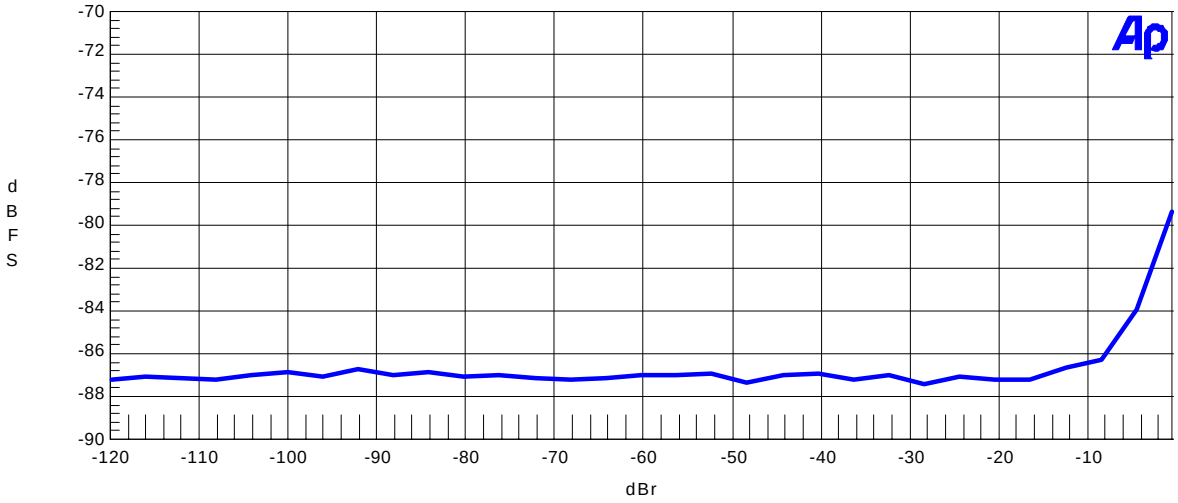

Fig 1. THD+N vs. Input Level

AKM

AK4551 ADC THD+N vs. Input Frequency
VDD=2.5V, fs=44.1kHz, Input=-0.5dBr

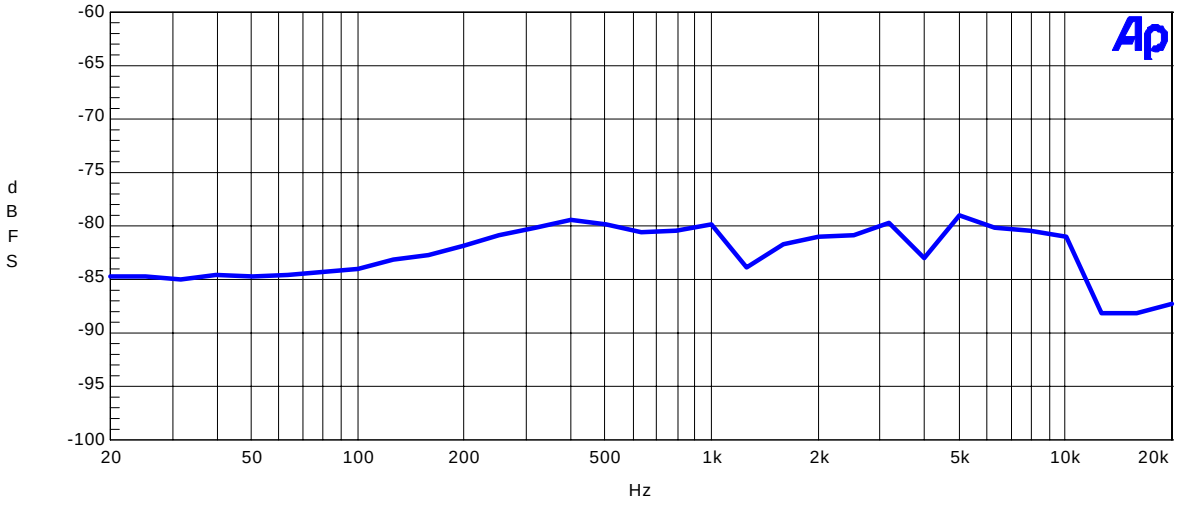

Fig 2. THD+N vs. Input Frequency

AKM

AK4551 ADC Linearity
VDD=2.5V, fs=44.1kHz, fin=1kHz

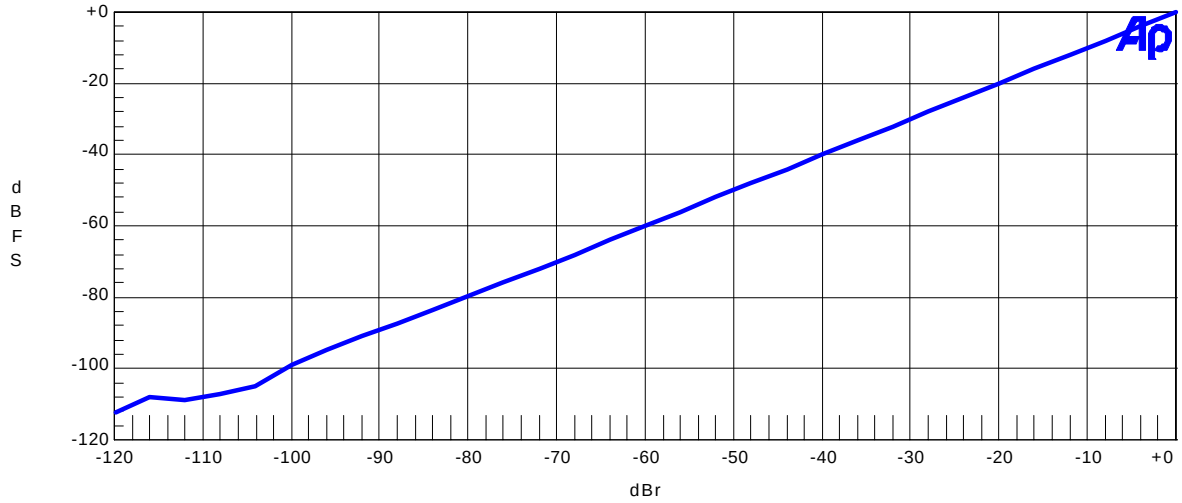

Fig 3. Linearity

AKM

AK4551 ADC Frequency Response
VDD=2.5V, fs=44.1kHz, Input=-0.5dBr

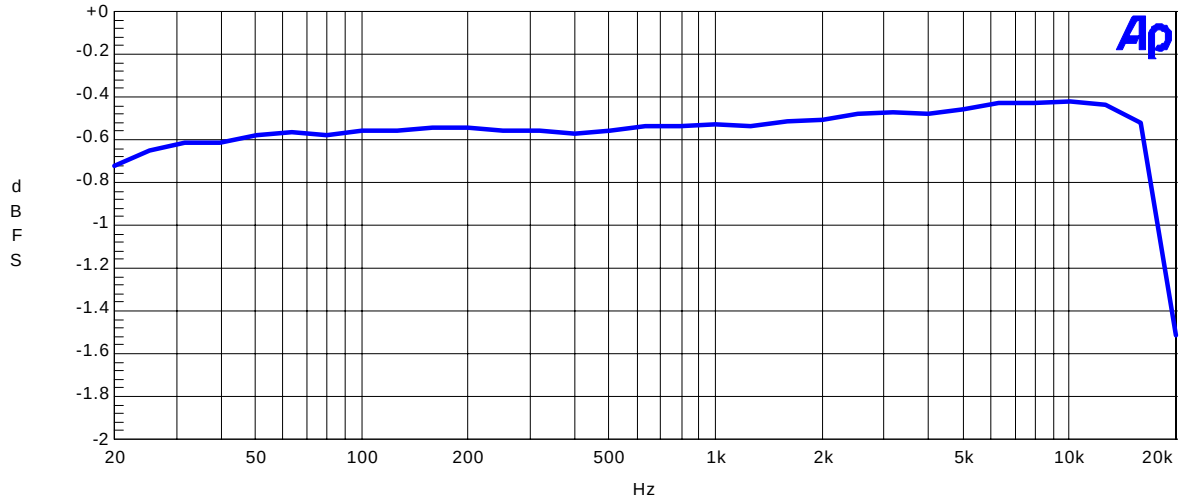

Fig 4. Frequency Response

AKM

AK4551 ADC Crosstalk
VDD=2.5V, fs=44.1kHz, Input=-0.5dBr

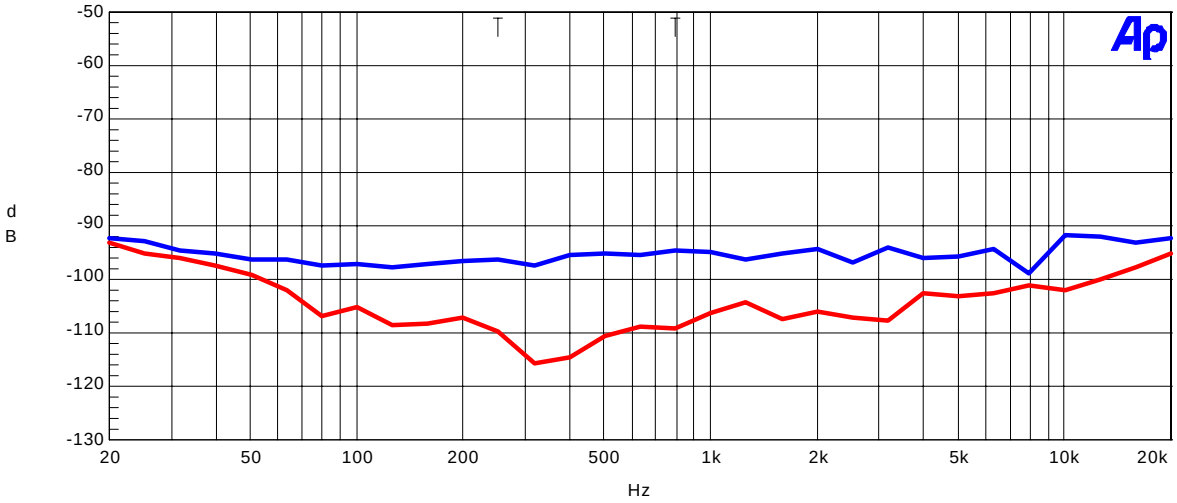

Fig 5. Crosstalk

AKM

AK4551 ADC FFT Plot
VDD=2.5V, fs=44.1kHz, fin=1kHz, Input=-0.5dBr

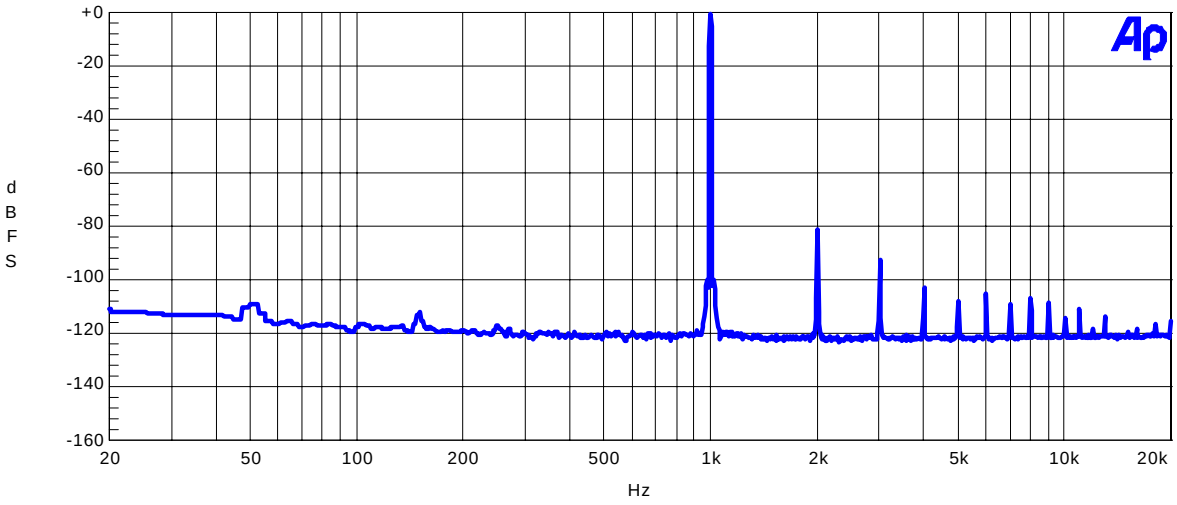

Fig 6. FFT Plot

AKM

AK4551 ADC FFT Plot
VDD=2.5V, fs=44.1kHz, fin=1kHz, Input=-60dBr

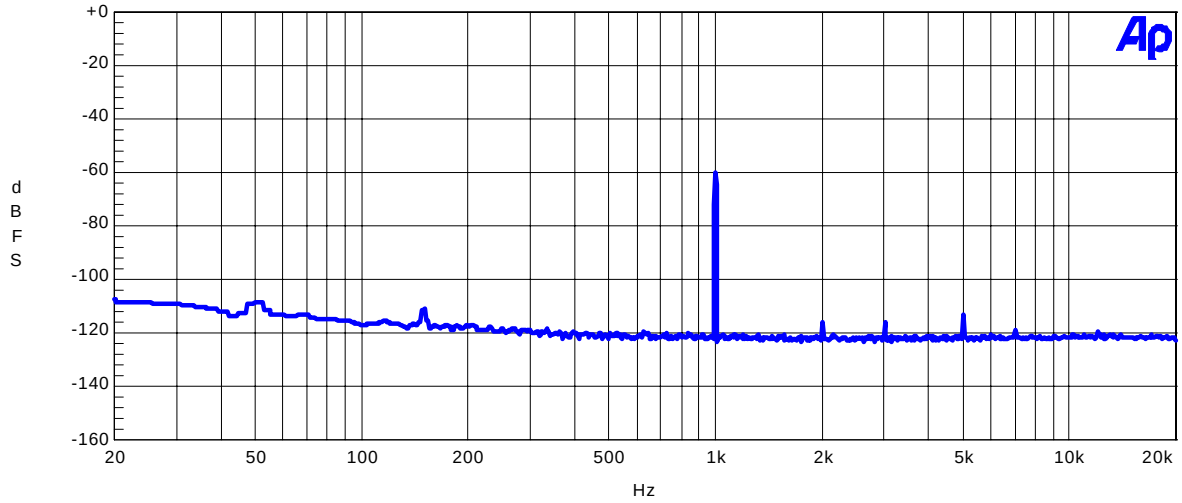

Fig 7. FFT Plot

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AK4551 ADC FFT Plot
VDD=2.5V, fs=44.1kHz, fin=None

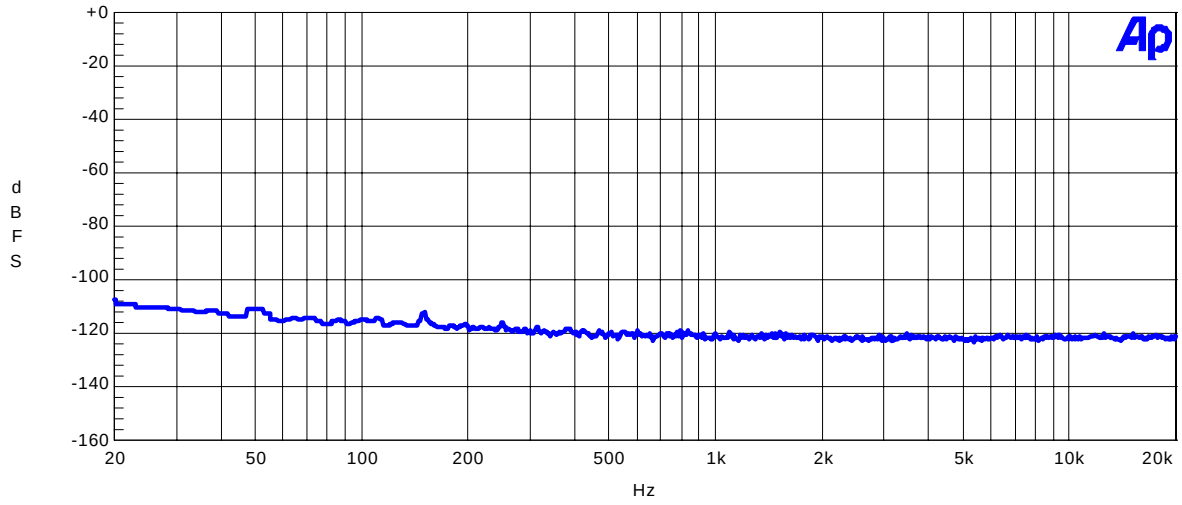

Fig 8. FFT Plot

(2) DAC

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AK4551 DAC THD+N vs. Input Level
VDD=2.5V, fs=44.1kHz, fin=1kHz

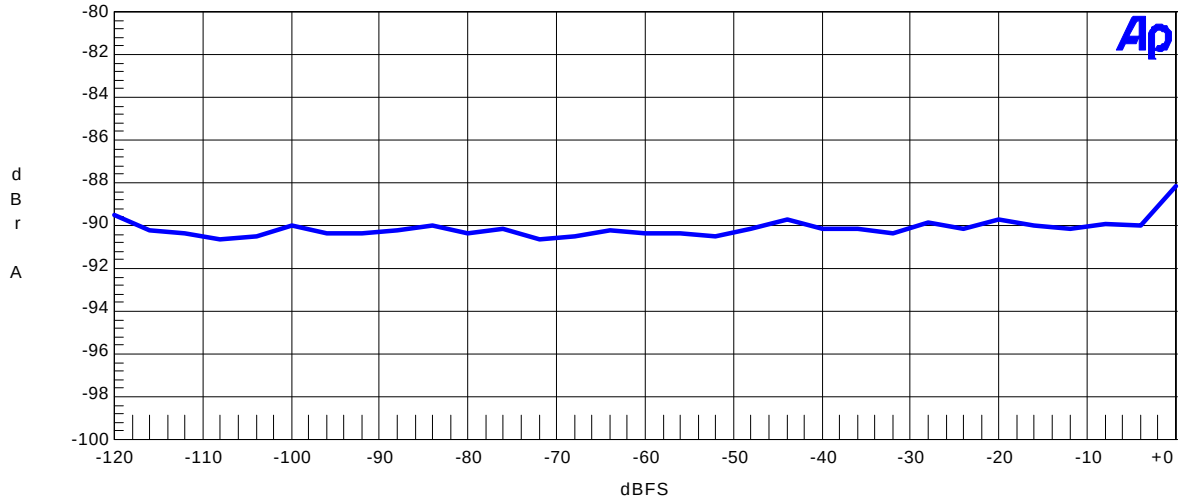

Fig 1. THD+N vs. Input Level

AKM

AK4551 DAC THD+N vs. Input Frequency
VDD=2.5V, fs=44.1kHz, Input=0dBFS

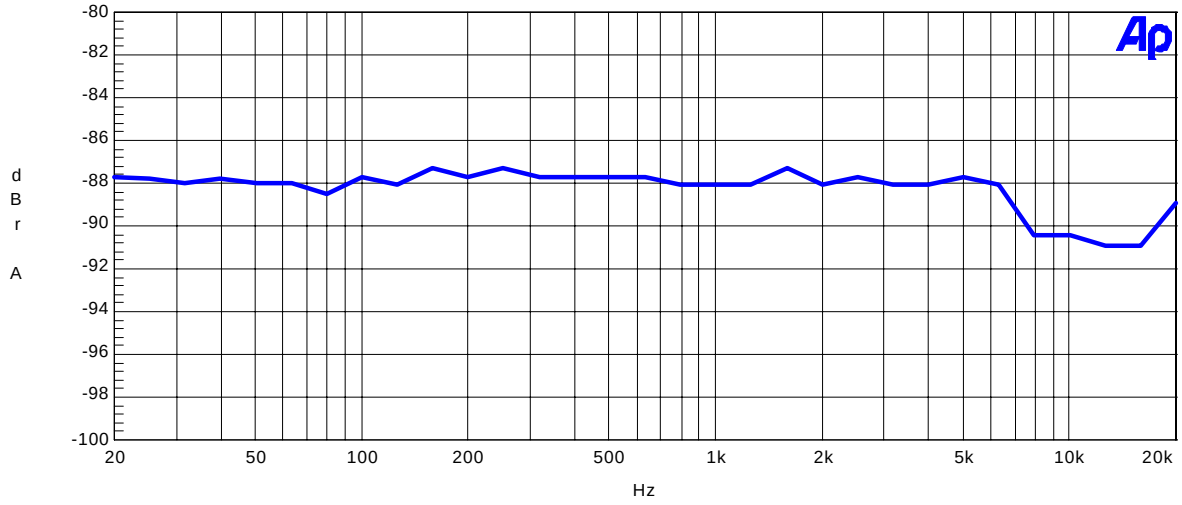

Fig 2. THD+N vs. Input Frequency

AKM

AK4551 DAC Linearity
VDD=2.5V, fs=44.1kHz, fin=1kHz

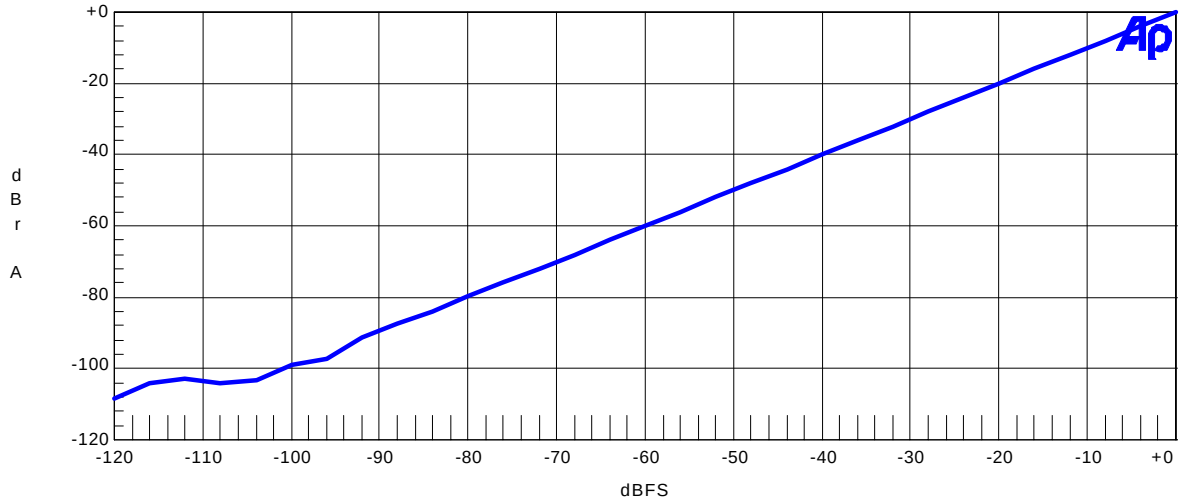

Fig 3. Linearity

AKM

AK4551 DAC Frequency Response
VDD=2.5V, fs=44.1kHz, Input=0dBFS

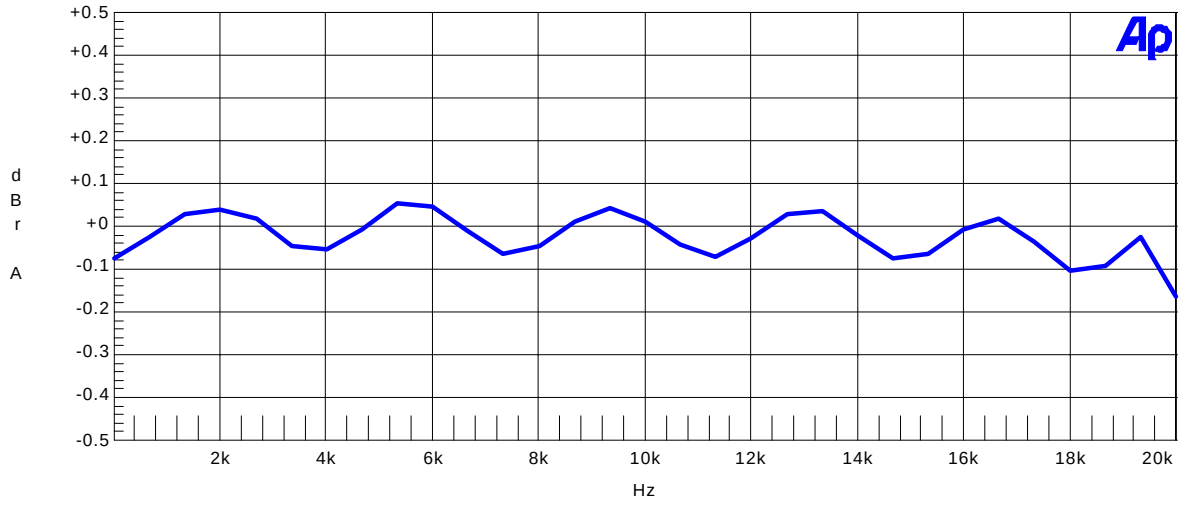

Fig 4. Frequency Response

AKM

AK4551 DAC Crosstalk
VDD=2.5V, fs=44.1kHz, Input=0dBFS

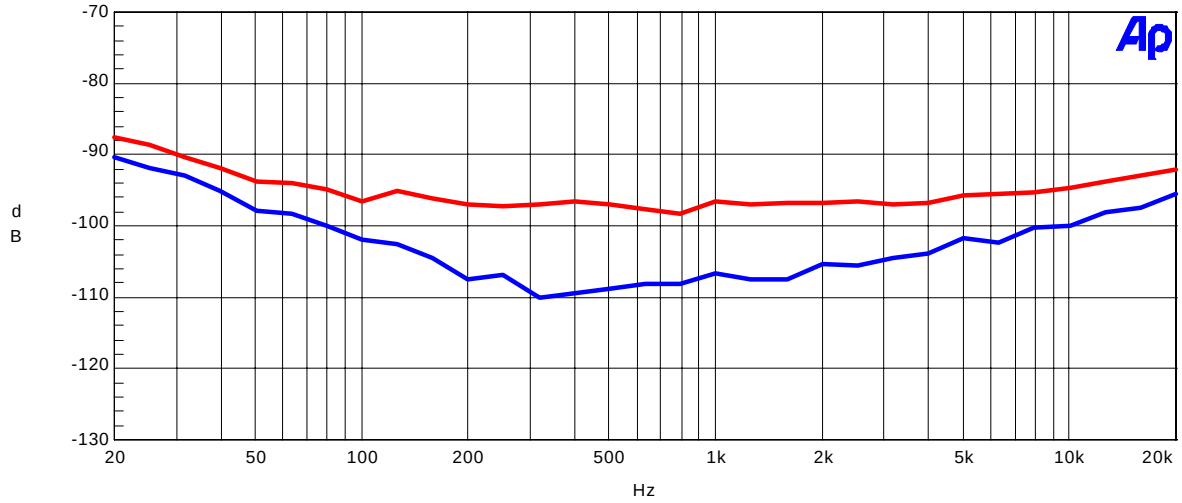

Fig 5. Crosstalk

AKM

AK4551 DAC FFT Plot
VDD=2.5V, fs=44.1kHz, fin=1kHz, Input=0dBFS

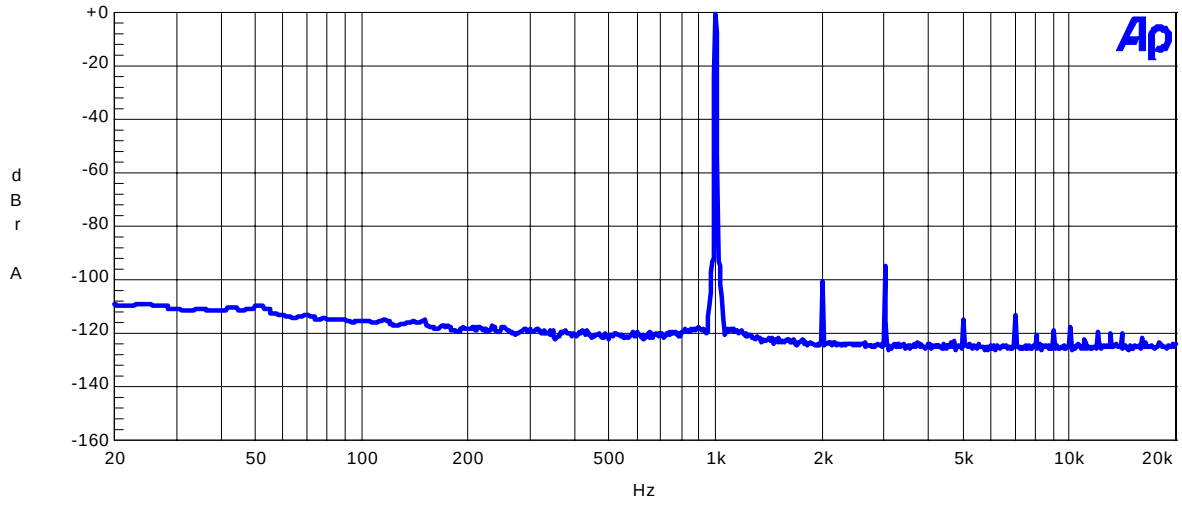

Fig 6. FFT Plot

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AK4551 DAC FFT Plot
VDD=2.5V, fs=44.1kHz, fin=1kHz, Input=-60dBFS

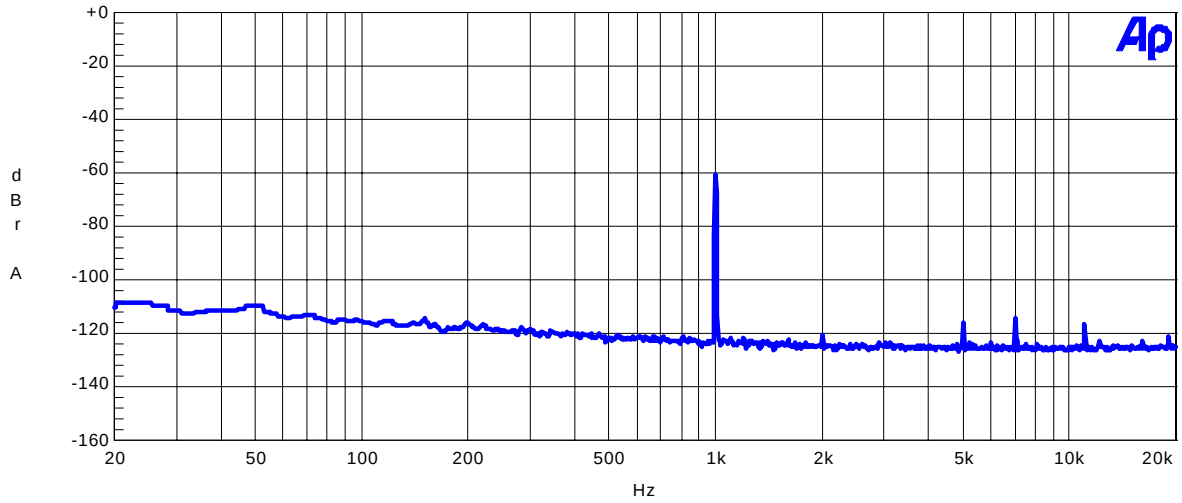

Fig 7. FFT Plot

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AK4551 DAC FFT Plot
VDD=2.5V, fs=44.1kHz, fin=None

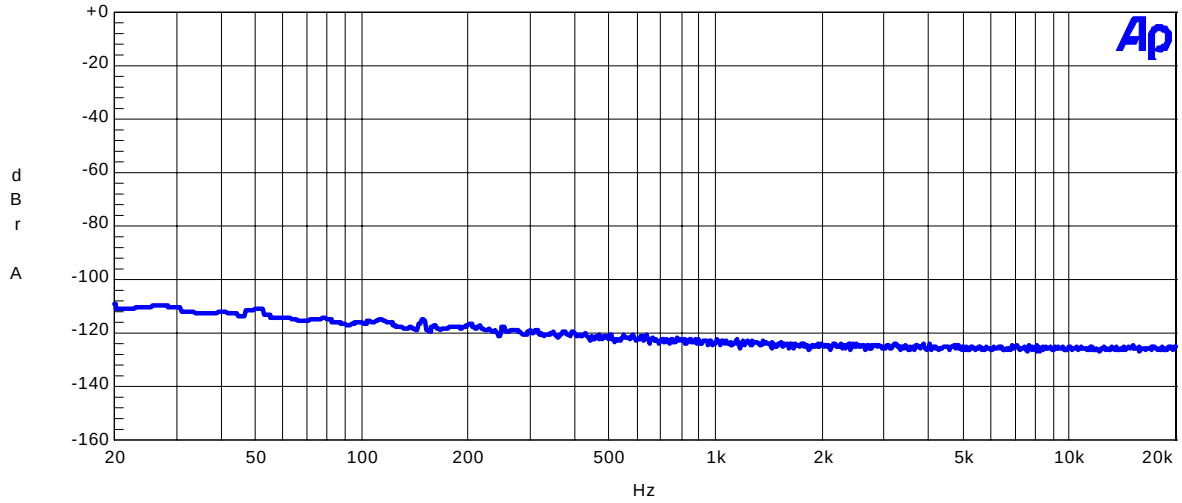

Fig 8. FFT Plot

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