AKD5392

Evaluation Board Rev.B for AK5392

General description

The AKD5392 is an evaluation board for the AK5392 professional audio 24bit A/D converter. The AKD5392 includes the input buffer circuit and also has a digital interface transmitter. Further, the AKD5392 can evaluate direct interface with AKD4324, AKD4321, AKD4320 and AKD4319.

■ Ordering guide

AKD5392 --- Evaluation board for AK5392

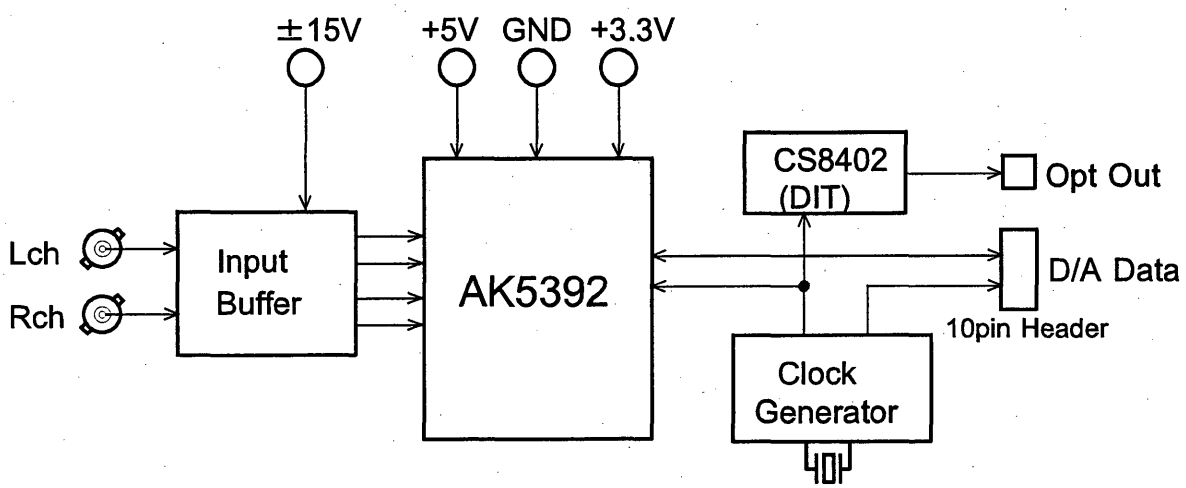
Function

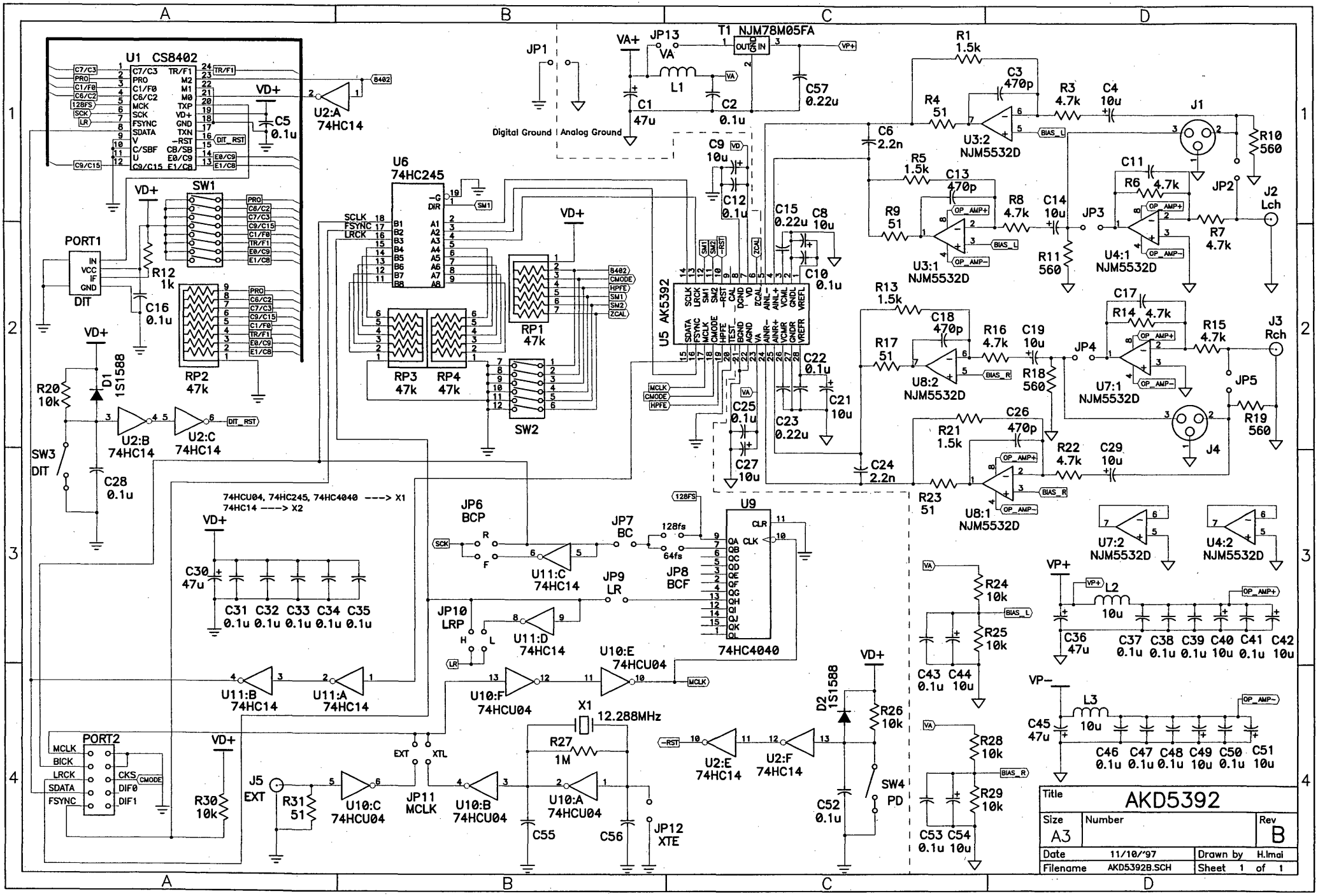
☐ On-board Full-differential input buffer circuit

☐ On-board clock generator

☐ Compatible with 2 types of interface
1) Direct interface with AKD4324, AKD4321, AKD4320 and AKD4319.
2) On-board CS8402 as DIT which transmits optical output.

☐ A BNC connector for an external clock input.




U1 CS8402
U2:A 74HC14
U2:B 74HC14
U2:C 74HC14
U2:D 74HC14
U2:E 74HC14
U2:F 74HC14
U3:1 NJM5532D
U3:2 NJM5532D
U4:1 NJM5532D
U4:2 NJM5532D
U5 AK5392
U6 74HC245
U7:1 NJM5532D
U7:2 NJM5532D
U8:1 NJM5532D
U8:2 NJM5532D
U9 74HC4040
U10:A 74HCU04
U10:B 74HCU04
U10:C 74HCU04
U10:D 74HCU04
U10:E 74HCU04
U10:F 74HCU04
U11:A 74HC14
U11:B 74HC14
U11:C 74HC14
U11:D 74HC14
T1 NJM78M05FA
SW1
SW2
SW3 DIT
SW4 PD
PORT1
PORT2
DIT
D1 1S1588
D2 1S1588
JP1
JP2
JP3
JP4
JP5
JP6 BCP
JP7 BC
JP8 BCF
JP9 LR
JP10 LRP
JP11 MCLK
JP12 XTE
J1
J2 Lch
J3 Rch
J4
J5 EXT
X1 12.288MHz
Digital Ground
Analog Ground
74HCU04, 74HC245, 74HC4040 ---> X1
74HC14 ---> X2
Title AKD5392
Size A3
Number
Rev B
Date 11/10/'97
Drawn by H.Imai
Filename AKD5392B.SCH
Sheet 1 of 1

■ Input buffer circuit

The AKD5392 includes full-differential input buffer circuit with an inverted-amp (gain:-9.9dB) . The capacitor (Cin) of 2200pF in the circuit decreases the clock feed through noise of modulator. And the resistor of 51 ohms is inserted in order to stabilize the op-amps before the AK5392. Figure 1. is a low pass filter with cut-off frequency of about 220kHz. External analog signal can be fed through the BNC connector or the Cannon connector.

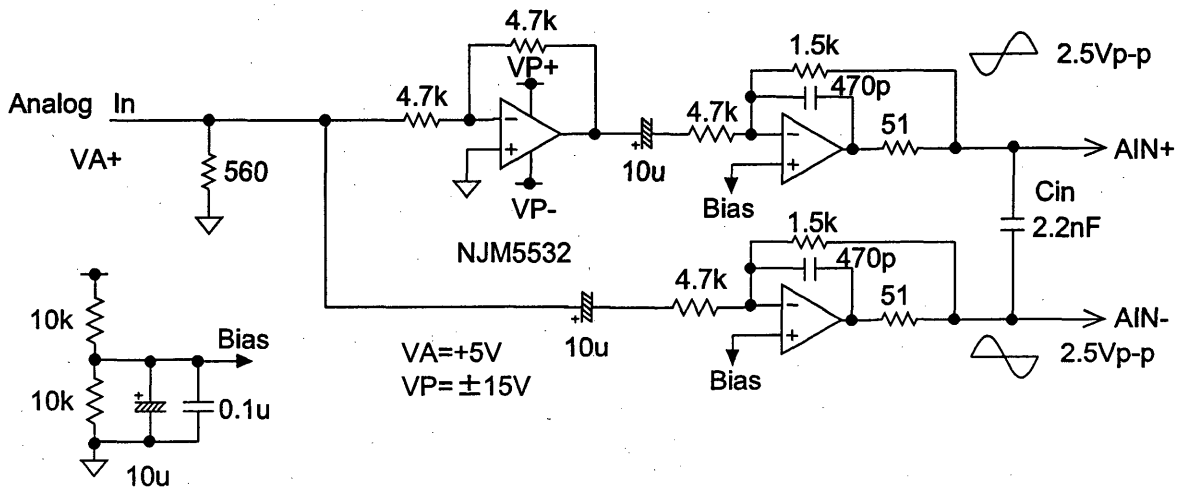


Figure 1. Full-differential input buffer circuit example

1: In case of using the BNC connector

[JP2,JP3,JP4,JP5] : Short
[R11,R18] : Open
The resistor value of R10 and R19 should be properly selected in order to much the output impedance of the signal source.

2: In case of using the Cannon connector

[JP2,JP3,JP4,JP5] : Open
The resistor value of R10, R11, R18 and R19 should be properly selected in order to much the output impedance of the signal source.

* AKM assumes no responsibility for the trouble when using the above circuit examples.

■ Power supply and Decoupling

VA and VD supplies to the AK5392 are decoupled separately in order to minimize the effect of the digital noise. A system analog supply is fed to VA. VA and VD lines should be distributed separately from the power unit.
Decoupling capacitors are connected to AK5392 as near as possible, particularly the ceramic capacitor to the VREFL/R pin.

■ Operation sequence

① Set up the power supply lines
VP+=+15V, VP- = -15V, VA+=+5V, VD+=+3.3V ~ 5.25V, AGND=DGND=0V
Each supply line should be distributed from the power unit.

② Set up the evaluation modes and jumper pins. (See next item)
There are many jumper pins to cover many evaluation modes.
Please take care of setting.

③ Set up the DIP SW position for the DIT. (See next item)
This does not affect AK5392 operation.

④ Power On.
The AK5392 should be reset once by bringing $\overline{PD}$ "L" (SW4) upon power-up.

⑤ AK5392 can be reset by SW4 during operation.
Lower position resets the device, and the upper position is for normal operation.

Note: In any case of changing clocks during operation, the device should be reset by bringing $\overline{PD}$ "L". If not followed, the AK5392 may be destroyed since its internal logic uses dynamic circuit.

■ The evaluation modes and corresponding jumper pin settings.

1. Evaluation Mode

Applicable Evaluation Mode

① Using D/A converter board for the analog performance analysis.
② DIT (Optical Link) [Default]
③ All interface signals (MCLK, BICK and LRCK) are fed from external circuit.
④ Feed all interface signals to the external circuit through PORT2.

① Using D/A converter board for the analog performance analysis.

The AK5392 can be evaluated by distortion analyzer using various AKM's D/A converter AKD4303, AKD4328, AKD4310, AKD4311, AKD4319 and AKD4320 through PORT2.
When SW2-2 (CMODE) goes "OFF", AK5392 operates with 384fs clock. [Slave mode]

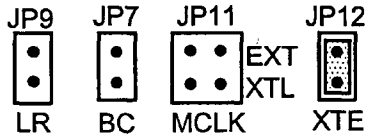
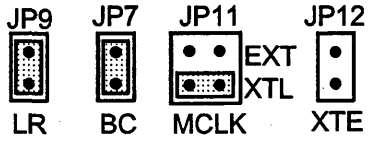


Figure 2. Jumper Set up (D/A)

② DIT (Optical Link)

PORT1 is used. DIT generates audio Bi-phase signal from received data and which is output through optical connector (TOTX174). It is possible to connect AKM's evaluation boards (AKD4328, AKD4311, AKD4310, AKD4320 and AKD4319) on the digital-amplifier which equips DIR input. There are two kinds of jumper setting depend on the SMODE1 and SMODE2 pin. The interface signals are output from PORT2. (See the ④). In case of using external clock through a BNC connector, select EXT on JP11 (MCLK) and shorts JP12 (XTE).

[Slave mode] (Default)



[Master mode]

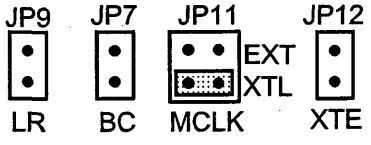


Figure 3. Jumper Set up (DIT)

③ All interface signals (MCLK, BICK and LRCK) are fed from external circuit.

[Slave mode]

Under the following set-up, MCLK, LRCK and SCLK signals needed for the A/D to operate could be fed through PORT2.
When SW2-2 (CMODE) goes "OFF", the AK5392 operates with 384fs clock.

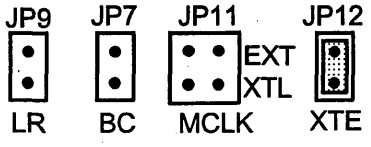


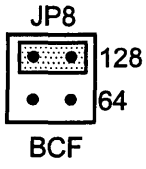
Figure 4. Jumper Set up (EXT)

④ Feed all interface signals to the external circuit through PORT2.

[Master, Slave mode]

Please set up as same as ②. All interfacing signal which drive AK5392 are output through PORT2. However, the FSYNC signal is input when the position of the SDATA is needed to be controlled.

2. BIT CLK(BCF) set up



[JP8] Either 64fs or 128fs for the BCF can be selected. Figure shows 128fs example.

128: 128fs, 64: 64fs

3. Jumper-set up and explanation

Set up the CS8402's data format corresponding the serial data interface of the AK5392.

AK5392 Data Format	SMODE2 (SW2-5)	SMODE1 (SW2-4)	8402 (SW2-1)	BCF (JP6)	LRP (JP10)
Slave mode	ON	ON	ON	F	H
Master mode	ON	OFF	OFF	R	L
I ^{2} S Slave mode	OFF	ON	OFF	R	H
I ^{2} S Master mode	OFF	OFF	OFF	R	H

Table 1. Serial data interface of AK5392 and CS8402

*** DIP-SW is ON="L" OFF="H".**

[SW2-1]: CS8402's data format
ON: MSB justified, 24bit
OFF:I ^{2} S Compatible

[JP6]: Define the polarity of SCLK.
F:SCLK is inverted.
R:SCLK coincides with AK5392

[JP10]: Define the polarity of LRCK.
L:LRCK is inverted.
H:LRCK coincides with AK5392.

4. The other function set up

No.	PIN	ON	OFF
1	8402	See the Table 1.	
2	CMODE	256 fs	384 fs
3	HPFE	disable	enable
4	SM1	See the Table 1.	
5	SM2		
6	CALMODE	VCOM	AIN

Table 2. DIP-SW2 set-up

*** DIP-SW is ON="L", OFF="H".**

→ Selects the master clock frequency of AK5392

→ Selects HPF of AK5392.

→ Selects the reference signal for Offset-Cal of AK5392
VCOM:VCOML,VCOMR pin
AIN: Analog input pin (AINL ±,AINR ±)

[JP13] Selects the analog power supply source to VA pin of the AK5392.
Open: Supply from the power supply terminal(VA+).
Short: Supply from 3-terminal voltage regulator(+5V) on the board.

■ The function of the toggle SW.

[SW3] Resets the CS8402. Upper position resets the internal counter of CS8402, then Bi-phase signal is not output. Keep the "L" position during normal operation.

[SW4] Resets the AK5392. Keep the "H" position during conversion.

■ DIP switch set up. (Default is the consumer mode.)

The DIP-SW1 sets the C-bit of CS8402. This set up does not affect the evaluation of the AK5392. In case of using DIT, need to set it up correctly. For more detailed configurations, please refer to the CS8402 data-sheet.

Switch	OFF=0,ON=1	Contents
8	$\overline{PRO}$=0	Professional mode, C0=1
7,6	$\overline{C6}$,$\overline{C7}$	C6,C7 - Sampling frequency
	1 1	00 - Not indicated. Receiver default to 48kHz.
	1 0	01 - 48kHz
	0 1	10 - 44.1kHz
	0 0	11 - 32kHz
5	$\overline{C9}$	C8,C9,C10,C11 - 1bit of channel mode
	1	0000 - Mode not indicated. Receiver default to 2-channel mode.
	0	0100 - Stereophonic.
4	$\overline{C1}$	C1 - Audio mode
	1	0 - Normal audio
	0	1 - Not audio
3	TRNPT	Transparent mode *CS8402 is CRE
	0	Normal mode
	1	Transparent mode
1,2	EM1,EM0	C2,C3,C4 - Encoded audio signal emphasis
	1 1	000 - Emphasis not indicated. Receiver defaults to no emphasis with manual override enable.
	1 0	100 - None
	0 1	110 - 50/15usec
	0 0	111 - CCITT J.17

Table 3. DIP switch set up of CS8402 (Professional mode)

Switch	OFF=0,ON=1	Contents
8	$\overline{PRO}$=1	Consumer mode, C0=0 (Default)
7	$\overline{C2}$	C2 - Copy
	1	0 - Copy inhibited
Default	0	1 - Copy permitted
6	$\overline{C3}$	C3,C4,C5 - Pre-emphasis
Default	1	000 - None
	0	100 - 50/15usec
5	$\overline{C15}$	C15 - Generation Status
	1	0 - See the standard
Default	0	1 - See the standard
3,4	FC1,FC0	C24,C25,C26,C27- Sampling frequency
	0 0	0000 - 44.1kHz
Default	0 1	0100 - 48kHz
	1 0	1100 - 32kHz
	1 1	0000 - 44.1kHz, CD mode
1,2	$\overline{C8}$,$\overline{C9}$	C8-C14 - Category code
Default	1 1	0000000 - General
	1 0	0100000 - PCM encoder/decoder
	0 1	1000000 - CD
	0 0	1100000 - DAT

Table 4. DIP switch set up of CS8402 (Consumer mode)

AK5392 Measurement Examples

[Measurement condition]

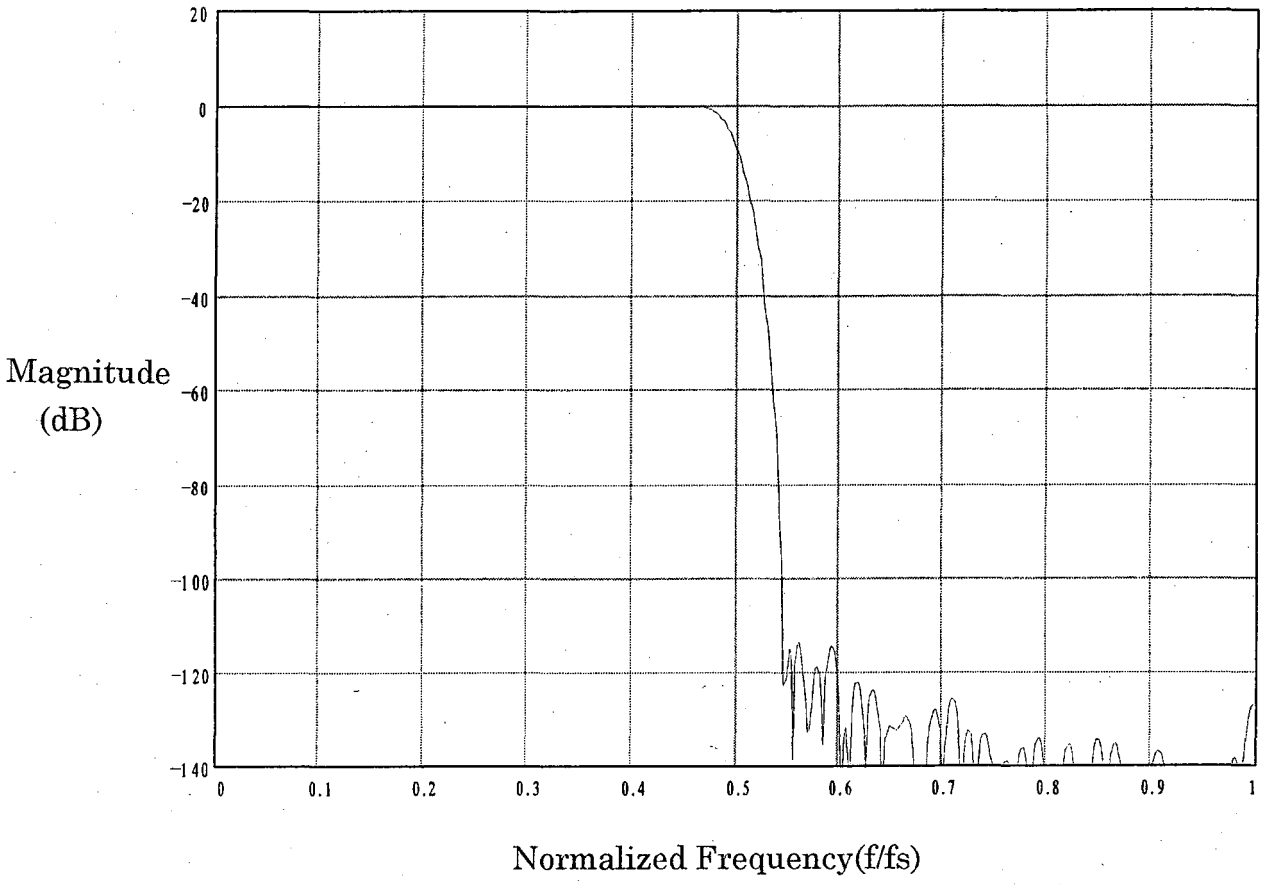
- AKD5392 Rev.B is used.
- Measurement Unit: ROHDE&SCHWARZ UPD04
- Power Supply: VA=5V, VD=3.3V
- Interface: DIT
- SCLK:128fs
- MCLK: 256fs, Slave mode
- fs: 48kHz
- Temperature: Room temperature
- Bit: 24bit

[Measurement Result]

Parameter	Input signal	Result	Band width
THD+N	1kHz, -1dB	105.0dB	20k
DR	1kHz, -60dB	113.7dB	20k
		116.7dB	20k, A-weight
S/N	1kHz, no input	113.7dB	20k
		116.7dB	20k, A-weight

Table 5. Dynamic performance by ROHDE & SCHWARZ UPD04

■ Digital Filter Characteristics



1) The passband and stopband scale with fs
2) The analog modulator samples the input at 6.144MHz for fs = 48kHz.
There is no rejection of input signals which are multiples of the modulator sampling frequency:
n * 6.144MHz ± 21.768kHz; n = 0, 1, 2, 3,

AK5392 Measurement Results

Measurement conditions :

AVDD=3.3V, DVDD=5.0V, fs=48kHz,
Input frequency = 1kHz,
Measurement bandwidth = 20Hz ~ 20kHz,
Measurement unit = ROHDE & SCHWARZ UPD04.

FFT plot : averaging = 4,
Points = 8192,
Window = RIFE VINC 3.

Plot :

Fig.1 : THD+N vs. input frequency (Level = -1.0dB)
Fig.2 : THD+N vs. input level
Fig.3 : Linearity
Fig.4 : Cross talk
Fig.5 : FFT (Input signal=1kHz,-1dBFS)
Fig.6 : FFT (Input signal=1kHz,-60dBFS)
Fig.7 : FFT (noise floor)

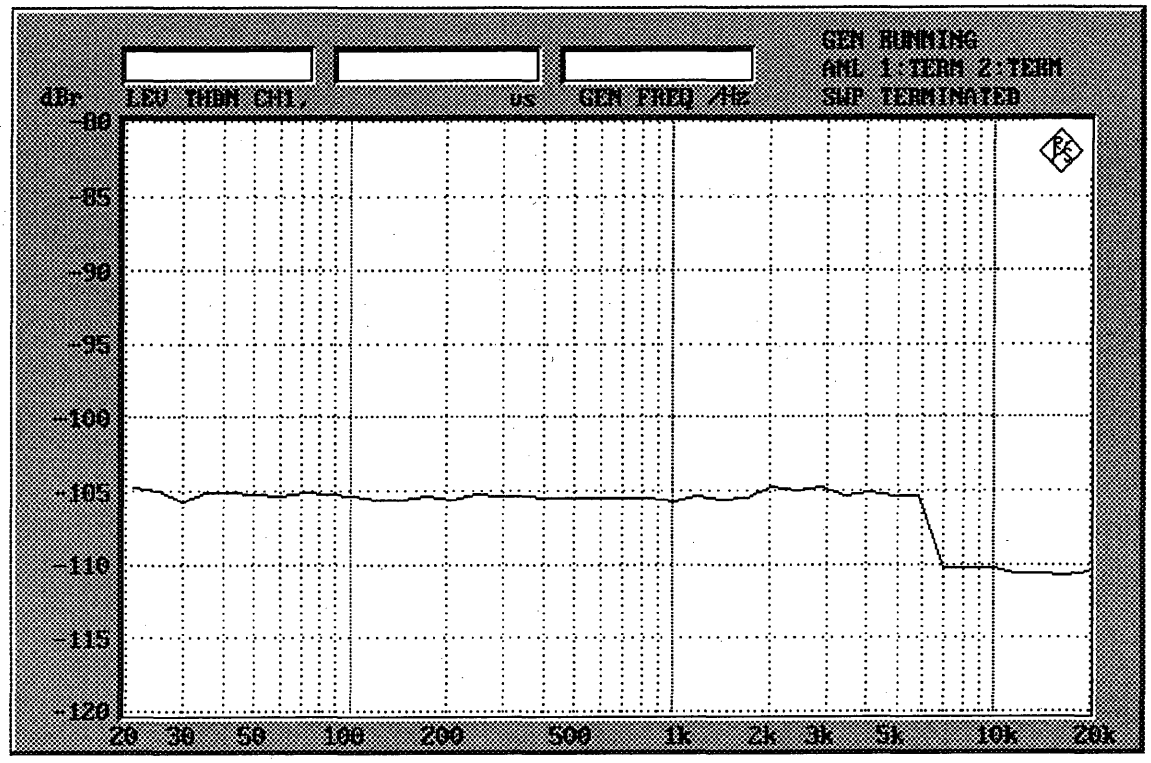


Fig.1 : THD+N vs. input frequency (Input level = -1.0dB @Lch)

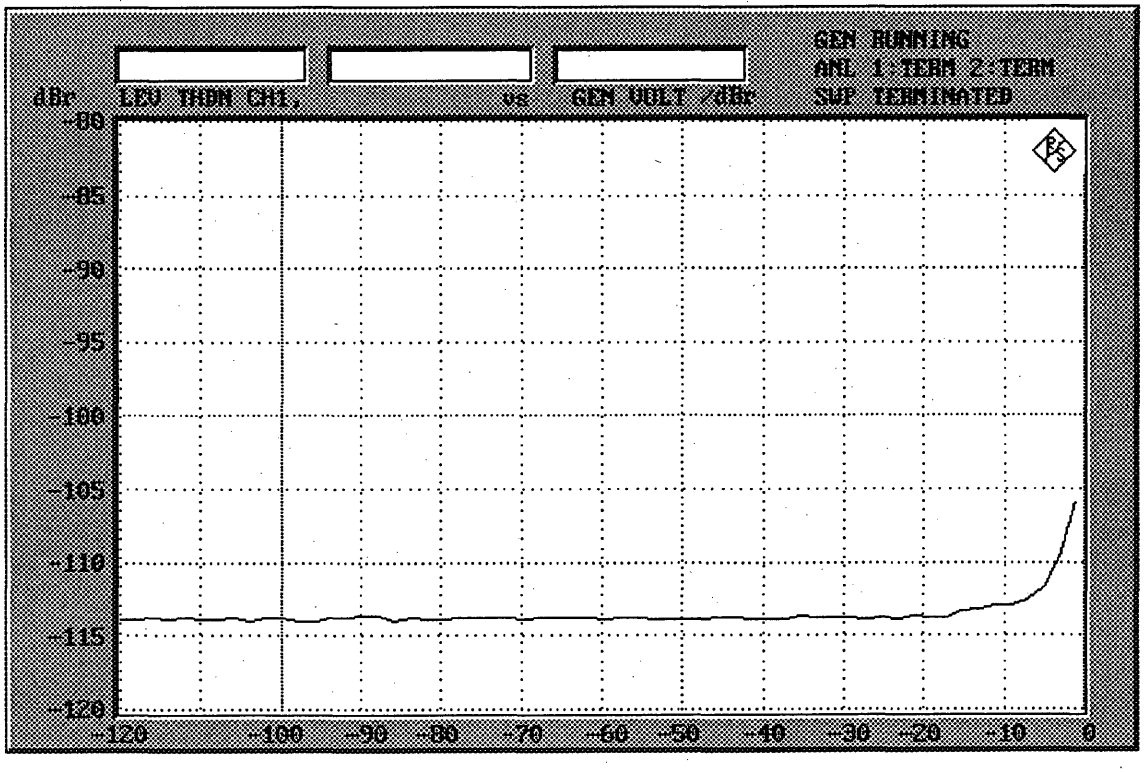


Fig.2 : THD+N vs. input level

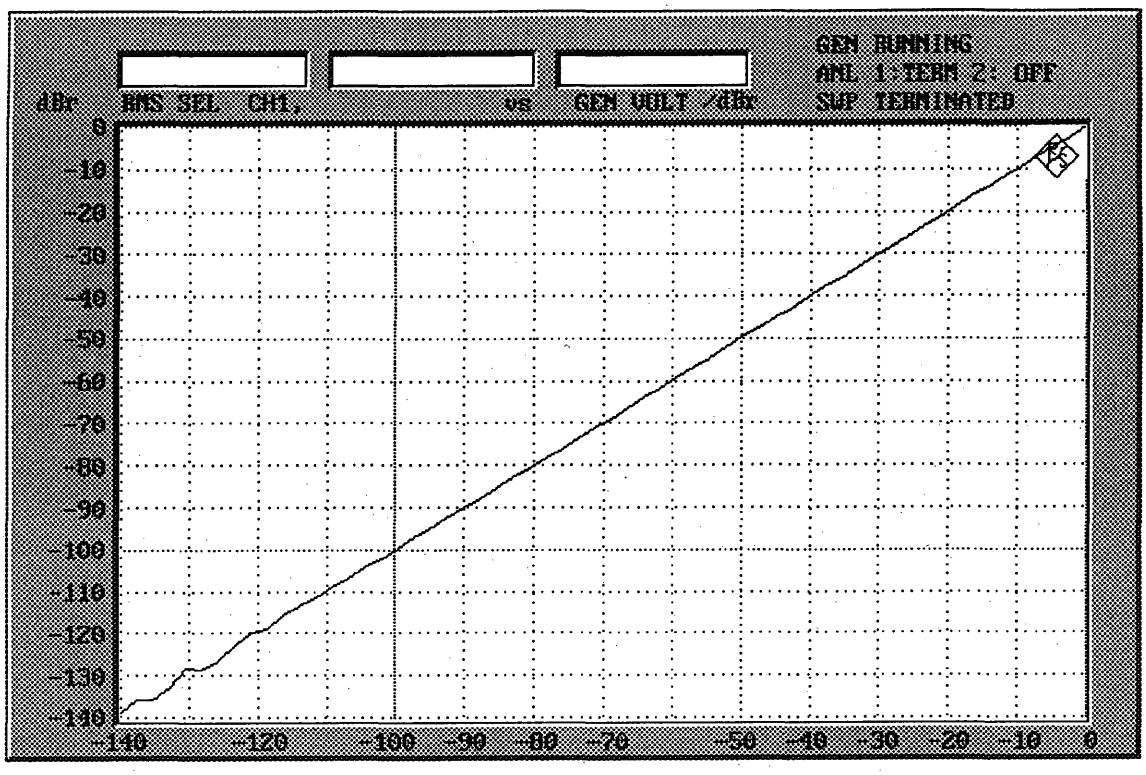


Fig.3 : Linearity

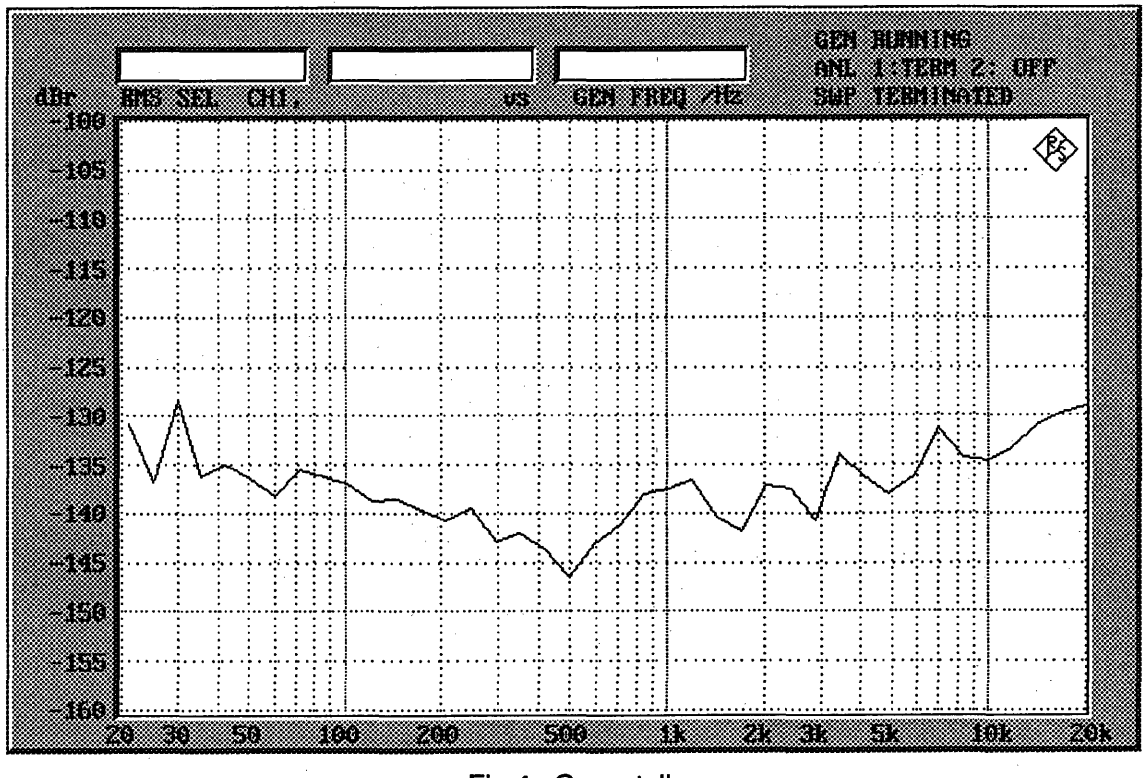


Fig.4 : Cross talk

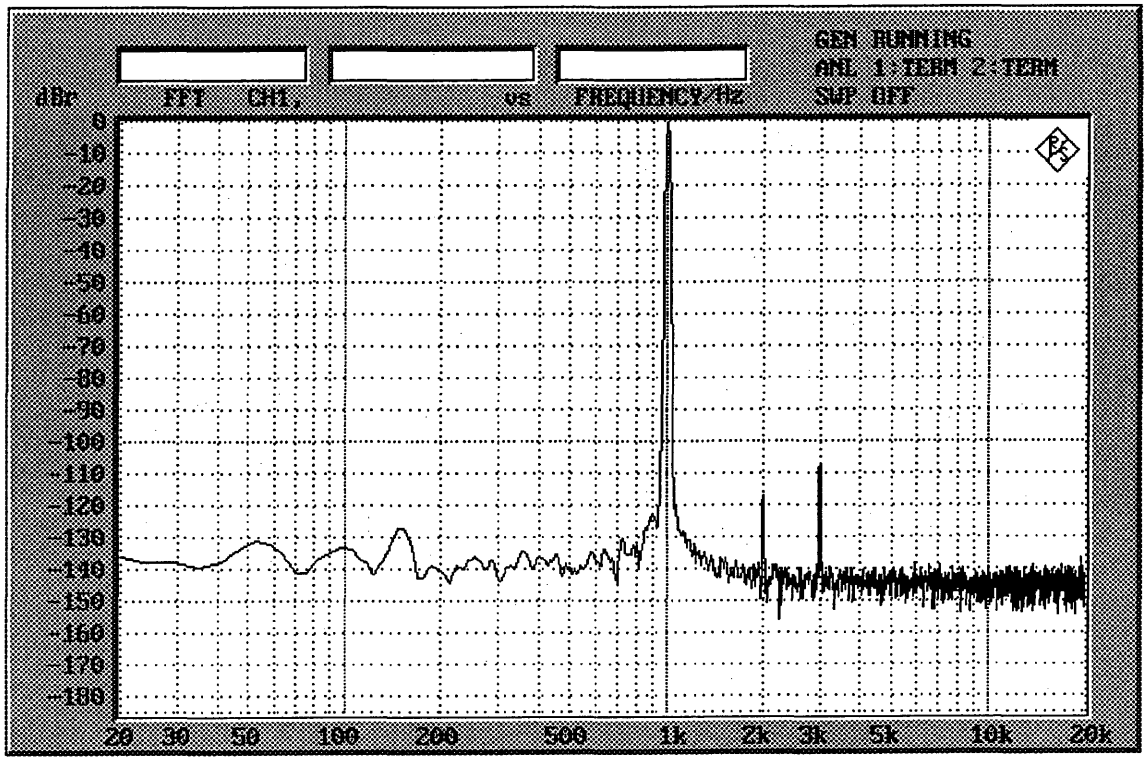


Fig.5 : FFT (Input signal=1kHz,-1.0dBFS)

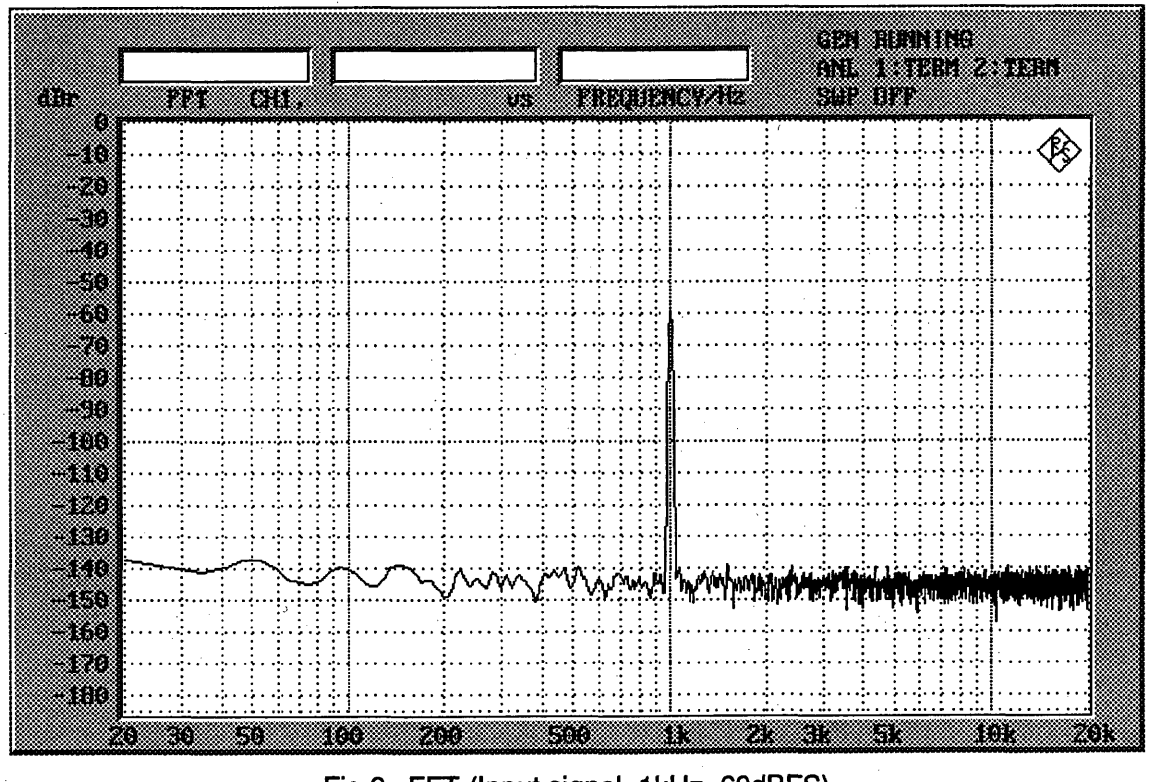


Fig.6 : FFT (Input signal=1kHz,-60dBFS)

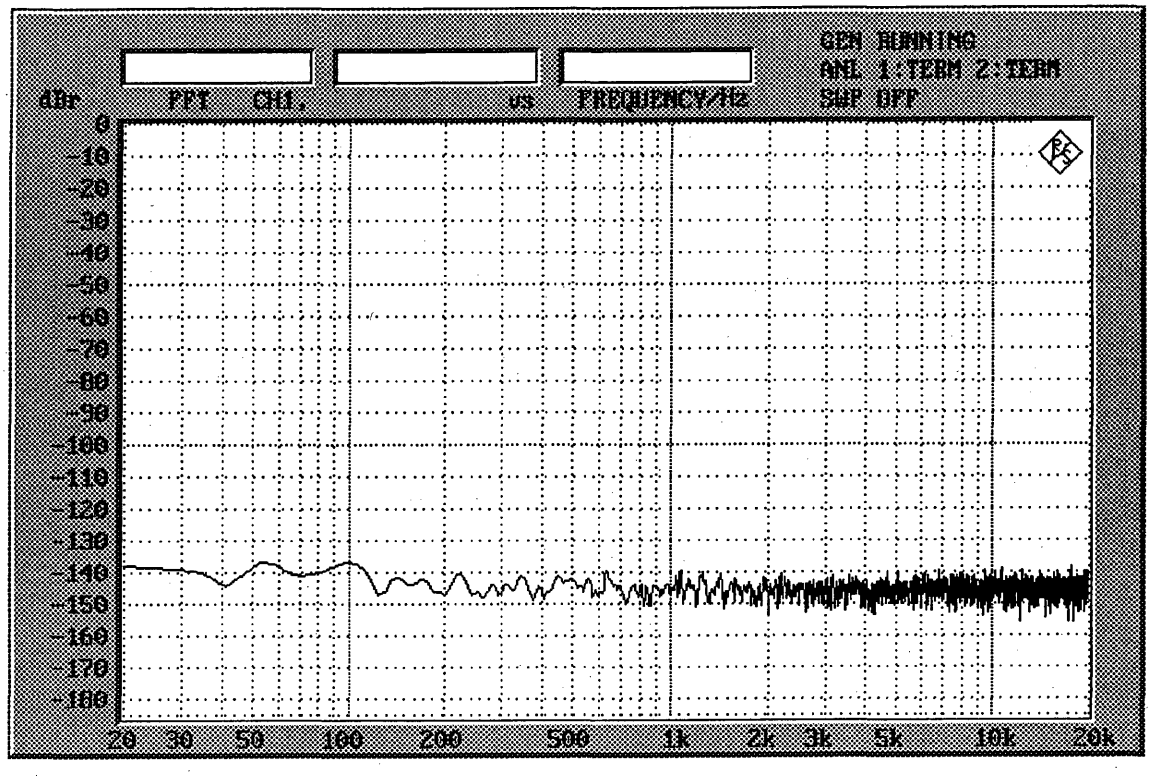
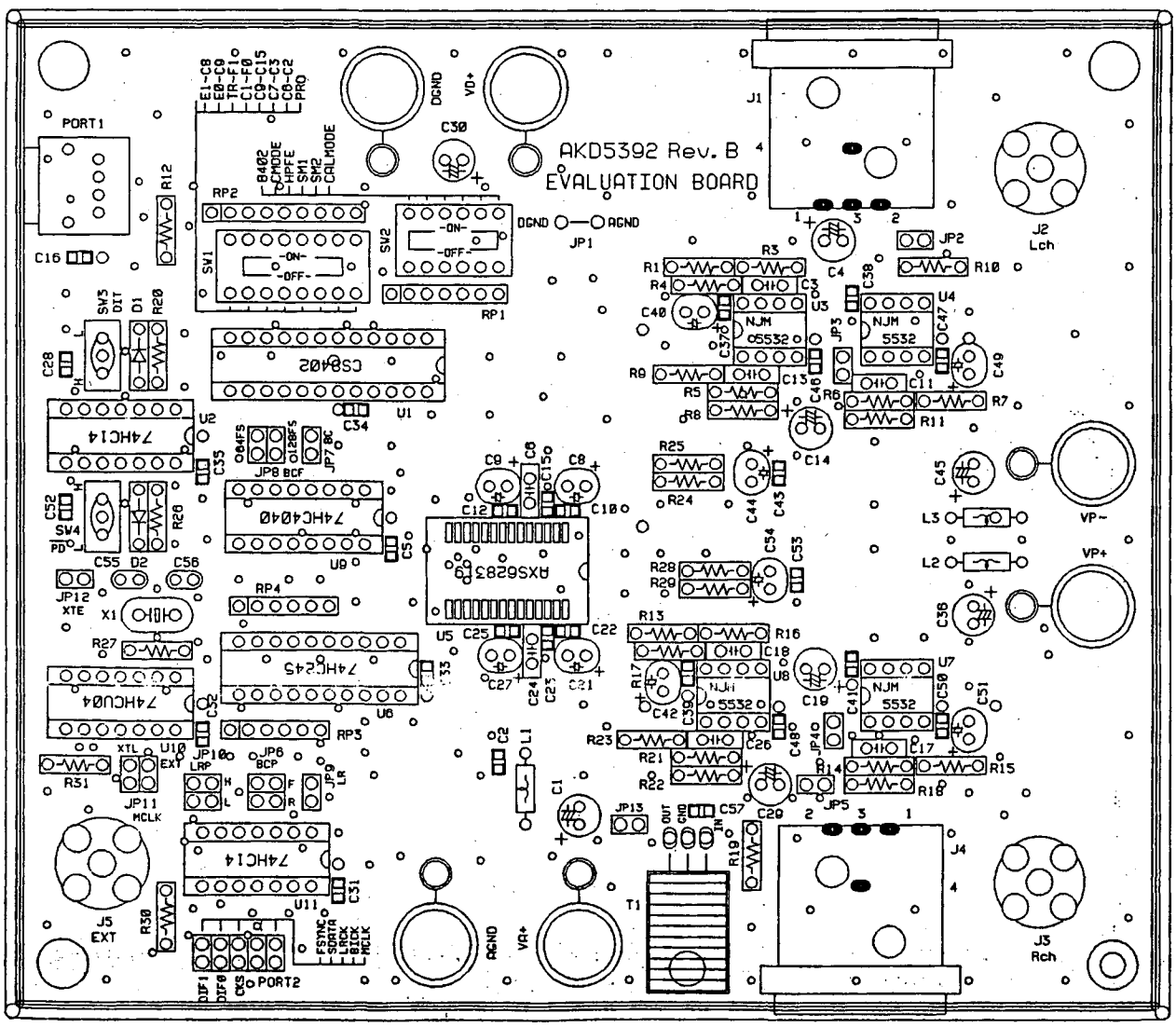
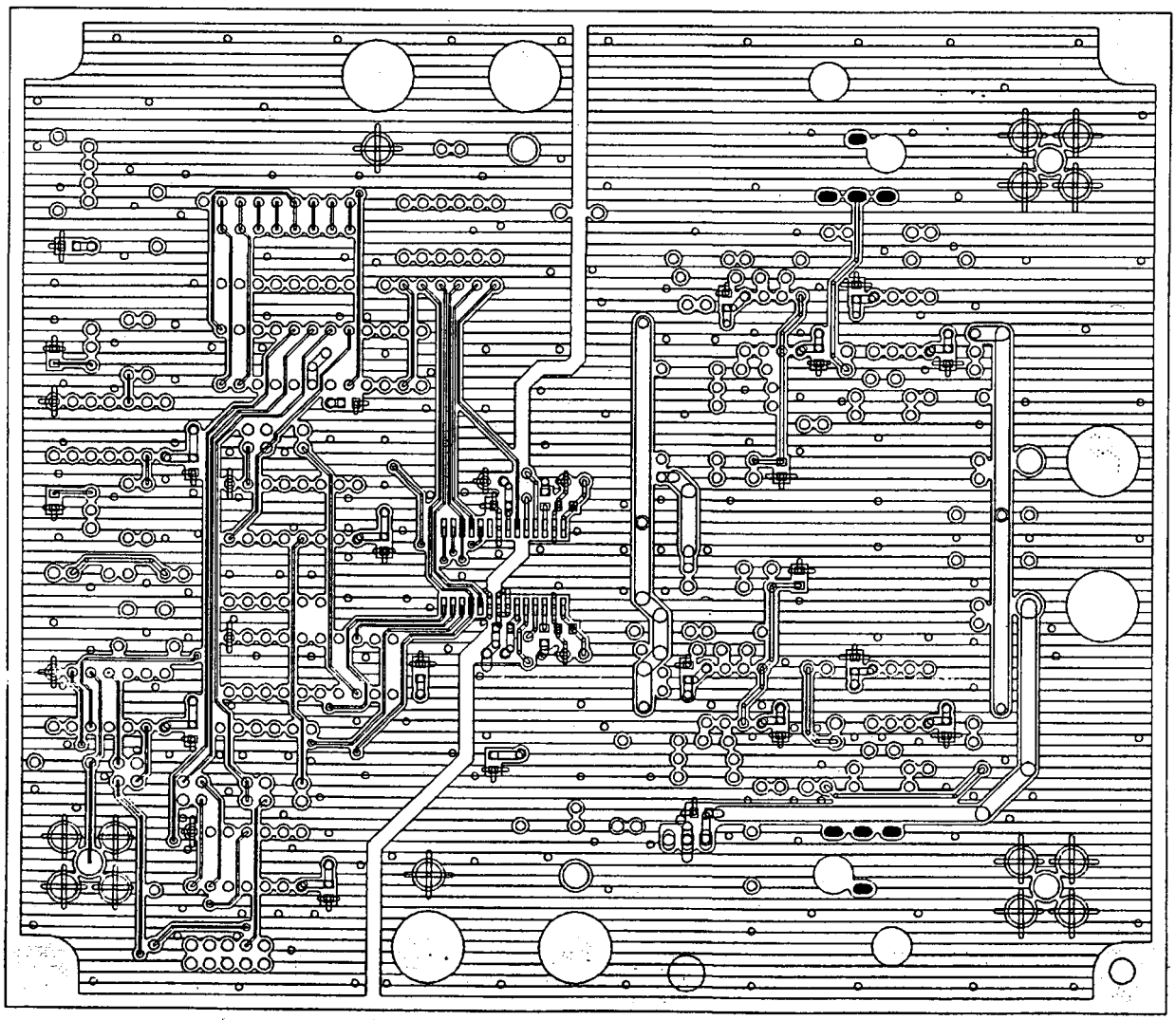


Fig.7 : FFT (noise floor)



AKD5392 rev. B L1 SR
AKD5392 rev. B L1 SILK



AKD5392 rev. B L1

AK0230 rev. B LS

IMPORTANT NOTICE

- These products and their specifications are subject to change without notice. Before considering any use or application, consult the Asahi Kasei Microsystems Co., Ltd. (AKM) sales office or authorized distributor concerning their current status.
- AKM assumes no liability for infringement of any patent, intellectual property, or other right in the application or use of any information contained herein.
- Any export of these products, or devices or systems containing them, may require an export license or other official approval under the law and regulations of the country of export pertaining to customs and tariffs, currency exchange, or strategic materials.
- AKM products are neither intended nor authorized for use as critical components in any safety, life support, or other hazard related device or system, and AKM assumes no responsibility relating to any such use, except with the express written consent of the Representative Director of AKM. As used here:
  (a) A hazard related device or system is one designed or intended for life support or maintenance of safety or for applications in medicine, aerospace, nuclear energy, or other fields, in which its failure to function or perform may reasonably be expected to result in loss of life or in significant injury or damage to person or property.
  (b) A critical component is one whose failure to function or perform may reasonably be expected to result, whether directly or indirectly, in the loss of the safety or effectiveness of the device or system containing it, and which must therefore meet very high standards of performance and reliability.
- It is the responsibility of the buyer or distributor of an AKM product who distributes, disposes of, or otherwise places the product with a third party to notify that party in advance of the above content and conditions, and the buyer or distributor agrees to assume any and all responsibility and liability for and hold AKM harmless from any and all claims arising from the use of said product in the absence of such notification.