PRECISION INTEGRATING ANALOG PROCESSOR

APPLICATIONS

- **4 1/2 digits to 5 1/2 digits plus sign measurements**
- **Precision analog signal processor**
- **Precision sensor interface**
- **High accuracy DC measurement functions**
- **Portable battery operated instruments**
- **Computer peripheral**
- **PCMCIA**

GENERAL DESCRIPTION

The ALD500AU/ALD500A/ALD500 are integrating dual slope analog processors, designed to operate on ±5V power supplies for building precision analog-to-digital converters. The ALD500AU/ALD500A/ALD500 feature specifications suitable for 18 bit/17 bit/16 bit resolution conversion, respectively. Together with three capacitors, one resistor, a precision voltage reference, and a digital controller, a precision Analog to Digital converter with auto zero can be implemented. The digital controller can be implemented by an external microcontroller, under either hardware (fixed logic) or software control. For ultra high resolution applications, up to 23 bit conversion can be implemented with an appropriate digital controller and software.

The ALD500 series of analog processors accept differential inputs and the external digital controller first counts the number of pulses at a fixed clock rate that a capacitor requires to integrate against an unknown analog input voltage, then counts the number of pulses required to deintegrate the capacitor against a known reference voltage. This unknown analog voltage can then be converted by the microcontroller to a digital word, which is translated into a high resolution number, representing an accurate reading. This reading, when ratioed against the reference voltage, yields an accurate, absolute voltage measurement reading.

The ALD500 analog processors consist of on-chip digital control circuitry to accept control inputs, integrating buffer amplifiers, analog switches, and voltage comparators. It functions in four operating modes, or phases, namely auto zero, integrate, deintegrate, and integrator zero phases. At the end of a conversion, the comparator output goes from high to low when the integrator crosses zero during deintegration. ALD500 analog processors also provide direct logic interface to CMOS logic families.

ORDERING INFORMATION

Operating Temperature Range *		
0°C to +70°C	0°C to +70°C	0°C to +70°C
16-Pin Plastic Pin Package	16-Pin Small Outline Package (SOIC)	16-Pin Wide Body Small Outline Package (SOIC)
ALD500PC (16 bit)	ALD500SC (16 bit)	ALD500SWC (16 bit)
ALD500APC (17 bit)	ALD500ASC (17 bit)	ALD500ASWC (17 bit)
ALD500AUPC (18 bit)	ALD500AUSC (18 bit)	ALD500AUSWC (18 bit)

***** Contact factory for industrial temperature range

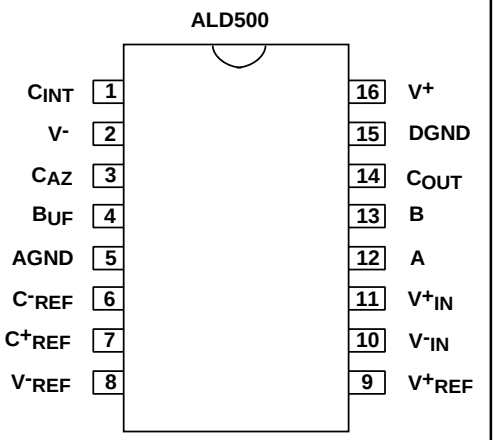
BENEFITS

- Wide dynamic signal range
- Very high noise immunity
- Low cost, simple functionality
- Automatic compensation and cancellation of error sources
- Easy to use to acquire true 18 bit,17 bit, or 16 bit conversion and noise performance
- Inherently linear and stable with temperature and component variations

FEATURES

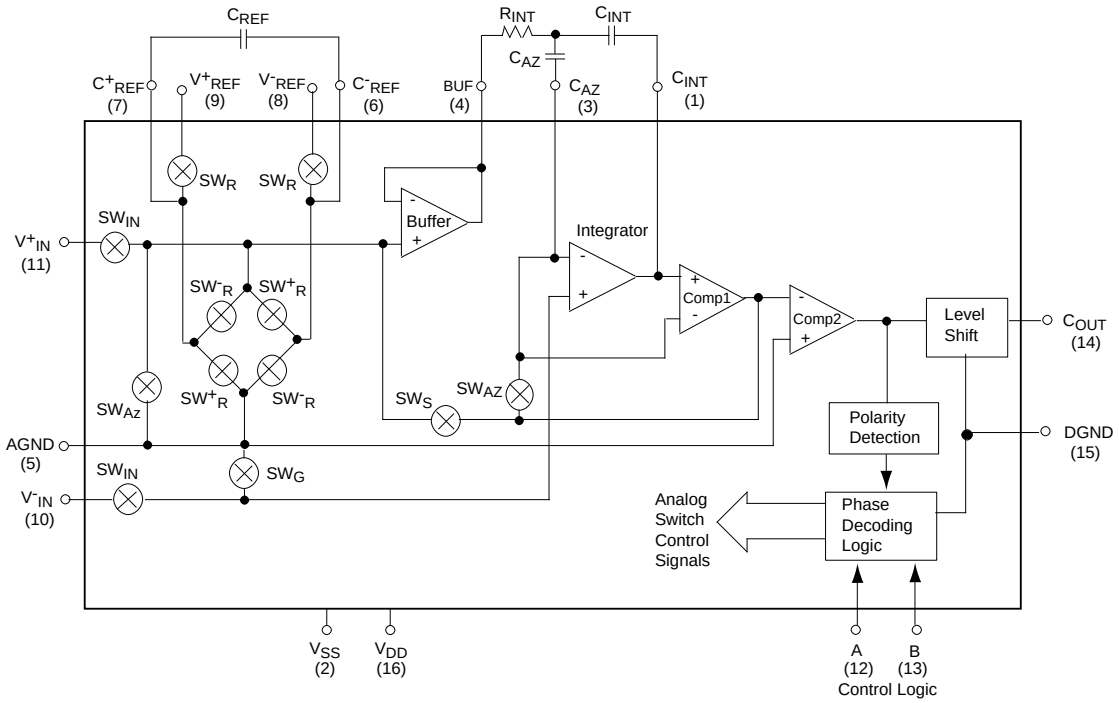
- Resolution up to 18 bits plus sign bit and over-range bit
- Accuracy independent of input source impedances
- High input impedance of $10^{12}\ \Omega$
- Inherently filters and integrates any external noise spikes
- Differential analog input
- Wide bipolar analog input voltage range ±3.5V
- Automatic zero offset compensation
- Low linearity error - as low as 0.002%
- Fast zero-crossing comparator - 1µs
- Low power dissipation - 6mW typical
- Automatic internal polarity detection
- Low input current - 2pA typical
- Microprocessor controlled conversion
- Optional digital control from a microcontroller, an ASIC, or a dedicated digital circuit
- Flexible conversion speed versus resolution trade-off

PIN CONFIGURATION



PC, SC, SWC PACKAGE

FIGURE 1. ALD 500 Functional Block Diagram



GENERAL THEORY OF OPERATION

Dual-Slope Conversion Principles of Operation

The basic principle of dual-slope integrating analog to digital converter is simple and straightforward. A capacitor, C_{INT}, is charged with the integrator from a starting voltage, V_X, for a fixed period of time at a rate determined by the value of an unknown input voltage, which is the subject of measurement. Then the capacitor is discharged at a fixed rate, based on an external reference voltage, back to V_X where the discharge time, or deintegration time, is measured precisely. Both the integration time and deintegration time are measured by a digital counter controlled by a crystal oscillator. It can be demonstrated that the unknown input voltage is determined by the ratio of the deintegration time and integration time, and is directly proportional to the magnitude of the external reference voltage.

The major advantages of a dual-slope converter are:

a. Accuracy is not dependent on absolute values of integration time t_{INT} and deintegration time t_{DINT}, but is dependent on their relative ratios. Long-term clock frequency variations will not affect the accuracy. A standard crystal controlled clock running digital counters is adequate to generate very high accuracies.

b. Accuracy is not dependent on the absolute values of R_{INT} and C_{INT}. as long as the component values do not vary through a conversion cycle, which typically lasts less than 1 second.

c. Offset voltage values of the analog components, such as V_X, are cancelled out and do not affect accuracy.

d. Accuracy of the system depends mainly on the accuracy and the stability of the voltage reference value.

e. Very high resolution, high accuracy measurements can be achieved simply and at very low cost.

An inherent benefit of the dual slope converter system is noise immunity. The input noise spikes are integrated (averaged to near zero) during the integration periods. Integrating ADCs are immune to the large conversion errors that plague successive approximation converters and other high resolution converters and perform very well in high-noise environments.

The slow conversion speed of the integrating converter provides inherent noise rejection with at least a 20dB/decade attenuation rate. Interference signals with frequencies at integral multiples of the integration period are, theoretically, completely removed. Integrating converters often establish the integration period to reject 50/60Hz line frequency interference signals.

The relationship of the integrate and deintegrate (charge and discharge) of the integrating capacitor values are shown below:

$$V_{INT} = V_X - (V_{IN} \cdot t_{INT} / R_{INT} \cdot C_{INT})$$

(integrate cycle) (1)

$V_X = V_{INT} - (V_{REF} \cdot t_{DINT} / R_{INT} \cdot C_{INT})$

(deintegrate cycle) (2)

Combining equations 1 and 2 results in:

$V_{IN} / V_{REF} = -t_{DINT} / t_{INT}$ (3)

where:

V_x = An offset voltage used as starting voltage
V_{INT} = Voltage change across C_{INT} during t_{INT} and during t_{DINT} (equal in magnitude)
V_{IN} = Average, or an integrated, value of input voltage to be measured during t_{INT} (Constant V_{IN})
t_{INT} = Fixed time period over which unknown voltage is integrated
t_{DINT} = Unknown time period over which a known reference voltage is integrated
V_{REF} = Reference Voltage
C_{INT} = Integrating Capacitor value
R_{INT} = Integrating Resistor value

Actual data conversion is accomplished in two phases: Input Signal Integration Phase and Reference Voltage Deintegration Phase.

The integrator output is initialized to 0V prior to the start of Input Signal Integration Phase. During Input Signal Integration Phase, internal analog switches connect V_{IN} to the buffer input where it is maintained for a fixed integration time period (t_{INT}). This fixed integration period is generally determined by a digital counter controlled by a crystal oscillator. The application of V_{IN} causes the integrator output to depart 0V at a rate determined by V_{IN} and a direction determined by the polarity of V_{IN}.

The Reference Voltage Deintegration Phase is initiated immediately after t_{INT}, within 1 clock cycle. During Reference Voltage Deintegration Phase, internal analog switches connect a reference voltage having a polarity opposite that of V_{IN} to the integrator input. Simultaneously the same digital counter controlled by the same crystal oscillator used above is used to start counting clock pulses. The Reference Voltage Deintegration Phase is maintained until the comparator output inside the dual slope analog processor changes state, indicating the integrator has returned to 0V. At that point the digital counter is stopped. The Deintegration time period (t_{DINT}), as measured by the digital counter, is directly proportional to the magnitude of the applied input voltage.

After the digital counter value has been read, the digital counter, the integrator, and the auto zero capacitor are all reset to zero through an Integrator Zero Phase and an Auto Zero Phase so that the next conversion can begin again. In practice, this process is usually automated so that analog-to-digital conversion is continuously updated. The digital control is handled by a microprocessor or a dedicated logic controller. The output, in the form of a binary serial word, is read by a microprocessor or a display adapter when desired.

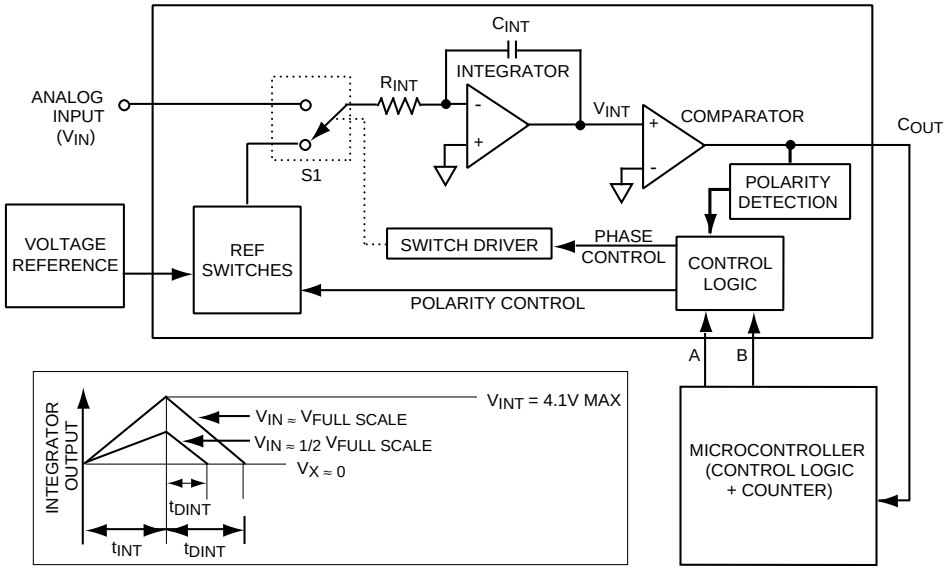


Figure 2. Basic Dual-Slope Converter

Figure 2. Basic Dual-Slope Converter

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V^+ — 13.2V
Differential input voltage range — -0.3V to V^+ +0.3V
Power dissipation — 600 mW
Operating temperature range PC, SC, SWC package — 0°C to +70°C
Storage temperature range — -65°C to +150°C
Lead temperature, 10 seconds — +260°C

OPERATING ELECTRICAL CHARACTERISTICS

T_A = 25°C V^+ = +5.0V V^- = -5.0V (V_{SUPPLY} = ±5.0 V) unless otherwise specified; C_{AZ} = C_{REF} = 0.47µf

		500AU			500A			500				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Resolution		15	30		30	60		60			µV	Note 1
Zero-Scale Error	Z_{SE}			0.0025 0.003			0.003 0.005			0.005 0.008	% %	 0°C to 70°C
End Point Linearity	E_{NL}			0.005 0.007		0.005	0.010 0.015		0.005	0.015 0.020	%	Notes 1, 2 0°C to +70°C
Best Case Straight Line Linearity	N_L			0.0025 0.004		0.003	0.005 0.008		0.003	0.008 0.015	%	Notes 1, 2 0°C to +70°C
Zero-Scale Temperature Coefficient	TC_{ZS}		0.3 0.15	0.6 0.3		0.3 0.15	0.7 0.35		0.3 0.15	0.7 0.35	µV/°C ppm/°C	0°C to +70°C Note 1
Full-Scale Symmetry Error (Rollover Error)	S_{YE}		0.005 0.008			0.008 0.010			0.01 0.012		% %	 0°C to 70°C
Full-Scale Temperature Coefficient	TC_{FS}		1.3			1.3			1.3		ppm/°C	0°C to +70°C
Input Current	I_{IN}		2			2			2		pA	V_{IN} = 0V
Common-Mode Voltage Range	CMVR	V^-+1.5		V^+-1.5	V^-+1.5		V^+-1.5	V^-+1.5		V^+-1.5	V	
Integrator Output Swing	V_{INT}	V^-+0.9		V^+-0.9	V^-+0.9		V^+-0.9	V^-+0.9		V^+-0.9	V	
Analog Input Signal Range	V_{IN}	V^-+1.5		V^+-1.5	V^-+1.5		V^+-1.5	V^-+1.5		V^+-1.5	V	AGND = 0V
Voltage Reference Range	V_{REF}	V^-+1		V^+-1	V^-+1		V^+-1	V^-+1		V^+-1	V	

DC ELECTRICAL CHARACTERISTICS

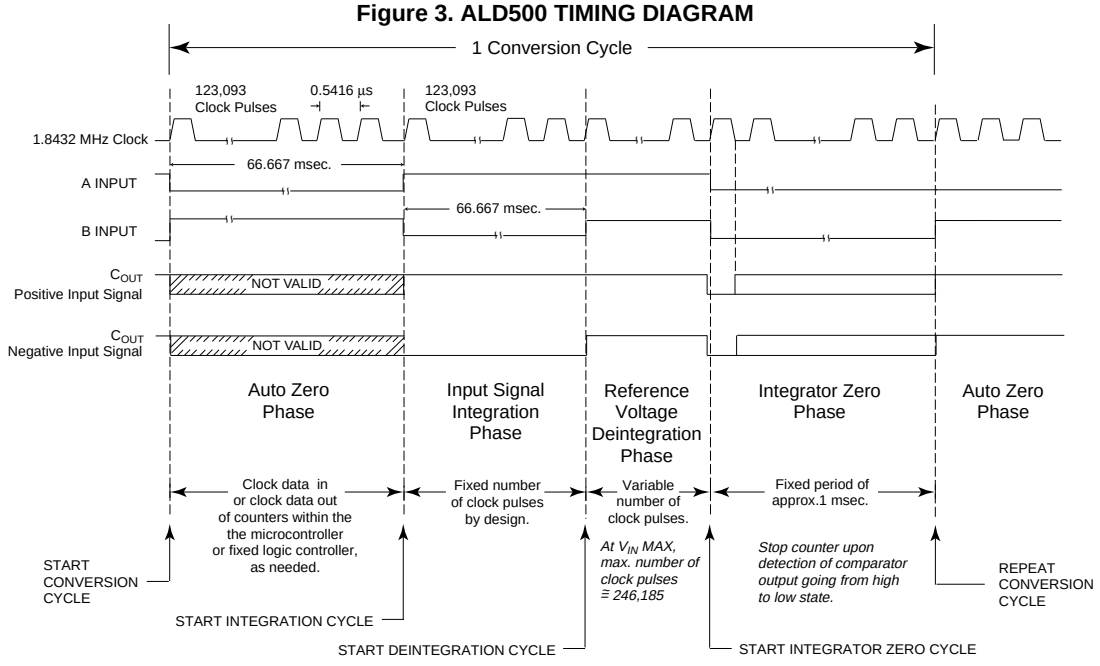
T_A = 25°C V^+ = +5.0V V^- = -5.0V (V_{SUPPLY} = ±5.0 V) unless otherwise specified; C_{AZ} = C_{REF} = 0.47µf

		500AU			500A			500				
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions**
Supply Current	I_S		0.6	1.0		0.6	1.0		0.6	1.0	mA	V^+ = 5V , A =1,B=1
Power Dissipation	P_D			10			10			10	mW	V_{SUPPLY} = ±5V
Positive Supply Range	V_{+S}	4.5		5.5	4.5		5.5	4.5		5.5	V	Note 4
Negative Supply Range	V_{-S}	-4.5		-5.5	-4.5		-5.5	-4.5		-5.5	V	Note 4
Comparator Logic 1, Output High	V_{OH}	4			4			4			V	I_{SOURCE} = 400µA
Comparator Logic 0, Output Low	V_{OL}			0.4			0.4			0.4	V	I_{SINK} = 1.1mA
Logic 1, Input High Voltage	V_{IH}	3.5			3.5			3.5			V	
Logic 0, Input Low Voltage	V_{IL}			1			1			1	V	
Logic Input Current	I_L		0.01			0.01			0.01		µA	
Comparator Delay	t_D		1			1			1		µsec	Note 5

NOTES:

1. Integrate time ≥ 66 msec., Auto Zero time ≥ 66 msec., $V_{INT} \cong$ 4V, V_{IN} = 2.0V Full Scale
   Resolution = V_{INT} /integrate time/clock period
2. End point linearity at ±1/4, ±1/2, ±3/4 Full Scale after Full Scale adjustment.
3. Rollover Error also depends on C_{INT}, C_{REF}, C_{AZ} characteristics.
4. Contact factory for other power supply operating voltage ranges, including Vsupply = ±3V or Vsupply = ±2.5V.
5. Recommended selection of clock periods of one of the following:
   t clk = 0.27µsec, 0.54µsec, or 1.09µsec
   which corresponds to clock frequencies of 3.6864 MHz, 1.8432 MHz, 0.9216 MHz respectively.

Figure 3. ALD500 TIMING DIAGRAM



PIN DESCRIPTION

Pin No.	Symbol	Description
1	C_{INT}	Integrator capacitor connection.
2	V^-	Negative power supply.
3	C_{AZ}	The Auto-zero capacitor connection.
4	BUF	The Integrator resistor buffer connection.
5	AGND	This pin is analog ground.
6	C^-_{REF}	Negative reference capacitor connection.
7	C^+_{REF}	Positive reference capacitor connection.
8	V^-_{REF}	External voltage reference (-) connection.
9	V^+_{REF}	External voltage reference (+) connection.
10	V^-_{IN}	Negative analog input.
11	V^+_{IN}	Positive analog input.
12	A	Converter phase control MSB Input.
13	B	Converter phase control LSB Input.
14	C_{OUT}	Comparator output. C_{OUT} is HIGH during the Integration phase when a positive input voltage is being integrated and is LOW when a negative input voltage is being integrated. A HIGH-to-LOW transition on C_{OUT} signals the processor that the Deintegrate phase is completed. C_{OUT} is undefined during the Auto-Zero phase. It should be monitored to time the Integrator Zero phase.
15	DGND	Digital ground.
16	V^+	Positive power supply.

Table 1. Conversion Phase and Control Logic Internal Analog Switch Functions

		Switch Functions					
Conversion Phase	**Control Logic**	**Input Connect**	**Reference Input Polarity**	**Auto Zero**	**Reference Sample**	**V_{IN}=AGND**	**System Offset**
		SW_{IN}	**SW^+_R or SW^-_R**	**SW_{AZ}**	**SW_R**	**SW_G**	**SW_S**
Auto Zero	**A = 0, B = 1**	**Open**	**Open**	**Closed**	**Closed**	**Closed**	**Open**
Input Signal Integration	**A = 1, B = 0**	**Closed**	**Open**	**Open**	**Open**	**Open**	**Open**
Reference Voltage Deintegration	**A = 1, B = 1**	**Open**	**Closed***	**Open**	**Open**	**Closed**	**Open**
Integrator Output Zero	**A = 0, B = 0**	**Open**	**Open**	**Open**	**Closed**	**Closed**	**Closed**

*SW^+_R would be closed for a positive input signal. SW^-_R would be closed for a negative input signal.

ALD500AU/ALD500A/ALD500 CONVERSION CYCLE

The ALD500AU/ALD500A/ALD500 conversion cycle takes place in four distinct phases, the Auto Zero Phase, the Input Signal Integration Phase, the Reference Voltage Deintegration Phase, and the Integrator Zero Phase. A typical measurement cycle uses all four phases in an order sequence as mentioned above. The internal analog switch status for each of these phases is summarized in Table 1.

The following is a detailed description of each one of the four phases of the conversion cycle.

Auto Zero Phase (AZ Phase)

The analog-to-digital conversion cycle begins with the Auto Zero Phase, when the digital controller applies low logic level to input A and high logic level to input B of the analog processor. During this phase, the reference voltage is stored on reference capacitor C_{REF}, comparator offset voltage and the sum of the buffer and integrator offset voltages are stored on auto zero capacitor C_{AZ}. During the Auto Zero Phase, the comparator output is characterized by an indeterminate waveform.

During the Auto Zero Phase, the external input signal is disconnected from the internal circuitry of the ALD500AU/ALD500A/ALD500 by opening the two SW_{IN} analog switches and connecting the internal input nodes internally to analog ground. A feedback loop, closed around the integrator and comparator, charges the C_{AZ} capacitor with a voltage to compensate for buffer amplifier, integrator and comparator offset voltages.

This is the system initialization phase, when a conversion is ready to be initiated at system turn-on. In practice the converter can be operated in continuous conversion mode, where AZ phase must be long enough for the circuit conditions to settle out any system errors. Typically this phase is set to be equal to t_{INT}.

Input Signal Integration Phase (INT Phase)

During the Input Signal Integration Phase (INT), the ALD500AU/ALD500A/ALD500 integrates the differential voltage across the (V^+_{IN}) and (V^-_{IN}) inputs. The differential voltage must be within the device's common-mode voltage range CMVR. The integrator charges C_{INT} for a fixed period of time, or counts a fixed number of clock pulses, at a rate determined by the magnitude of the input voltage. During this phase, the analog inputs see only the high impedance of the noninverting operational amplifier input of the buffer. The integrator responds only to the voltage difference between the analog input terminals, thus providing true differential analog inputs.

The input signal polarity is determined by software control at the end of this phase: C_{OUT} = 1 for positive input polarity; C_{OUT} = 0 for negative input polarity. The value is, in effect, the sign bit for the overall conversion result.

The duration of this phase is selected by design to be a fixed time and depends on system parameters and component value selections. The total number of clock pulses or clock counts, during integration phase determine the resolution of the conversion. For high resolution applications, this total number of clock pulses should be maximized. The basic unit of resolution is in μV/count. Before the end of this phase, comparator output is sampled by the microcontroller. This phase is terminated by changing logic inputs AB from 10 to 11.

Reference Voltage Deintegration Phase (D_{INT} Phase)

At the end of the Input Signal Integration Phase, Reference Voltage Deintegration Phase begins. The previously charged reference capacitor is connected with the proper polarity to ramp the integrator output back to zero. The ALD500AU/ALD500A/ALD500 analog processors automatically selects the proper logic state to cause the integrator to ramp back toward zero at a rate proportional to the reference voltage stored on the reference capacitor. The time required to return to zero is measured by the counter in the digital processor using the same crystal oscillator. The phase is terminated by the comparator output after the comparator senses when the integrator output crosses zero. The counter contents are then transferred to the register. The resulting time measurement is proportional to the magnitude of the applied input voltage.

The duration of this phase is precisely measured from the transition of AB from 10 to 11 to the falling edge of the comparator output, usually with a crystal controlled digital counter chain. The comparator delay contributes some error in this phase. The typical comparator delay is 1μ_{sec}. The comparator delay and overshoot will result in error timing, which translates into error voltages. This error can be zeroed and minimized during Integrator Output Zero Phase and corrected in software, to within ±1 count of the crystal clock (which is equivalent to within ± 1 LSB, when 1 clock pulse = 1 LSB).

Integrator Zero Phase (I_{NTZ} Phase)

This phase guarantees the integrator output is at 0V when the Auto Zero phase is entered, and that only system offset voltages are compensated. This phase is used at the end of the reference voltage deintegration and is used for applications with high resolutions. If this phase is not used, the value of the Auto-Zero capacitor (C_{AZ}) must be much greater than the value of the integration capacitor (C_{INT}) to reduce the effects of charge-sharing. The Integrator Zero phase should be programmed to operate until the Output of the Comparator returns "HIGH". A typical Integrator Zero Phase lasts 1msec.

The comparator delay and the controller's response latency may result in Overshoot causing charge buildup on the integrator at the end of a conversion. This charge must be removed or performance will degrade. The Integrator Output Zero phase should be activated (AB = 00) until C_{OUT} goes high. At this point, the integrator output is near zero. Auto Zero Phase should be entered (AB = 01) and the ALD500AU/ALD500A/ALD500 is held in this state until the next conversion cycle.

Differential Inputs (V^+_{IN},V^-_{IN})

The ALD500AU/ALD500A/ALD500 operates with differential voltages within the input amplifier common-mode voltage range. The amplifier common-mode range extends from 1.5V below positive supply to 1.5V above negative supply. Within this common-mode voltage range, common-mode rejection is typically 95dB.

The integrator output also follows the common-mode voltage. When large common-mode voltages with near full-scale differential input voltages are applied, the input signal drives the integrator output to near the supply rails where the integrator output is near saturation. Under such conditions, linearity of the converter may be adversely affected as the integrator swing can be reduced. The integrator output must not be allowed to saturate. Typically, the integrator output can swing to within 0.9V of either supply rails without loss of linearity.

Analog Ground

Analog Ground is V^-_{IN} during Auto Zero Phase and Reference Voltage Deintegration Phase. If V^-_{IN} is different from analog ground, a common-mode voltage exists at the inputs. This common mode signal is rejected by the high common mode rejection ratio of the converter. In most applications, V^-_{IN} is set at a fixed known voltage (i.e., power supply ground). All other ground connections should be connected to digital ground in order to minimize noise at the inputs.

Differential Reference (V^+_{REF}, V^-_{REF})

The reference voltage can be anywhere from 1V of the power supply voltage rails of the converter. Roll-over error is caused by the reference capacitor losing or gaining charge due to the stray capacitance on its nodes. The difference in reference for (+) or (-) input voltages will cause a roll-over error. This error can be minimized by using a large reference capacitor in comparison to the stray capacitance.

Phase Control Inputs (A, B)

The A and B logic inputs select the ALD500AU/ALD500A/ALD500 operating phase. The A and B inputs are normally driven by a microprocessor I/O port or external logic, using CMOS logic levels. For logic control functions of A and B logic inputs, see Table 1.

Comparator Output (C_{OUT})

By monitoring the comparator output during the Input Signal Integration Phase, which is a fixed signal integrate time period, the input signal polarity can be determined by the microcontroller controlling the conversion. The comparator output is HIGH for positive signals and LOW for negative signals during the Input Signal Integration Phase. The state of the comparator should be checked by the microcontroller at the end of the Input Signal Integration Phase, just before transition to the Reference Voltage Deintegration Phase. For very low level input signals noise may cause the comparator output state to toggle between positive and negative states. For the ALD500AU/ALD500A/ALD500, this noise has been minimized to typically within one count.

At the start of the Reference Voltage Deintegration Phase, comparator output is set to HIGH state. During the Reference Voltage Deintegration Phase, the microcontroller must monitor the comparator output to make a HIGH-to-LOW transition as the integrator output ramp crosses zero relative to analog ground. This transition indicates that the conversion is complete. The microcontroller then stops and records the pulse count. The internal comparator delay is 1µsec, typically. The comparator output is undefined during the Auto Zero Phase.

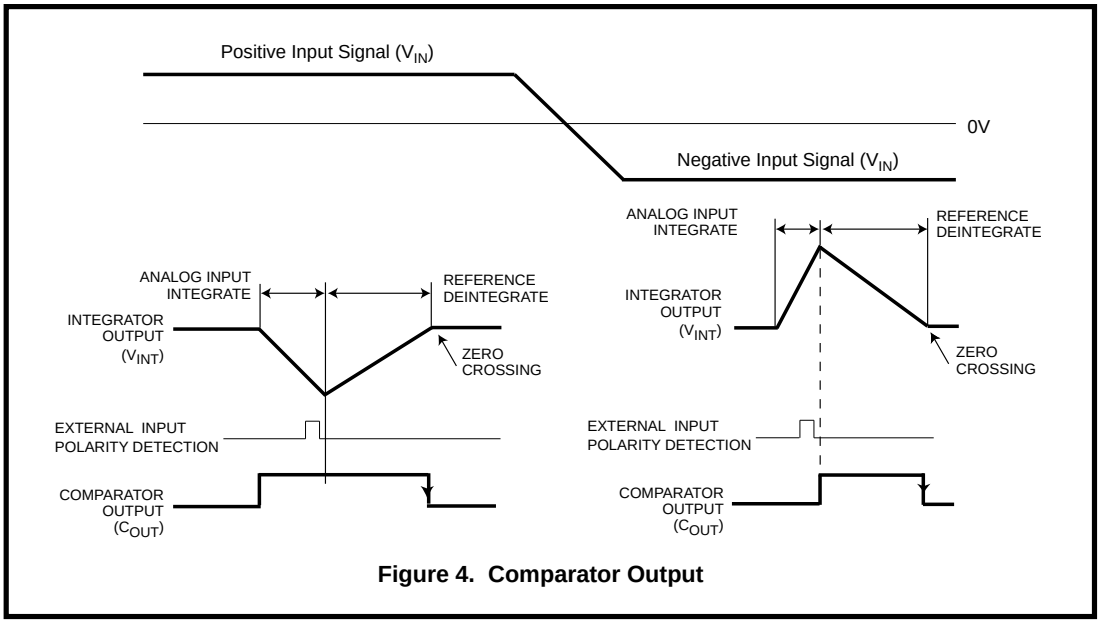


Figure 4. Comparator Output

APPLICATIONS AND DESIGN NOTES

Determination and Selection of System Variables

The procedure outlined below allows the user to determine the values for the following ALD500AU/ALD500A/ALD500 system design variables:

(1) Determine Input Voltage Range
(2) Clock Frequency and Resolution Selection
(3) Input Integration Phase Timing
(4) Integrator Timing Components (R_{INT}, C_{INT})
(5) Auto Zero and Reference Capacitors
(6) Voltage Reference

System Timing

Figure 3 and Figure 4 show the overall timing for a typical system in which ALD500AU/ALD500A/ALD500 is interfaced to a microcontroller. The microcontroller drives the A, B inputs with I/O lines and monitors the comparator output, C_{OUT}, using an I/O line or dedicated timer-capture control pin. It may be necessary to monitor the state of the comparator output in addition to having it control a timer directly during the Reference Deintegration Phase.

There are four critical timing events: sampling the input polarity; capturing the deintegration time; minimizing overshoot and properly executing the Integrator Output Zero Phase.

Selecting Input Integration Time

For maximum 50/60 cycle noise rejection, Input Integration Time must be picked as a multiple of the period of line frequency. For example, t_{INT} times of 33msec, 66msec and 100 msec maximize 60Hz line rejection, and 20msec, 40 msec, 80msec, and 100 msec maximize 50Hz line rejection. Note that t_{INT} of 100 msec maximizes both 60 Hz and 50Hz line rejection.

INT and D_{INT} Phase Timing

The duration of the Reference Deintegrate Phase (D_{INT}) is a function of the amount of voltage charge stored on the integrator capacitor during INT phase, and the value of V_{REF}. The D_{INT} phase must be initiated immediately following INT phase and terminated when an integrator output zero-crossing is detected. In general, the maximum number of counts chosen for D_{INT} phase is twice to three times that of INT phase with V_{REF} chosen as a maximum voltage relative to V_{IN}. For example, $V_{REF} = V_{IN}(max)/2$ would be a good reference voltage.

Integrating Resistor (R_{INT})

The desired full-scale input voltage and amplifier output current capability determine the value of R_{INT}. The buffer and integrator amplifiers each have a full-scale current of 20µA.

The value of R_{INT} is therefore directly calculated as follows:

$$R_{INT} = V_{IN}\ MAX / 20\ \mu A$$

where:

V_{IN} MAX = Maximum input voltage desired (full count voltage)
R_{INT} = Integrating Resistor value

For minimum noise and maximum linearity, R_{INT} should be in the range of between 50kΩ to 150kΩ .

Integrating Capacitor (C_{INT})

The integrating capacitor should be selected to maximize integrator output voltage swing V_{INT}, for a given integration time, without output level saturation. For +/-5V supplies, recommended V_{INT} range is between +/- 3 Volt to +/-4 Volt. Using the 20µA buffer maximum output current, the value of the integrating capacitor is calculated as follows:

$$C_{INT} = (t_{INT}) \cdot (20 \times 10^{-6}) / V_{INT}$$

where: t_{INT} = Input Integration Phase Period
V_{INT} = Maximum integrator output voltage swing

It is critical that the integrating capacitor must have a very low dielectric absorption, as charge loss or gain during conversion directly converts into an error voltage. Polypropylene capacitors are recommended while Polyester and Polybicarbonate capacitors may also be used in less critical applications.

Reference (C_{REF}) and Auto Zero (C_{AZ}) Capacitors

C_{REF} and C_{AZ} must be low leakage capacitors (e.g. polypropylene types). The slower the conversion rate, the larger the value C_{REF} must be. Recommended capacitor values for C_{REF} and C_{AZ} are equal to C_{INT}. Larger values for C_{AZ} and C_{REF} may also be used to limit roll-over errors.

Calculate V_{REF}

The reference deintegration voltage is calculated using:

$$V_{REF} = (V_{INT}) \cdot (C_{INT}) \cdot (R_{INT}) / 2(t_{INT})$$

Converter Noise

The converter noise is the total algebraic sum of the integrator noise and the comparator noise. This value is typically 14 µV peak to peak. The higher the value of the reference voltage, the lower the converter noise. Such sources of noise errors can be reduced by increased integration times, which effectively filter out any such noise. If the integration time periods are selected as multiples of 50/60Hz frequencies, then 50/60Hz noise is also rejected, or averaged out. The signal-to-noise ratio is related to the integration time (t_{INT}) and the integration time constant (R_{INT}) (C_{INT}) as follows:

$$S/N\ (dB) = 20\ Log\ ((V_{INT} / 14 \times 10^{-6}) \cdot t_{INT} /(R_{INT} \cdot C_{INT}))$$

This converter noise can also be reduced by using multiple samples and mathematically averaged. For example, taking 16 samples and averaging the readings result in a mathematical (by software) filtering of noise to less than 4µV.

EQUATIONS AND DERIVATIONS

Dual Slope Analog Processor equations and derivations are as follows:

$$\frac{1}{R_{INT} \cdot C_{INT}} \int_0^{t_{INT}} V_{IN}(t)dt = \frac{V_{REF} \cdot t_{DINT}}{R_{INT} \cdot C_{INT}} \quad (1)$$

For $V_{IN}(t) = V_{IN}$ (constant):

$$\frac{1}{R_{INT} \cdot C_{INT}} t_{INT} \cdot V_{IN} = \frac{V_{REF} \cdot t_{DINT}}{R_{INT} \cdot C_{INT}} \quad (2)$$

$$\therefore V_{IN} = V_{REF} \cdot \frac{t_{DINT}}{t_{INT}} \quad (2a)$$

$$C_{INT} = \frac{t_{INT} \cdot I_B}{V_{INT}} \quad (3)$$

At $V_{IN}MAX$, the current I_B is also at a maximum level, for a given R_{INT} value:

$$R_{INT} = \frac{V_{IN}}{I_B} = \frac{V_{IN}MAX}{I_BMAX} \quad (4)$$

From equation (2a),

$$V_{REF} = \frac{V_{IN} \cdot t_{INT}}{t_{DINT}} \quad (5a)$$

OR

$$V_{REF} = \frac{V_{IN}\,MAX \cdot t_{INT}}{t_{DINT}\,MAX} \quad (5b)$$

Rearranging equations (3) and (4):

$$t_{INT} = \frac{C_{INT} \cdot V_{INT}}{I_B} \quad (6)$$

and

$$I_BMAX = \frac{V_{IN}MAX}{R_{INT}} \quad (7)$$

At $V_{INT} = V_{INT}$ MAX, equation (6) becomes:

$$t_{INT} = \frac{C_{INT} \cdot V_{INT}MAX}{I_BMAX} \quad (6a)$$

Combining (6a) and (7):

$$\therefore t_{INT} = \frac{C_{INT} \cdot V_{INT}MAX \cdot R_{INT}}{V_{IN}MAX} \quad (8)$$

In equation (5b), substituting equation (8) for t_{INT}:

$$V_{REF} = \frac{V_{IN}\,MAX \cdot \dfrac{C_{INT} \cdot V_{INT}MAX \cdot R_{INT}}{V_{IN}\,MAX}}{t_{DINT}\,MAX} \quad (9)$$

$$= \frac{C_{INT} \cdot V_{INT}MAX \cdot R_{INT}}{t_{DINT}\,MAX}$$

For t_{DINT} MAX = 2 x t_{INT}, equation (9) becomes:

$$V_{REF} = \frac{C_{INT} \cdot V_{INT}MAX \cdot R_{INT}}{2t_{INT}} \quad (10)$$

DESIGN EXAMPLES

We now apply these equations in the following design examples.

Design Example 1:

1. Pick resolution = 16 bit.

2. Pick $t_{INT} = 4x\frac{1}{60Hz}$ = 4 x 16.6667 msec.
   = 66.6667ms
   = 0.0666667 sec.

3. Pick clock period = 1.08507 μs and number of counts over $t_{INT} = \frac{0.0666667}{1.08507x10^{-6}}$ = 61440

4. Pick $V_{IN}MAX$ value, e.g., $V_{IN}MAX$ = 2.0 V

   $I_BMAX = 20\mu A \rightarrow R_{INT} = \frac{2.0}{20x10^{-6}} = 100\ k\Omega$

5. Applying equation (3) to calculate C_{INT}:

   $C_{INT} = (0.0666667)(20x10^{-6})/4$ where V_{INT} = 4.0V
   $\cong 0.33\ \mu F$

6. Pick C_{REF} and $C_{AZ} \geq C_{INT}$: $C_{REF} \cong C_{AZ} \cong 0.33\ \mu F$

7. Pick $t_{DINT} = 2 \times t_{INT}$ = 133.3334 msec

8. Calculate $V_{REF} = \frac{V_{INT}MAX \cdot C_{INT} \cdot R_{INT}}{t_{DINT}\,MAX}$ V

   $= \frac{4 \times 0.33 \times 10^{-6} \times 100 \times 10^{3}}{133.3334 \times 10^{-3}}$ V

   = 0.99V

   $\cong$ 1.00V

Design Example 2:

1. Select resolution of 17 bit. Total number of counts during t_{INT} is131,072.

2. We can pick t_{INT} of 16.6667 msec. x 5 = 83.3333 msec.
   or alternately, pick t_{INT} equal
   16.6667 msec. x 6 = 100.00 msec.
   (for 60 Hz rejection)
   which is t_{INT} = 20.00 msec. x 5
   = 100.00 msec. (for 50 Hz rejection)

   Therefore, using t_{INT} = 100 msec. would achieve both 50 Hz and 60 Hz cycle noise rejection. For this example, the following calculations would assume t_{INT} of 100 msec. Now select period equal to 0.5425 μsec. (clock frequency of 1.8432 MHz)

3. Pick $V_{IN}MAX = \pm 2V$

   For $I_B MAX = 20\mu A$, applying equation (4),

   $$R_{INT} = \frac{2}{20x10^{-6}} = 100\ K\Omega$$

4. Calculate, using equation (3) for C_{INT}:

   $$C_{INT} = (0.1) \times (20 \times 10^{-6}/4)$$
   $$\cong 0.5\ \mu F \qquad (\text{assume } V_{INT}MAX = 4V)$$

   Use C_{INT} 0.47μF as the closest practical value.

5. Pick C_{REF} and $C_{AZ} = 0.47\ \mu F$

6. Pick $t_{DINT} = 2 \times t_{INT} = 200$ msec.

7. Calculate the value for V_{REF}, from equation (10):

   $$V_{REF} = \frac{C_{INT} \cdot V_{INT}MAX \cdot R_{INT}}{t_{DINT}\ MAX}$$
   $$= \frac{0.5 \times 10^{-6} \times 4 \times 100 \times 10^{3}}{200 \times 10^{-3}}$$
   $$= 1.00V$$

Design Example 3:

1. Pick resolution of 18 bit. Total number of counts during t_{INT} is 262,144.

2. Pick t_{INT} = 16.66667 msec. x 10 cycles

   = 0.1666667 sec.

   This t_{INT} allows clock period of 0.5425 μsec. and still achieve 18 bits resolution.

3. Again, as shown from previous example, pick $V_{IN}MAX = \pm 2V$

   For $I_B MAX = 20\ \mu A$, $R_{INT} = \frac{2}{20x10^{-6}} = 100\ K\Omega$

4. Next, we calculate C_{INT}:

   $$C_{INT} = (0.1666667) \times (20 \times 10^{-6})/4$$
   $$\cong 0.83\ \mu F \qquad (V_{INT}MAX = 4.0V)$$

   In this case, use CINT = 1.0 μF to keep $V_{INT} < 4.0V$

5. Pick C_{REF} and $C_{AZ} = 1.0\ \mu F$

6. Select $t_{DINT} = 2 \times t_{INT} = 333.333$ msec.

7. Calculate V_{REF} as shown in the previous examples and $V_{REF} = 1.00V$

Design Example 4:
Objective: 5 1/2 digit + sign +over-range measurement.

1. Pick t_{INT} = 133.333 msec. for 60Hz noise rejection. (16.6667 msec. x 8 cycles)
   Frequency = 1.8432 MHz
   clock period = 0.5425 μsec.

   During Input Integrate Phase,

   $$\text{total count} = \frac{133.333 \times 10^{-3}}{0.5425 \times 10^{-6}}$$
   $$= 245776$$

   For $V_{INT} = 4.0V$, the basic resolution is

   $$\frac{4}{245776} \text{ or } 16.276\ \mu V/\text{count}$$

   For $V_{IN}MAX = 2.00V$, the input resolution is

   $$16.276 \times \frac{V_{IN}MAX}{V_{INT}MAX} = 8.138\ \mu V/\text{count}$$

2. Pick V_{IN} range = ± 2V

   For $I_B = 20\ \mu A$, $R_{INT} = \frac{2}{20 \times 10^{-6}} = 100\ K\Omega$

3. Calculate $C_{INT} = (0.133333) \times (20 \times 10^{-6})/4 \cong 0.67\ \mu F$

4. Pick $C_{REF} = C_{AZ} = 0.67\ \mu F$

5. Select $t_{DINT} = 2 \times t_{INT} = 266.667$ msec.

6. Calculate V_{REF} as shown in Design Example 1, substituting the appropriate values:

   $$V_{REF} = \frac{C_{INT} \cdot V_{INT}MAX \cdot R_{INT}}{t_{DINT}\ MAX}$$
   $$\cong 1.005V$$