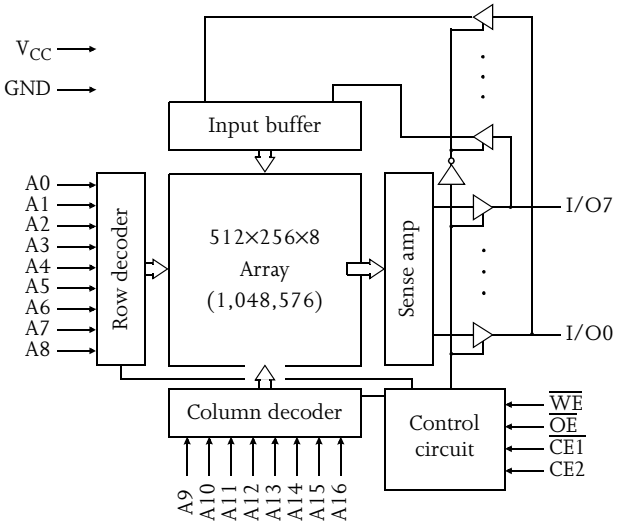
5V/3.3V 128KX8 CMOS SRAM (Evolutionary Pinout)

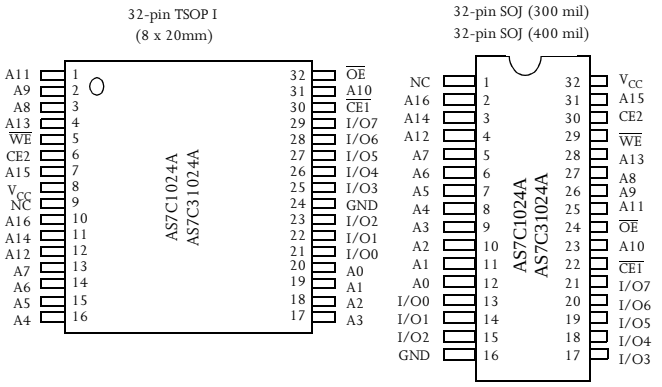
Features

- AS7C1024A (5V version)
- AS7C31024A (3.3V version)
- Industrial and commercial temperatures
- Organization: 131,012 words x 8 bits
- High speed
  - 10/12/15/20 ns address access time
  - 3/3/4/5 ns output enable access time
- Low power consumption: ACTIVE
  - 660 mW (AS7C1024A) / max @ 10 ns
  - 324 mW (AS7C31024A) / max @ 10 ns
- Low power consumption: STANDBY
  - 55 mW (AS7C1024A) / max CMOS
  - 36 mW (AS7C31024A) / max CMOS
- Latest 6T 0.25u CMOS technology
- 2.0V data retention
- Easy memory expansion with $\overline{CE1}$, CE2, $\overline{OE}$ inputs
- TTL/LVTTL-compatible, three-state I/O
- 32-pin JEDEC standard packages
  - 300 mil SOJ
  - 400 mil SOJ
  - 8 × 20mm TSOP I
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram



Pin arrangement



Selection guide

		AS7C1024A-10 AS7C31024A-10	AS7C1024A-12 AS7C31024A-12	AS7C1024A-15 AS7C31024A-15	AS7C1024A-20 AS7C31024A-20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		3	3	4	5	ns
Maximum operating current	ASAS7C1024A	120	110	100	100	mA
	AS7C31024A	90	80	80	80	mA
Maximum CMOS standby current	AS7C1024A	10	10	10	15	mA
	AS7C31024A	10	10	10	15	mA

Functional description

The AS7C1024A and AS7C31024A are high performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) devices organized as 131,012 words x 8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 3/3/4/5 ns are ideal for high performance applications. Active high and low chip enables ($\overline{CE1}$, CE2) permit easy memory expansion with multiple-bank systems.

When $\overline{CE1}$ is high or CE2 is low the devices enter standby mode. If inputs are still toggling, the device will consume I_{SB} power. If the bus is static, then full standby power is reached (I_{SB1}). For example, the AS7C31024A is guaranteed not to exceed 36mW under nominal full standby conditions. All devices in this family will retain data when VCC is reduced as low as 2.0V.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and both chip enables ($\overline{CE1}$, CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or the active-to-inactive edge of $\overline{CE1}$ or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and both chip enables ($\overline{CE1}$, CE2), with write enable ($\overline{WE}$) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable is inactive, output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

Absolute maximum ratings

Parameter		Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	AS7C1024A	V_{t1}	−0.50	+7.0	V
	AS7C31024A	V_{t1}	-0.50	+5.0	V
Voltage on any pin relative to GND	Both	V_{t2}	−0.50	V_{CC} +0.50	V
Power dissipation	Both	P_D	–	1.0	W
Storage temperature (plastic)	Both	T_{stg}	−65	+150	°C
Ambient temperature with V_{CC} applied	Both	T_{bias}	−55	+125	°C
DC current into outputs (low)	Both	I_{OUT}	–	20	mA

Note: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby (I_{SB}, I_{SB1})
X	L	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	H	High Z	Output disable (I_{CC})
L	H	H	L	D_{OUT}	Read (I_{CC})
L	H	L	X	D_{IN}	Write ($_{ICC}$)

Key: X = Don't Care, L = Low, H = High

Recommended operating conditions

Parameter	Device	Symbol	Min	Nominal	Max	Unit
Supply voltage	AS7C1024A	V_{CC}	4.5	5.0	5.5	V
	AS7C31024A	V_{CC}	3.0	3.3	3.6	V
Input voltage	ASAS7C1024A	V_{IH}	2.2	–	V_{CC} + 0.5	V
	AS7C31024A	V_{IH}	2.0	–	V_{CC} + 0.5	V
		V_{IL}†	–0.5	–	0.8	V
Ambient operating temperature	commercial	T_A	0	–	70	°C
	industrial	T_A	–40	–	85	°C

† V_{IL}min. = –3.0V for pulse width less than $t_{RC/2}$.

DC operating characteristics (over the operating range)[1]

Parameter	Sym	Test conditions	Device	-10		-12		-15		-20		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$\|I_{LI}\|$	V_{CC} = Max, V_{IN} = GND to V_{CC}	Both	–	1	–	1	–	1	–	1	µA
Output leakage current	$\|I_{LO}\|$	V_{CC} = Max, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{OUT} = GND to V_{CC}	Both	–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	V_{CC} = Max, $\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, f = f_{Max}, I_{OUT} = 0 mA	AS7C1024A	–	120	–	110	–	100	–	100	mA
			AS7C31024A	–	90	–	80	–	80	–	80	
Standby power supply current	I_{SB}	V_{CC} = Max, $\overline{CE1}$ ≥ V_{IH} and/or CE2 ≤ V_{IL}, V_{IN} = V_{IH} or V_{IL}, f = f_{Max}, I_{OUT} = 0mA	AS7C1024A	–	30	–	25	–	20	–	20	mA
			AS7C31024A	–	30	–	25	–	20	–	20	
	I_{SB1}	V_{CC} = Max, $\overline{CE1}$ ≥ V_{CC}–0.2V V_{IN} ≤ GND + 0.2V or V_{IN} ≥ V_{CC} –0.2V, f = 0	AS7C1024A	–	10	–	10	–	10	–	15	mA
			AS7C31024A	–	10	–	10	–	10	–	15	
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min		–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min		2.4	–	2.4	–	2.4	–	2.4	–	V
Data retention current	ICCDR	V_{CC} = 2.0V $\overline{CE1}$ ≥ V_{CC}–0.2V or CE2 ≤ 0.2V V_{IN} ≥ V_{CC}–0.2V or V_{IN} ≤ 0.2V	AS7C1024A	-	1	-	1	-	1	-	5	mA
			AS7C31024A	-	1	-	1	-	1	-	5	mA

Capacitance (f = 1 MHz, T_a = 25 °C, V_{CC} = NOMINAL)[2]

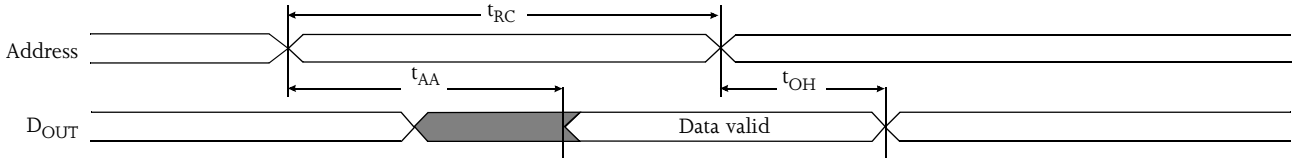
Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE1}$, CE2, $\overline{WE}$, $\overline{OE}$	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	7	pF

Read cycle (over the operating range)[3,9,12]

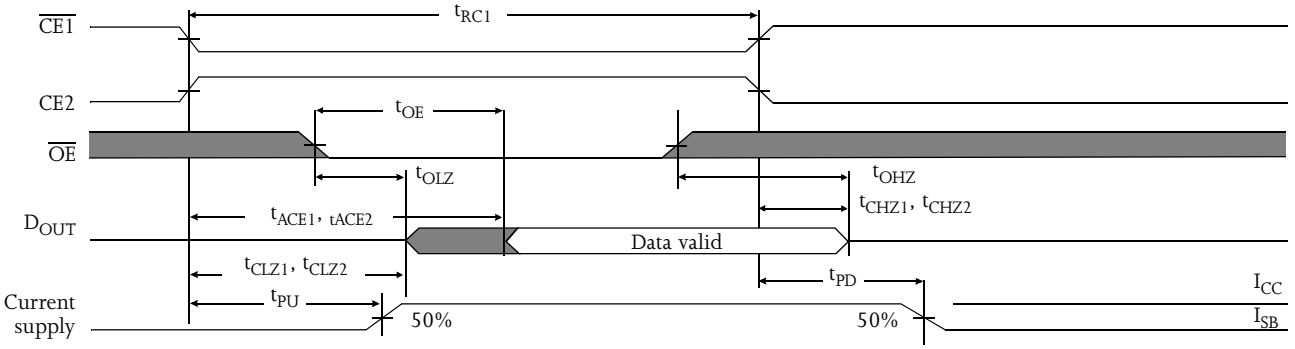
Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	3
Chip enable ($\overline{CE1}$) access time	t_{ACE1}	–	10	–	12	–	15	–	20	ns	3, 12
Chip enable (CE2) access time	t_{ACE2}	–	10	–	12	–	15	–	20	ns	3, 12
Output enable ($\overline{OE}$) access time	t_{OE}	–	3	–	3	–	4	–	5	ns	
Output hold from address change	t_{OH}	2	–	3	–	3	–	3	–	ns	5
$\overline{CE1}$ Low to output in low Z	t_{CLZ1}	0	–	0	–	0	–	0	–	ns	4, 5, 12
CE2 High to output in low Z	t_{CLZ2}	0	–	0	–	0	–	0	–	ns	4, 5, 12
$\overline{CE1}$ Low to output in high Z	t_{CHZ1}	–	3	–	3	–	4	–	5	ns	4, 5, 12
CE2 Low to output in high Z	t_{CHZ2}	–	3	–	3	–	4	–	5	ns	4, 5, 12
$\overline{OE}$ Low to output in low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ High to output in high Z	t_{OHZ}	–	3	–	3	–	4	–	5	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5, 12
Power down time	t_{PD}	–	10	–	12	–	15	–	20	ns	4, 5, 12

Key to switching waveforms

Read waveform 1 (address controlled)[3,6,7,9,12]



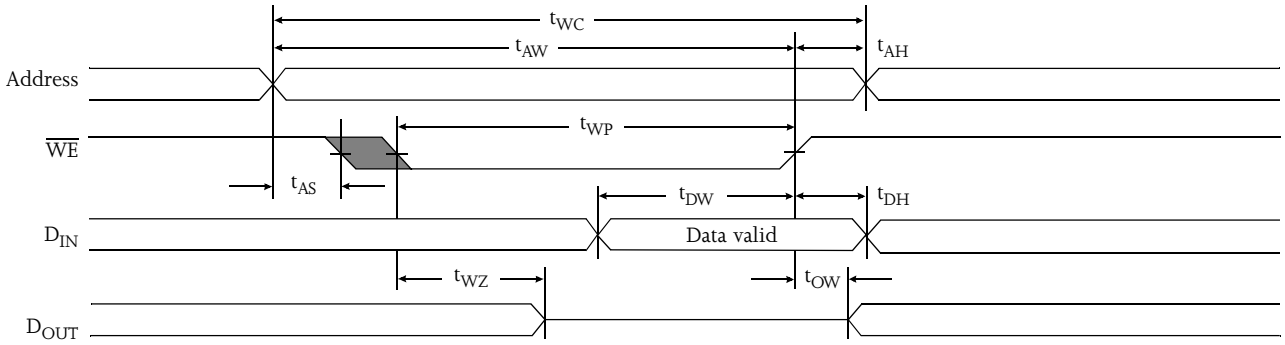
Read waveform 2 ($\overline{CE1}$, CE2, and $\overline{OE}$ controlled)[3,6,8,9,12]



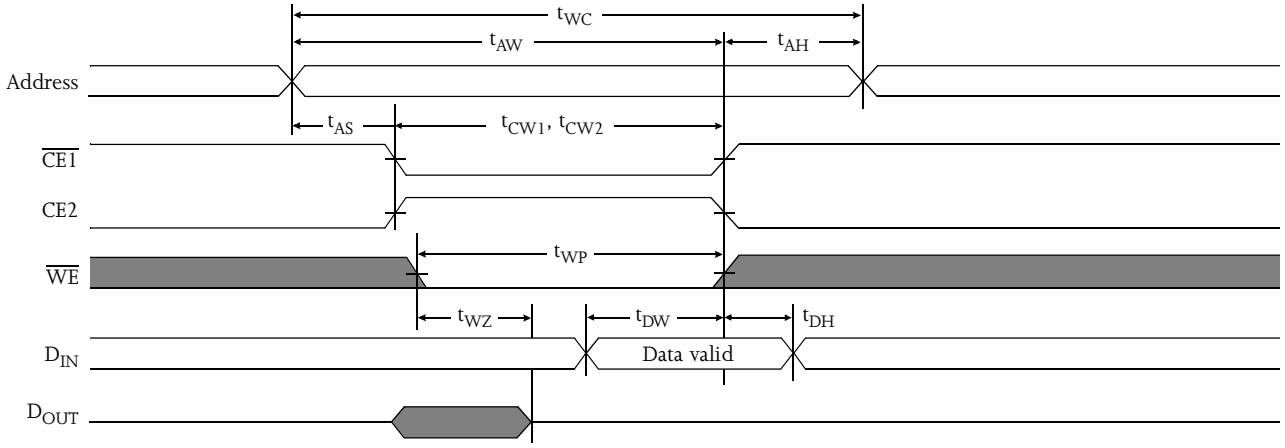
Write cycle (over the operating range)[11, 12]

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10	–	12	–	15	–	20	–	ns	
Chip enable ($\overline{CE1}$) to write end	t_{CW1}	8	–	10	–	12	–	12	–	ns	12
Chip enable (CE2) to write end	t_{CW2}	8	–	10	–	12	–	12	–	ns	12
Address setup to write end	t_{AW}	8	–	9	–	10	–	12	–	ns	
Address setup time	t_{AS}	0	–	0	–	0	–	0	–	ns	12
Write pulse width	t_{WP}	7	–	8	–	9	–	12	–	ns	
Address hold from end of write	t_{AH}	0	–	0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5	–	6	–	8	–	10	–	ns	
Data hold time	t_{DH}	0	–	0	–	0	–	0	–	ns	4, 5
Write enable to output in high Z	t_{WZ}	–	6	–	6	–	6	–	8	ns	4, 5
Output active from write end	t_{OW}	1	–	1	–	1	–	2	–	ns	4, 5

Write waveform 1 ($\overline{WE}$ controlled)[10,11,12]



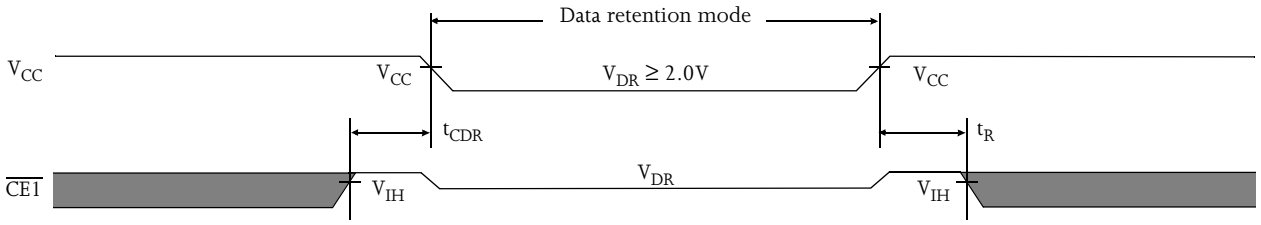
Write waveform 2 ($\overline{CE1}$ and CE2 controlled)[10,11,12]



Data retention characteristics (over the operating range)

Parameter	Symbol	Test conditions	Device	Min	Max	Unit
V_{CC} for data retention	VDR	V_{CC} = 2.0V $\overline{CE1} \geq V_{CC}-0.2V$ or CE2 ≤ 0.2V $V_{IN} \geq V_{CC}-0.2V$ or $V_{IN} \leq 0.2V$		2.0	–	V
Chip deselect to data retention time	tCDR			0	–	ns
Operation recovery time	tR			t_{RC}	–	ns
Input leakage current	| ILI |			–	1	µA

Data retention waveform



AC test conditions

- Output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

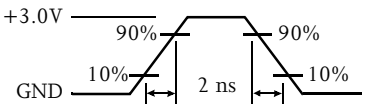


Figure A: Input pulse

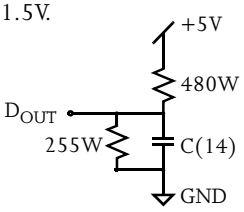


Figure B: 5V Output load

Thevenin equivalent:

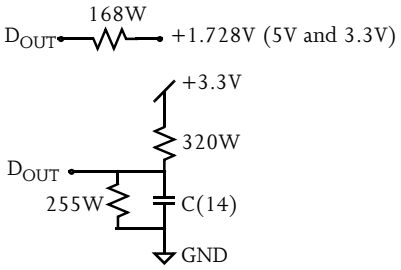
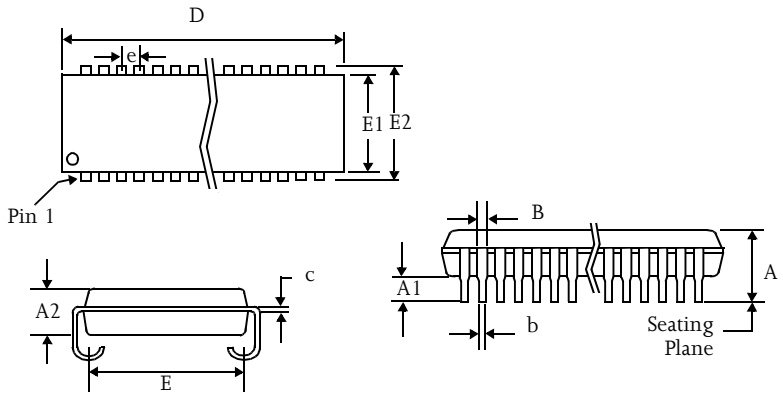


Figure C: 3.3V Output load

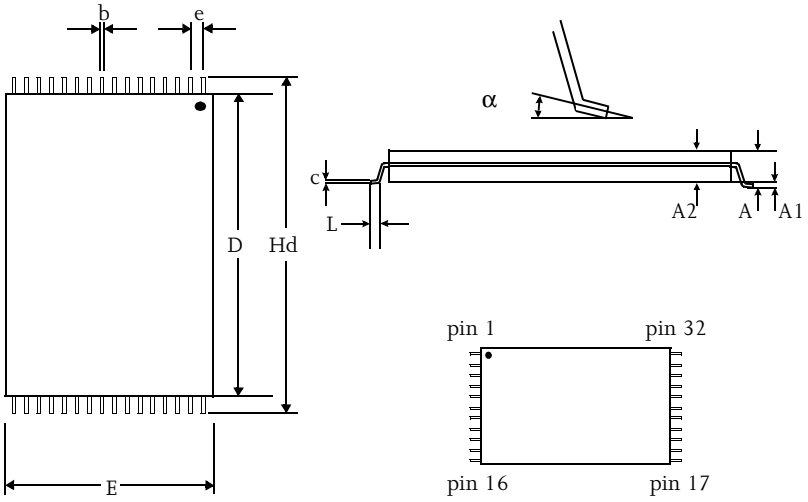
Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE1}$ is required to meet I_{SB} specification.
2 This parameter is sampled and not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, and C.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5pF, as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed, but not 100% tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE1}$ and $\overline{OE}$ are Low and CE2 is High for read cycle.
8 Address valid prior to or coincident with $\overline{CE1}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE1}$ or $\overline{WE}$ must be High or CE2 Low during address transitions. Either $\overline{CE1}$ or $\overline{WE}$ asserting high terminates a write cycle.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 $\overline{CE1}$ and CE2 have identical timing.
13 C=30pF, except all high Z and low Z parameters, C=5pF.

Package dimensions



	32-pin SOJ 300 mil		32-pin SOJ 400 mil	
	Min	Max	Min	Max
A	-	0.145	-	0.145
A1	0.025	-	0.025	-
A2	0.086	0.105	0.086	0.115
B	0.026	0.032	0.026	0.032
b	0.014	0.020	0.015	0.020
c	0.006	0.013	0.007	0.013
D	0.820	0.830	0.820	0.830
E	0.250	0.275	0.360	0.380
E1	0.292	0.305	0.395	0.405
E2	0.330	0.340	0.435	0.445
e	0.050 BSC		0.050 BSC	



	32-pin TSOP 8×20 mm	
	Min	Max
A	–	1.20
A1	0.05	0.15
A2	0.95	1.05
b	0.17	0.27
c	0.10	0.21
D	18.20	18.60
e	0.50 nominal	
E	7.80	8.20
Hd	19.80	20.20
L	0.50	0.70
α	0°	5°

Ordering codes

Package \ Access time	Volt/Temp	10 ns	12 ns	15 ns	20 ns
Plastic SOJ, 300 mL	5V commercial	AS7C1024A-10TJC	AS7C1024A-12TJC	AS7C1024A-15TJC	AS7C1024A-20TJC
	5V industrial	AS7C1024A-10TJI	AS7C1024A-12TJI	AS7C1024A-15TJI	AS7C1024A-20TJI
	3.3V commercial	AS7C31024A-10TJC	AS7C31024A-12TJC	AS7C31024A-15TJC	AS7C31024A-20TJC
	3.3V industrial	AS7C31024A-10TJI	AS7C31024A-12TJI	AS7C31024A-15TJI	AS7C31024A-20TJI
Plastic SOJ, 400 mL	5V commercial	AS7C1024A-10JC	AS7C1024A-12JC	AS7C1024A-15JC	AS7C1024A-20JC
	5V industrial	AS7C1024A-10JI	AS7C1024A-12JI	AS7C1024A-15JI	AS7C1024A-20JI
	3.3V commercial	AS7C31024A-10JC	AS7C31024A-12JC	AS7C31024A-15JC	AS7C31024A-20JC
	3.3V industrial	AS7C31024A-10JI	AS7C31024A-12JI	AS7C31024A-15JI	AS7C31024A-20JI
TSOP 8×20	5V commercial	AS7C1024A-10TC	AS7C1024A-12TC	AS7C1024A-15TC	AS7C1024A-20TC
	5V industrial	AS7C1024A-10TI	AS7C1024A-12TI	AS7C1024A-15TI	AS7C1024A-20TI
	3.3V commercial	AS7C31024A-10TC	AS7C31024A-12TC	AS7C31024A-15TC	AS7C31024A-20TC
	3.3V industrial	AS7C31024A-10TI	AS7C31024A-12TI	AS7C31024A-15TI	AS7C31024A-20TI

Part numbering system

AS7C	X	1024	–XX	X	X
SRAM prefix	Blank=5V CMOS 3=3.3V CMOS	Device number	Access time	Package:T=TSOP 8×20 J=SOJ 400 mil TJ=SOJ 300 mil	Temperature range C = Commercial, 0°C to 70°C I = Industrial, -40°C to 85°C