



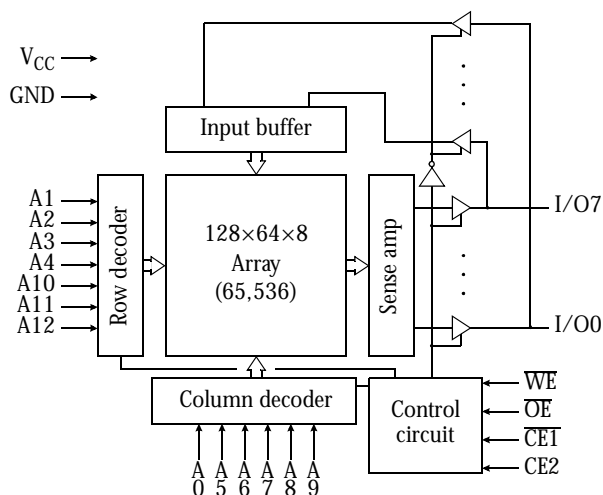
5V 8Kx8 CMOS SRAM

Features

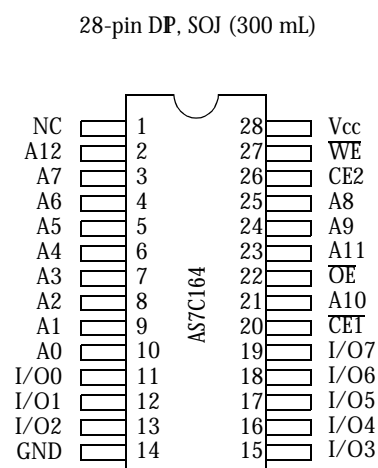
- AS7C164 (5V version)
- Commercial temperatur
- Organization: 8,192 words × 8 bits
- Center power and ground pins
- High speed
  - 12/15/20 ns address access time
  - 3/4/5 ns output enable access time
- Low power consumption: ACTIVE
  - 550 mW (AS7C164) / max @ 12 ns
- Low power consumption: STANDBY
  - 11 mW (AS7C164) / max CMOS I/O
- 2.0V data retention
- Easy memory expansion with  $\overline{CE1}$ ,  $CE2$ ,  $\overline{OE}$  inputs
- TTL-compatible, three-state I/O
- 28-pin JEDEC standard package
  - 300 mil PDIP and SOJ
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

SRAM

Logic block diagram



Pin arrangement



Selection guide

	AS7C164-12	AS7C164-15	AS7C164-20	Unit
Maximum address access time	12	15	20	ns
Maximum output enable access time	3	4	5	ns
Maximum operating current	110	100	90	mA
Maximum CMOS standby current	2.0	2.0	2.0	mA



## Functional description

The AS7C164 is a high performance CMOS 65,536-bit Static Random Access Memory (SRAM) device organized as 8,192 words  $\times$  8 bits. It is designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times ( $t_{AA}$ ,  $t_{RC}$ ,  $t_{WC}$ ) of 12/15/20 ns with output enable access times ( $t_{OE}$ ) of 3/4/5 ns are ideal for high performance applications. Active high and low chip enables ( $\overline{CE1}$ , CE2) permit easy memory expansion with multiple-bank memory systems.

When  $\overline{CE1}$  is High or CE2 is Low the device enters standby mode. The standard AS7C164 is guaranteed not to exceed 11.0 mW power consumption in standby mode, and typically requires only 250  $\mu$ W; it offers 2.0V data retention with maximum power of 120  $\mu$ W.

A write cycle is accomplished by asserting write enable ( $\overline{WE}$ ) and both chip enables ( $\overline{CE1}$ , CE2). Data on the input pins I/O0-I/O7 is written on the rising edge of  $\overline{WE}$  (write cycle 1) or the active-to-inactive edge of  $\overline{CE1}$  or CE2 (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ( $\overline{OE}$ ) or write enable ( $\overline{WE}$ ).

A read cycle is accomplished by asserting output enable ( $\overline{OE}$ ) and both chip enables ( $\overline{CE1}$ , CE2), with write enable ( $\overline{WE}$ ) High. The chip drives I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply. The AS7C164 is packaged in all high volume industry standard packages.

## Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on $V_{CC}$ relative to GND	AS7C164	$V_{t1}$	-0.50	+7.0	V
Voltage on any pin relative to GND		$V_{t2}$	-0.50	$V_{CC} + 0.50$	V
Power dissipation		$P_D$	-	1.0	W
Storage temperature (plastic)		$T_{stg}$	-65	+150	$^{\circ}$ C
Ambient temperature with $V_{CC}$ applied		$T_{bias}$	-55	+125	$^{\circ}$ C
DC current into outputs (low)		$I_{out}$	-	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Truth table

$\overline{CE1}$	CE2	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
X	L	X	X	High Z	Standby ( $I_{SB}$ , $I_{SB1}$ )
L	H	H	H	High Z	Output disable ( $I_{CC}$ )
L	H	H	L	$D_{out}$	Read ( $I_{CC}$ )
L	H	L	X	$D_{in}$	Write ( $I_{CC}$ )

Key: X = Don't Care, L = Low, H = High



### Recommended operating conditions

Parameter	Device	Symbol	Min	Typical	Max	Unit
Supply voltage	AS7C164	$V_{CC}$	4.5	5.0	5.5	V
Input voltage	AS7C164	$V_{IH}$	2.2	–	$V_{CC}+1$	V
		$V_{IL}$	-0.5*	–	0.8	V
Ambient operating temperature	AS7C164	$T_A$	0	–	70	°C

\*  $V_{IL}$  min = -3.0V for pulse width less than  $t_{RC}/2$ .

### DC operating characteristics (over the operating range)<sup>1</sup>

Parameter	Symbol	Test Conditions	Device	-12		-15		-20		Unit
				Min	Max	Min	Max	Min	Max	
Input leakage current	$ I_{LI} $	$V_{CC} = \text{Max},$ $V_{IN} = \text{GND to } V_{CC}$		–	1	–	1	–	1	$\mu\text{A}$
Output leakage current	$ I_{LO} $	$V_{CC} = \text{Max},$ $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL},$ $V_{OUT} = \text{GND to } V_{CC}$		–	1	–	1	–	1	$\mu\text{A}$
Operating power supply current	$I_{CC}$	$V_{CC} = \text{Max},$ $\overline{CE1} = V_{IL}, CE2 = V_{IH},$ $f = f_{\text{Max}}, I_{OUT} = 0 \text{ mA}$	AS7C164	–	110	–	100	–	90	mA
Standby power supply current	$I_{SB}$	$V_{CC} = \text{Max},$ $\overline{CE1} = V_{IH}$ or $CE2 = V_{IL},$ $f = f_{\text{Max}}$	AS7C164	–	30	–	25	–	25	mA
	$I_{SB1}$	$V_{CC} = \text{Max},$ $\overline{CE1} \geq V_{CC}-0.2\text{V}$ or $CE2 \leq 0.2\text{V},$ $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC}-0.2\text{V}, f = 0$	AS7C164	–	2.0	–	2.0	–	2.0	mA
Output voltage	$V_{OL}$	$I_{OL} = 8 \text{ mA}, V_{CC} = \text{Min}$		–	0.4	–	0.4	–	0.4	V
	$V_{OH}$	$I_{OH} = -4 \text{ mA}, V_{CC} = \text{Min}$		2.4	–	2.4	–	2.4	–	V

### Capacitance ( $f=1\text{MHz}, T_a=25^\circ\text{C}, V_{CC} = \text{NOMINAL}$ )<sup>2</sup>

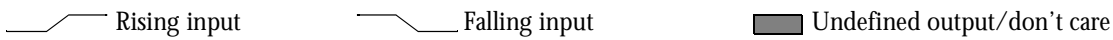
Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	$C_{IN}$	A, $\overline{CE1}$ , CE2, WE, OE	$V_{in} = 0\text{V}$	5	pF
I/O capacitance	$C_{I/O}$	I/O	$V_{in} = V_{out} = 0\text{V}$	7	pF



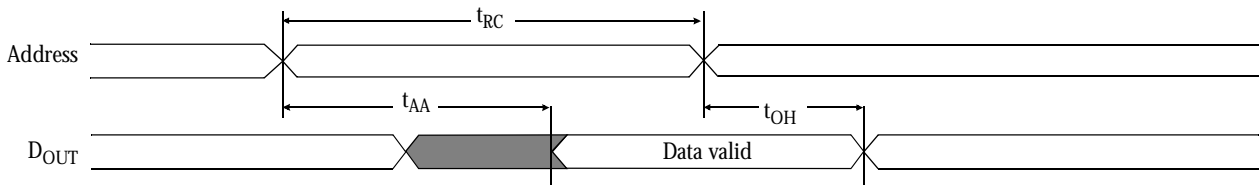
Read cycle (over the operating range)<sup>3,9</sup>

Parameter	Symbol	-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Read cycle time	$t_{RC}$	12	-	15	-	20	-	ns	
Address access time	$t_{AA}$	-	12	-	15	-	20	ns	3
Chip enable ( $\overline{CE1}$ ) access time	$t_{ACE1}$	-	12	-	15	-	20	ns	3, 12
Chip enable (CE2) access time	$t_{ACE2}$	-	12	-	15	-	20	ns	3, 12
Output enable ( $\overline{OE}$ ) access time	$t_{OE}$	-	3	-	4	-	5	ns	
Output hold from address change	$t_{OH}$	3	-	3	-	3	-	ns	5
$\overline{CE1}$ Low to output in low Z	$t_{CLZ1}$	3	-	3	-	3	-	ns	4, 5, 12
CE2 High to output in low Z	$t_{CLZ2}$	3	-	3	-	3	-	ns	4, 5, 12
$\overline{CE1}$ High to output in high Z	$t_{CHZ1}$	-	3	-	4	-	5	ns	4, 5, 12
CE2 Low to output in high Z	$t_{CHZ2}$	-	3	-	4	-	5	ns	4, 5, 12
$\overline{OE}$ Low to output in low Z	$t_{OLZ}$	0	-	0	-	0	-	ns	4, 5
$\overline{OE}$ High to output in high Z	$t_{OHZ}$	-	3	-	4	-	5	ns	4, 5
Power up time	$t_{PU}$	0	-	0	-	0	-	ns	4, 5, 12
Power down time	$t_{PD}$	-	12	-	15	-	20	ns	4, 5, 12

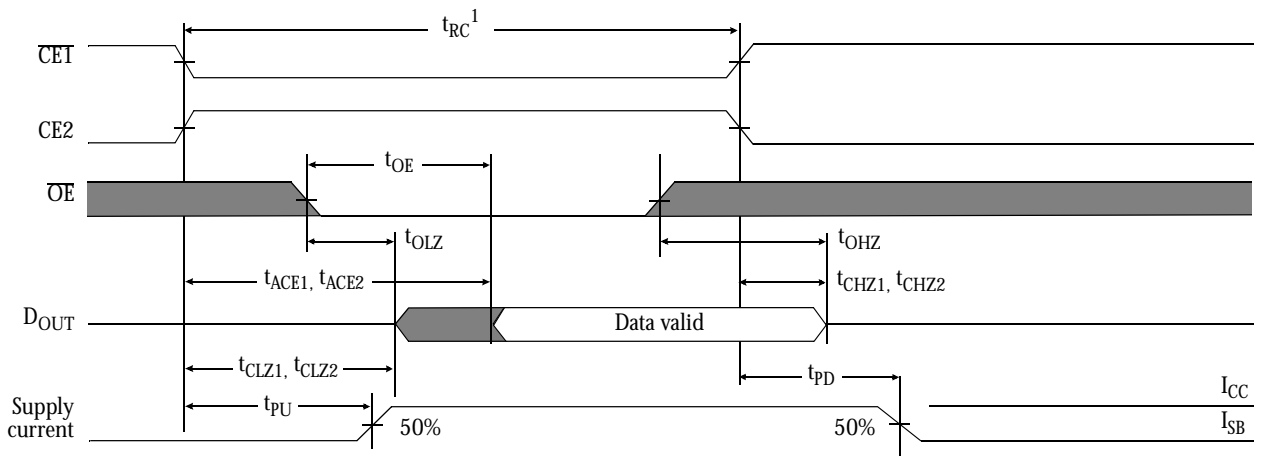
Key to switching waveforms



Read waveform 1 (address controlled)<sup>3, 6, 7, 9, 12</sup>

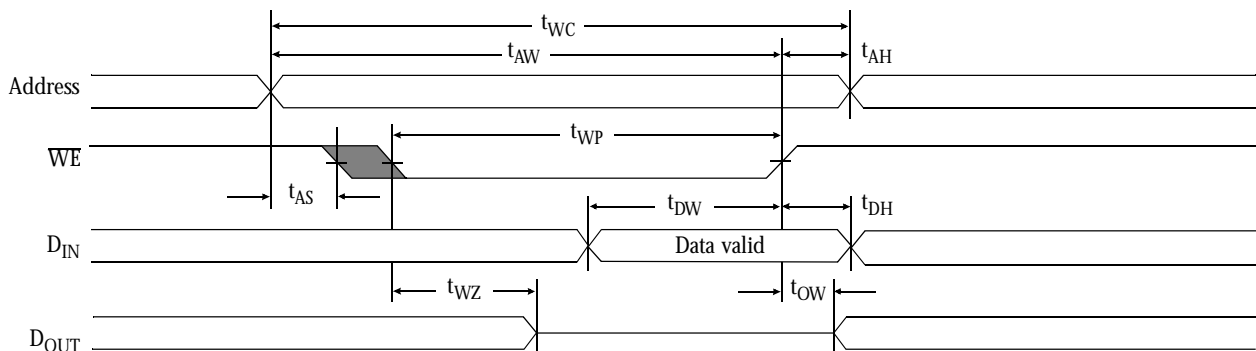
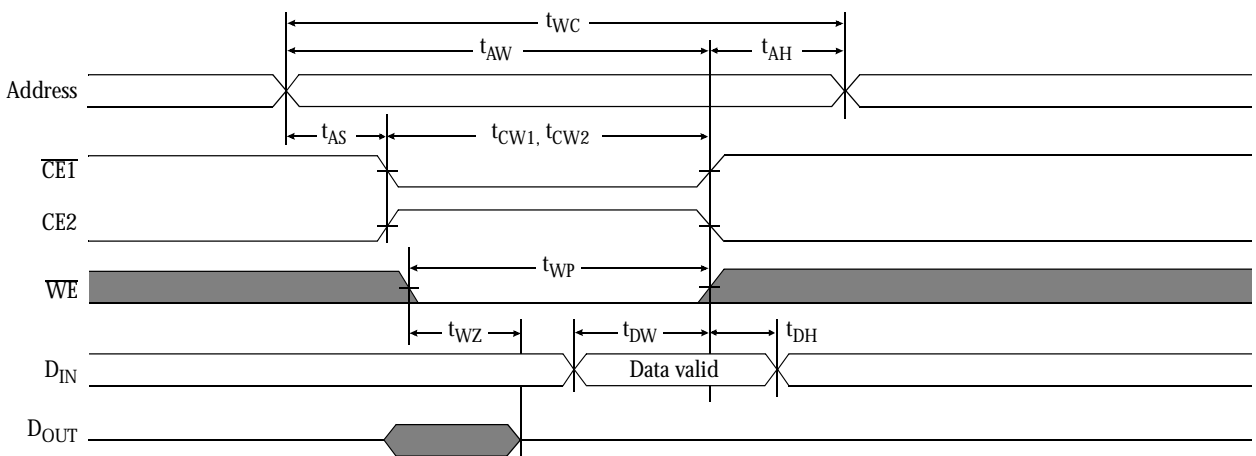


Read waveform 2 ( $\overline{CE1}$  and CE2 controlled)<sup>3, 6, 8, 9, 12</sup>



Write cycle (over the operating range)<sup>11</sup>

Parameter	Symbol	-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max		
Write cycle time	$t_{WC}$	12	–	15	–	20	–	ns	
Chip enable ( $\overline{CE1}$ ) to write end	$t_{CW1}$	9	–	10	–	12	–	ns	12
Chip enable ( $\overline{CE2}$ ) to write end	$t_{CW2}$	9	–	10	–	12	–	ns	12
Address setup to write end	$t_{AW}$	9	–	10	–	12	–	ns	
Address setup time	$t_{AS}$	0	–	0	–	0	–	ns	12
Write pulse width	$t_{WP}$	8	–	9	–	12	–	ns	
Address hold from write end	$t_{AH}$	0	–	0	–	0	–	ns	
Data valid to write end	$t_{DW}$	6	–	7	–	8	–	ns	
Data hold time	$t_{DH}$	0	–	0	–	0	–	ns	4, 5
Write enable to output in high Z	$t_{WZ}$	–	5	–	5	–	5	ns	4, 5
Output active from write end	$t_{OW}$	3	–	3	–	3	–	ns	4, 5

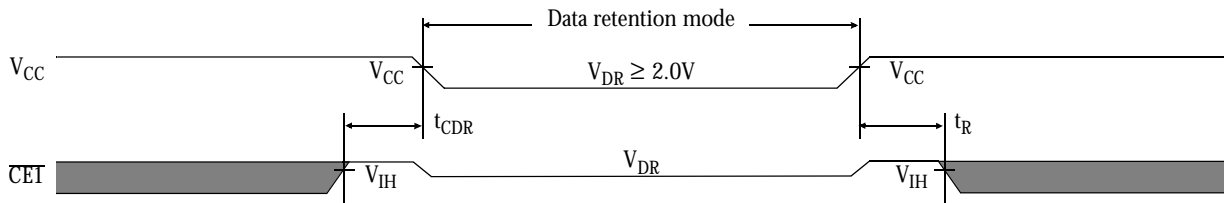
Write waveform 1 ( $\overline{WE}$  controlled)<sup>10, 11, 12</sup>Write waveform 2 ( $\overline{CE1}$  and  $\overline{CE2}$  controlled)<sup>10, 11, 12</sup>



Data retention characteristics (over the operating range)<sup>13</sup>

Parameter	Symbol	Test conditions	Min	Max	Unit
V <sub>CC</sub> for data retention	V <sub>DR</sub>	V <sub>CC</sub> = 2.0V $\overline{CE1} \geq V_{CC} - 0.2V$ or CE2 ≤ 0.2V	2.0	–	V
Data retention current	I <sub>CCDR</sub>		–	60	μA
Chip enable to data retention time	t <sub>CDR</sub>		0	–	ns
Operation recovery time	t <sub>R</sub>		t <sub>RC</sub>	–	ns

Data retention waveform



AC test conditions

- Output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

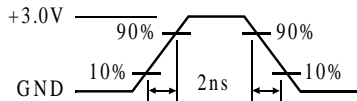


Figure A: Input pulse

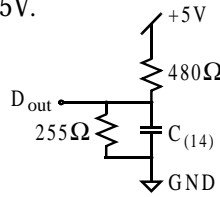


Figure B: 5V Output load

Thevenin Equivalent:  
 D<sub>out</sub> ← 168Ω → +1.728V (5V)

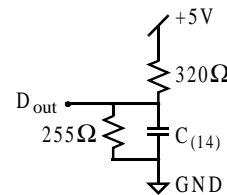


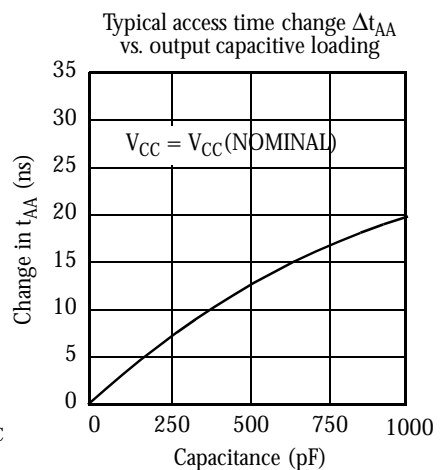
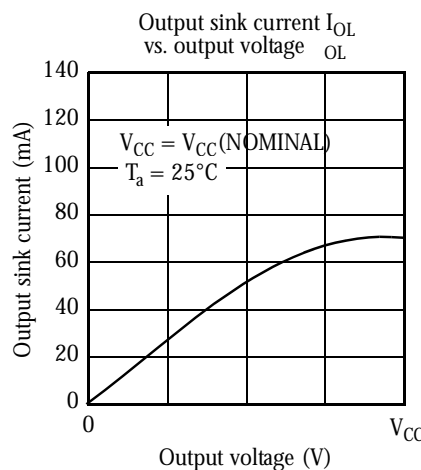
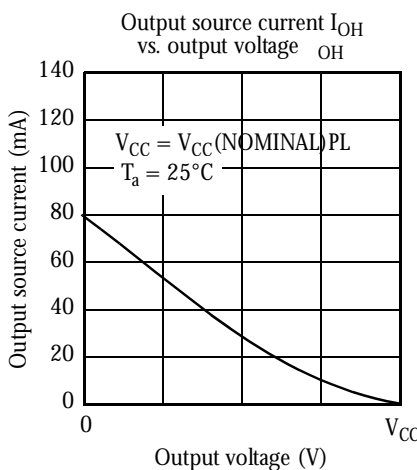
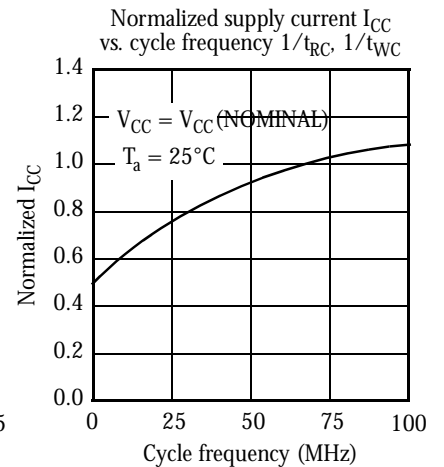
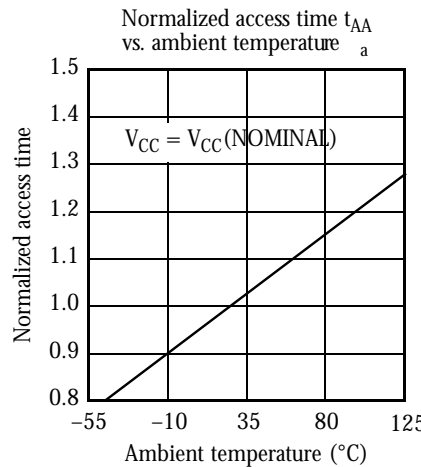
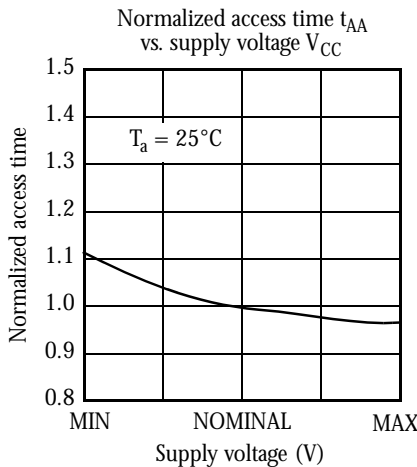
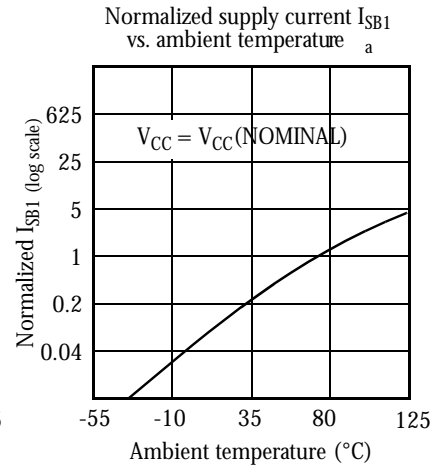
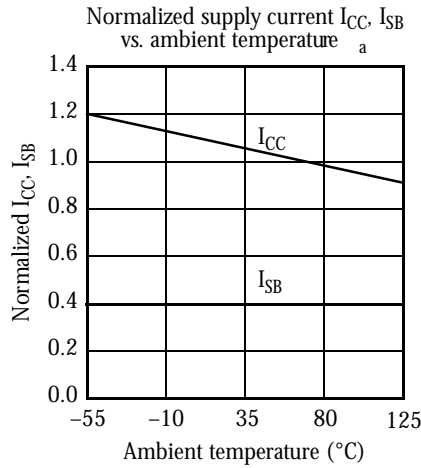
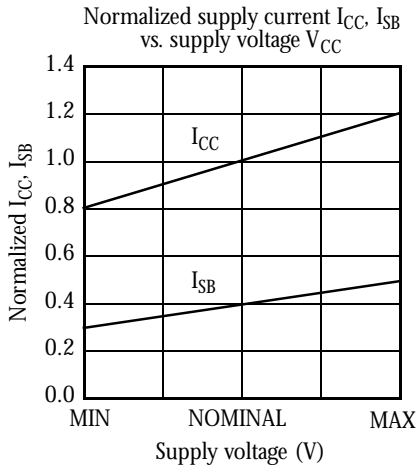
Figure C: 3.3V Output load

Notes

- 1 During V<sub>CC</sub> power-up, a pull-up resistor to V<sub>CC</sub> on  $\overline{CE1}$  is required to meet I<sub>SB</sub> specification.
- 2 This parameter is sampled, but not 100% tested.
- 3 For test conditions, see AC Test Conditions, Figures A, B, and C.
- 4 t<sub>CLZ</sub> and t<sub>CHZ</sub> are specified with CL = 5pF as in Figures B or C. Transition is measured ±500mV from steady-state voltage.
- 5 This parameter is guaranteed, but not 100% tested.
- 6 WE is High for read cycle.
- 7  $\overline{CE1}$  and OE are Low and CE2 is High for read cycle.
- 8 Address valid prior to or coincident with  $\overline{CE1}$  transition Low and CE2 transition High.
- 9 All read cycle timings are referenced from the last valid address to the first transitioning address.
- 10  $\overline{CE1}$  or WE must be High or CE2 Low during address transitions. Either  $\overline{CE}$  or WE asserting high terminates a write cycle.
- 11 All write cycle timings are referenced from the last valid address to the first transitioning address.
- 12  $\overline{CE1}$  and CE2 have identical timing.
- 13 2V data retention applies to the commercial operating range only.
- 14 C = 30pF, except on High Z and Low Z parameters, where C = 5pF.



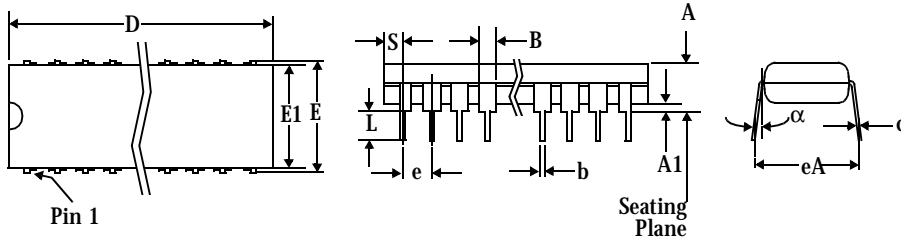
Typical DC and AC characteristics



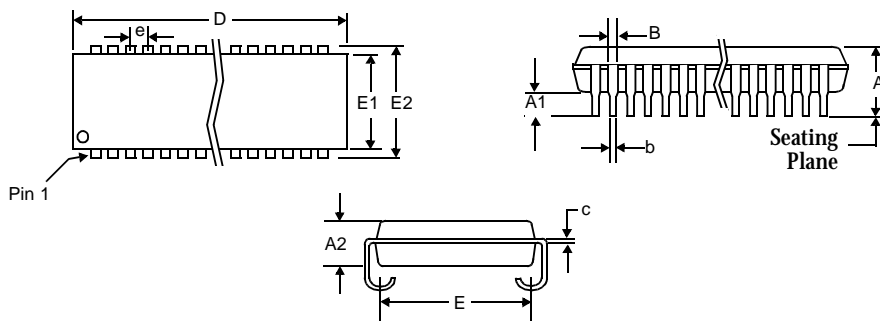


Package dimensions

SRAM



	28-pin PDIP	
	Min	Max
A	-	0.175
A1	0.010	-
B	0.058	0.064
b	0.016	0.022
c	0.008	0.014
D	-	1.400
E	0.295	0.320
E1	0.278	0.298
e	0.100 BSC	
eA	0.330	0.370
L	0.120	0.140
$\alpha$	0°	15°
S	-	0.055



	28-pin SOJ	
	Min	Max
A	-	0.140
A1	0.025	-
A2	0.095	0.105
B	0.028 TYP	
b	0.018 TYP	
c	0.010 TYP	
D	-	0.730
E	0.245	0.285
E1	0.295	0.305
E2	0.327	0.347
e	0.050 BSC	

Ordering codes

Package\ Access time	Volt/Temp	12 ns	15 ns	20 ns
Plastic DIP\300 mL	5V commercial	AS7C164-12PC	AS7C164-15PC	AS7C164-20PC
Plastic SOJ\300 mL	5V commercial	AS7C164-12JC	AS7C164-15JC	AS7C164-20JC

Part numbering system

AS7C	164	X	-XX	X	C
SRAM prefix	Device number	Blank = Standard power	Access time	Package code: P=PDIP 300 mil J=SOJ 300 mil	Commercial temperature range, 0°C to 70°C