SUPPLEMENT

Am29F200A Known Good Die

2 Megabit (256 K x 8-Bit/128 K x 16-Bit) CMOS 5.0 Volt-only, Sectored Flash Memory—Die Revision 1

DISTINCTIVE CHARACTERISTICS

- **5.0 V ± 10% for read and write operations**
  - — Minimizes system level power requirements
- **High performance**
  - — 90 or 120 ns access time
- **Low power consumption**
  - — 20 mA typical active read current (byte mode)
  - — 28 mA typical active read current for (word mode)
  - — 30 mA typical program/erase current
  - — 1 µA typical standby current
- **Sector erase architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and three 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and three 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 100,000 write/erase cycles guaranteed**
- **Compatible with JEDEC standards**
  - — Pinout and software compatible with single-power-supply flash
  - — Superior inadvertent write protection
- **Data# Polling and Toggle Bit**
  - — Detects program or erase cycle completion
- **Ready/Busy# output (RY/BY#)**
  - — Hardware method for detection of program or erase cycle completion
- **Erase Suspend/Resume**
  - — Supports reading data from a sector not being erased
- **Hardware RESET# pin**
  - — Resets internal state machine to the reading array data
- **Tested to datasheet specifications at temperature**
- **Quality and reliability levels equivalent to standard packaged components**

Publication# **21257** Rev: **B** Amendment/**0**
Issue Date: **December 1997**

GENERAL DESCRIPTION

The Am29F200A in Known Good Die (KGD) form is a 2 Mbit, 5.0 Volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29F200A Features

The Am29F200A is organized as 262,144 bytes of 8 bits each or 131,072 words of 16 bits each. The 8-bit data appears on DQ0-DQ7; the 16-bit data appears on DQ0-DQ15. This device is designed to be programmed in-system with the standard system 5.0 Volt V_{CC} supply. A 12.0 volt V_{PP} is not required for program or erase operations.

The standard Am29F200A in KGD form offers an access time of 90 or 120 ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#), and output enable (OE#) controls.

The device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6/DQ2 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The system can place the device into the **standby mode**. Power consumption is greatly reduced in this mode.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

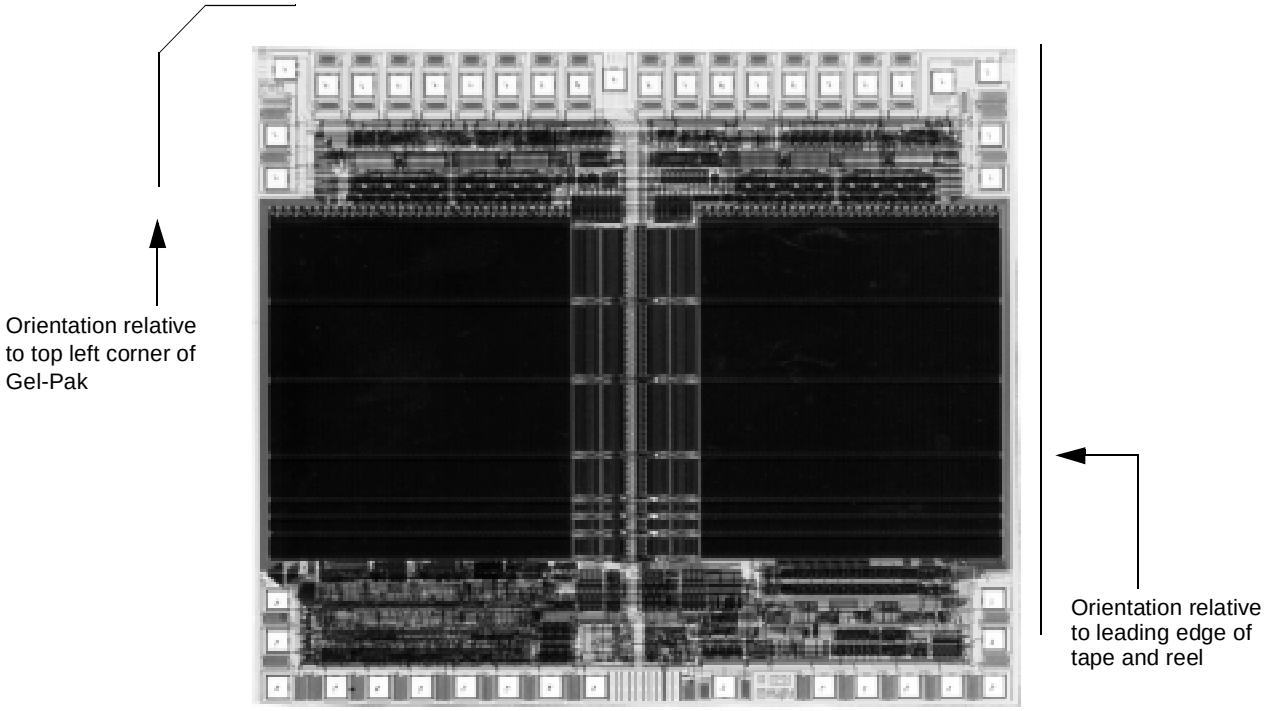
ELECTRICAL SPECIFICATIONS

Refer to the Am29F200A data sheet, publication number 20380, for full electrical specifications on the Am29F200A.

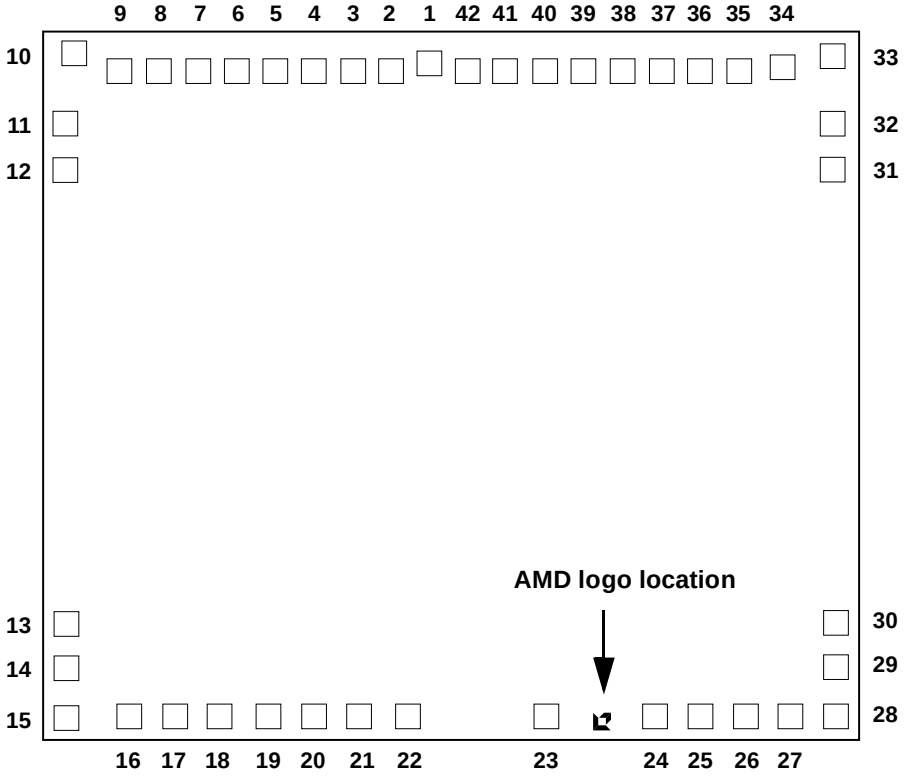
PRODUCT SELECTOR GUIDE

Family Part Number	**Am29F200A KGD**	
Speed Option (V_{CC} = 5.0 V ± 10%)	**-90**	**-120**
Max access time, ns (t_{ACC})	90	120
Max CE# access time, ns (t_{CE})	90	120
Max OE# access time, ns (t_{OE})	35	50

DIE PHOTOGRAPH



DIE PAD LOCATIONS



PAD DESCRIPTION

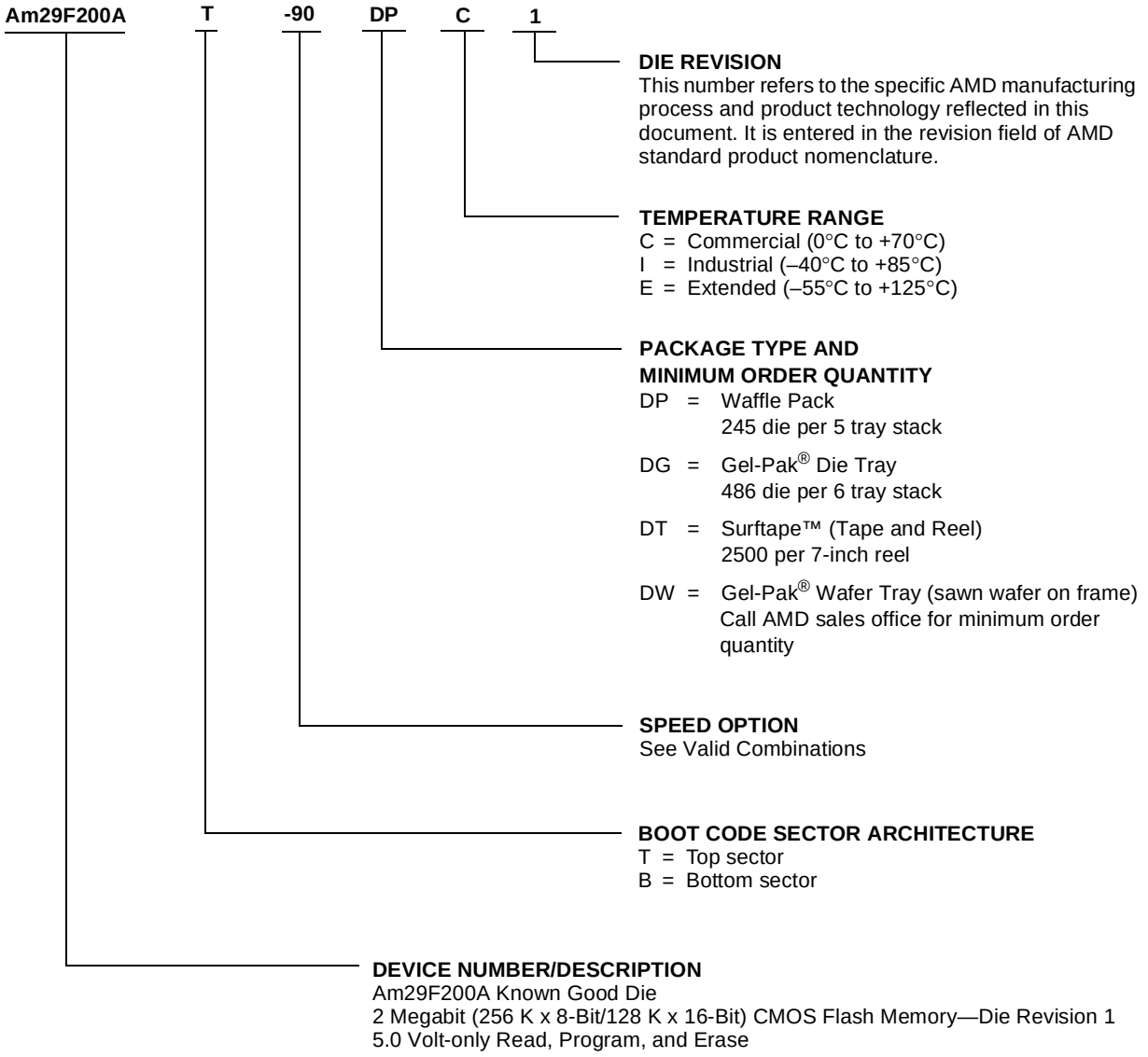
Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	0.0	0.0	0.0000	0.0000
2	DQ4	8.5	–1.2	–0.2159	–0.0305
3	DQ12	–17.3	–1.2	–0.4394	–0.0305
4	DQ5	–26.1	–1.2	–0.6629	–0.0305
5	DQ13	–34.9	–1.2	–0.8865	–0.0305
6	DQ6	–43.6	–1.2	–1.1074	–0.0305
7	DQ14	–52.4	–1.2	–1.3310	–0.0305
8	DQ7	–61.2	–1.2	–1.5545	–0.0305
9	DQ15/A-1	–69.9	–1.2	–1.7755	–0.0305
10	V_{SS}	–80.2	2.7	–2.0371	0.0686
11	BYTE#	–82.3	–13.5	–2.0904	–0.3429
12	A16	–82.3	–24.1	–2.0904	–0.6121
13	A15	–82.3	–128.4	–2.0904	–3.2614
14	A14	–82.3	–138.7	–2.0904	–3.5230
15	A13	–82.3	–150.0	–2.0904	–3.8100
16	A12	–68.2	–150.0	–1.7323	–3.8100
17	A11	–57.9	–150.0	–1.4707	–3.8100
18	A10	–47.6	–150.0	–1.2090	–3.8100
19	A9	–36.7	–150.0	–0.9322	–3.8100
20	A8	–26.4	–150.0	–0.6706	–3.8100
21	WE#	–16.1	–150.0	–0.4089	–3.8100
22	RESET#	–5.2	–150.0	–0.1321	–3.8100
23	RY/BY#	26.1	–150.0	0.6629	–3.8100
24	A7	50.2	–150.0	1.2751	–3.8100
25	A6	60.5	–150.0	1.5367	–3.8100
26	A5	70.8	–150.0	1.7983	–3.8100
27	A4	81.1	–150.0	2.0599	–3.8100
28	A3	91.4	–150.0	2.3216	–3.8100
29	A2	91.5	–138.7	2.3241	–3.5230
30	A1	91.5	–128.4	2.3241	–3.2614
31	A0	91.5	–24.1	2.3241	–0.6121
32	CE#	91.5	–13.6	2.3241	–0.3454
33	V_{SS}	91.1	1.8	2.3139	0.0457
34	OE#	79.8	–0.7	2.0269	–0.0178
35	DQ0	70.0	–1.2	1.7780	–0.0305
36	DQ8	61.3	–1.2	1.5570	–0.0305
37	DQ1	52.5	–1.2	1.3335	–0.0305
38	DQ9	43.7	–1.2	1.1100	–0.0305
39	DQ2	34.9	–1.2	0.8865	–0.0305
40	DQ10	26.2	–1.2	0.6655	–0.0305
41	DQ3	17.4	–1.2	0.4420	–0.0305
42	DQ11	8.6	–1.2	0.2184	–0.0305

Note: *The coordinates above are relative to the center of pad 1 and can be used to operate wire bonding equipment.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
Am29F200AT-90, Am29F200AB-90	DPC 1, DPI 1, DPE 1, DGC 1, DGI 1, DGE 1, DTC 1, DTI 1, DTE 1, DWC 1, DWI 1, DWE 1
Am29F200AT-120, Am29F200AB-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PRODUCT TEST FLOW

Figure 1 provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29F200A product qualification database supplement for KGD. AMD implements quality assurance procedures throughout the product test flow. In addition, an off-line quality monitoring program (QMP) further guarantees AMD quality standards are met on Known Good Die products. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in.

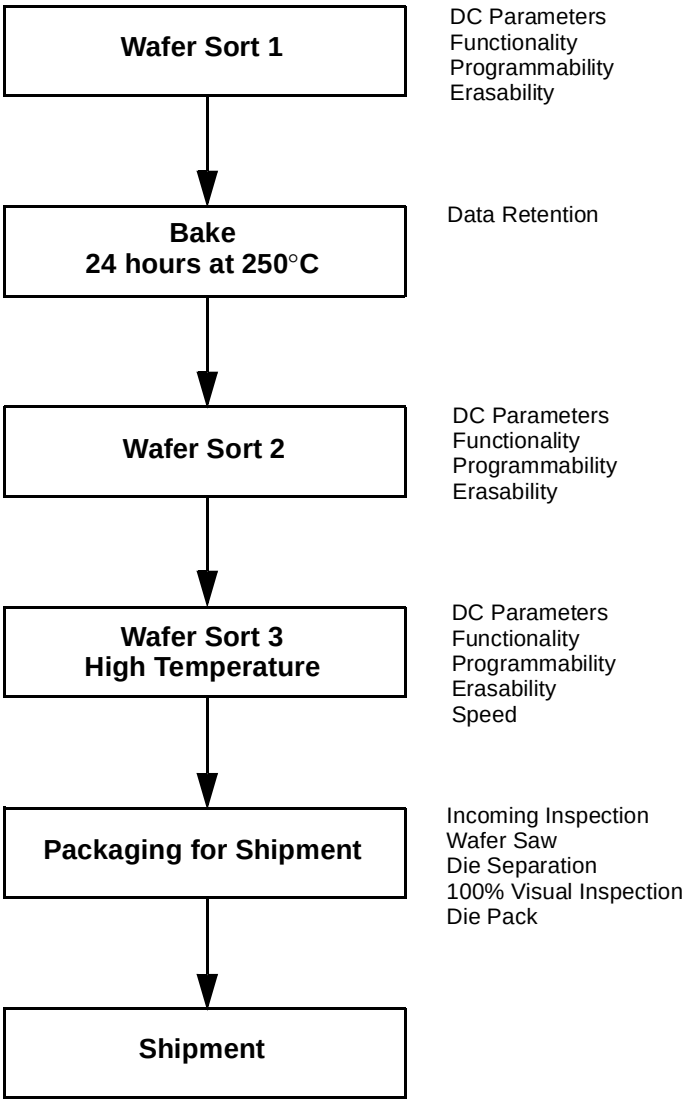


Figure 1. AMD KGD Product Test Flow

PHYSICAL SPECIFICATIONS

Die dimensions . . . . . 191 mils x 174 mils
. . . . . 4.85 mm x 4.42 mm

Die Thickness . . . . . ~20 mils

Bond Pad Size . . . . . 4.55 mils x 4.55 mils
. . . . . 115.6 µm x 115.6 µm

Pad Area Free of Passivation . . . . . 20.70 $mils^2$
. . . . . 13,363 μm^2

Pads Per Die 42

Bond Pad Metalization . . . . . Al/Cu/Si

Die Backside . . . . . No metal, may be grounded (optional)

Passivation . . . . . Nitride/SOG/Nitride

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage) . . . . . 4.5 V to 5.5 V

Junction Temperature Under Bias . . T_J (max) = 130°C

Operating Temperature

- Commercial . . . . . 0°C to +70°C
- Industrial . . . . . –40°C to +85°C
- Extended . . . . . –55°C to +125°C

MANUFACTURING INFORMATION

Manufacturing . . . . . FASL

Test . . . . . SDC

Manufacturing ID (Top Boot) 98483AK
(Bottom Boot) 98483ABK

Preparation for Shipment . . . . . Penang, Malaysia

Fabrication Process CS29AF

Die Revision 1

SPECIAL HANDLING INSTRUCTIONS

Processing

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

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REVISION SUMMARY FOR AM29F200A KNOWN GOOD DIE

Formatted to match current template. Updated Distinctive Characteristics and General Description sections using the current main data sheet.