SUPPLEMENT

Am29F400B Known Good Die

4 Megabit (512 K x 8-Bit/256 K x 16-Bit)
CMOS 5.0 Volt-only, Boot Sector Flash Memory—Die Revision 1

DISTINCTIVE CHARACTERISTICS

- **Single power supply operation**
  - — 5.0 volt-only operation for read, erase, and program operations
  - — Minimizes system level requirements
- **Manufactured on 0.35 µm process technology**
  - — Compatible with 0.5 µm Am29F400 device
- **High performance**
  - — Acess time as fast as 70 ns
- **Low power consumption (typical values at 5 MHz)**
  - — 1 µA standby mode current
  - — 20 mA read current (byte mode)
  - — 28 mA read current (word mode)
  - — 30 mA program/erase current
- **Flexible sector architecture**
  - — One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and seven 64 Kbyte sectors (byte mode)
  - — One 8 Kword, two 4 Kword, one 16 Kword, and seven 32 Kword sectors (word mode)
  - — Supports full chip erase
  - — Sector Protection features:

    A hardware method of locking a sector to prevent any program or erase operations within that sector

    Sectors can be locked via programming equipment

    Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Top or bottom boot block configurations available**
- **Embedded Algorithms**
  - — Embedded Erase algorithm automatically preprograms and erases the entire chip or any combination of designated sectors
  - — Embedded Program algorithm automatically writes and verifies data at specified addresses
- **Minimum 1,000,000 write cycle per sector guaranteed**
- **Compatibility with JEDEC standards**
  - — Pinout and software compatible with single-power-supply Flash
  - — Superior inadvertent write protection
- **Data# Polling and toggle bits**
  - — Provides a software method of detecting program or erase operation completion
- **Ready/Busy# pin (RY/BY#)**
  - — Provides a hardware method of detecting program or erase cycle completion
- **Erase Suspend/Erase Resume**
  - — Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Hardware reset pin (RESET#)**
  - — Hardware method to reset the device to reading array data

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GENERAL DESCRIPTION

The Am29F400B in Known Good Die (KGD) form is a 4 Mbit, 5.0 volt-only Flash memory. AMD defines KGD as standard product in die form, tested for functionality and speed. AMD KGD products have the same reliability and quality as AMD products in packaged form.

Am29F400B Features

The Am29F400B is a 4 Mbit, 5.0 volt-only Flash memory organized as 524,288 bytes or 262,144 words. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in-system with the standard system 5.0 volt V_{CC} supply. A 12.0 V V_{PP} is not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

This device is manufactured using AMD's 0.35 µm process technology, and offers all the features and benefits of the Am29F400, which was manufactured using 0.5 µm process technology.

To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 5.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved via programming equipment.

The **Erase Suspend** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The system can place the device into the **standby mode**. Power consumption is greatly reduced in this mode.

AMD's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

ELECTRICAL SPECIFICATIONS

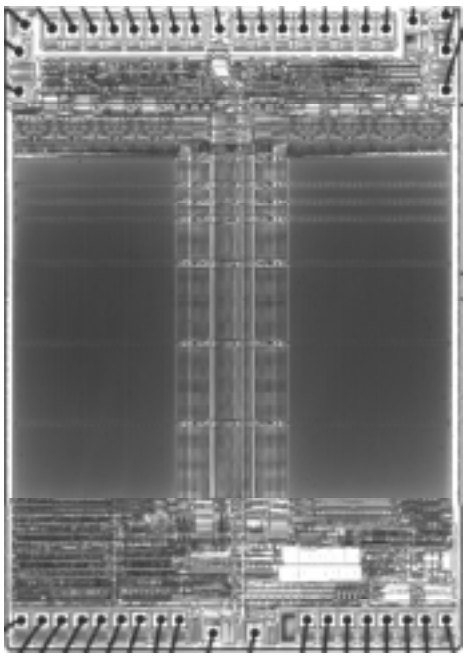
Refer to the Am29F400B data sheet, document number 21505, for full electrical specifications on the Am29F400B in KGD form.

PRODUCT SELECTOR GUIDE

Family Part Number		Am29F400B KGD		
Speed Option	V_{CC} = 5.0 V ± 5%	**-75**		
	V_{CC} = 5.0 V ± 10%		**-90**	**-120**
Max access time, ns (t_{ACC})		70	90	120
Max CE# access time, ns (t_{CE})		70	90	120
Max OE# access time, ns (t_{OE})		30	35	50

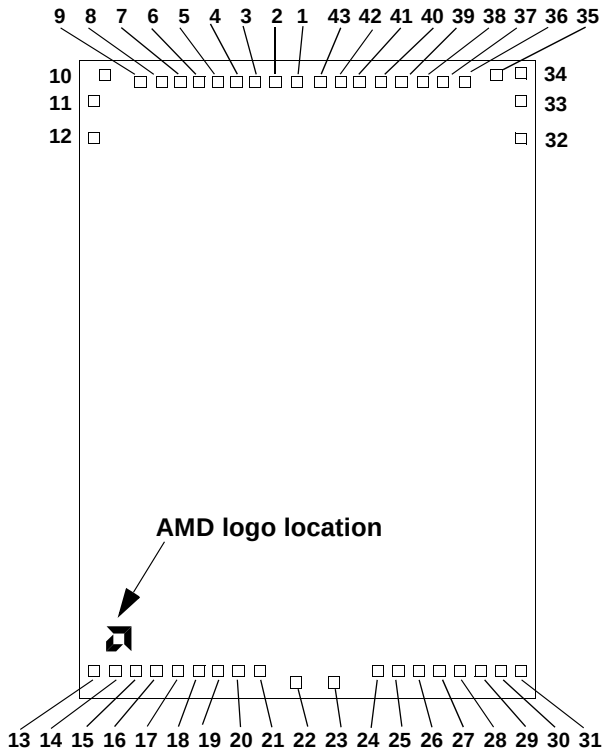
DIE PHOTOGRAPH

Orientation relative to leading edge of tape and reel



Orientation relative to top left corner of Gel-Pak

DIE PAD LOCATIONS



PAD DESCRIPTION

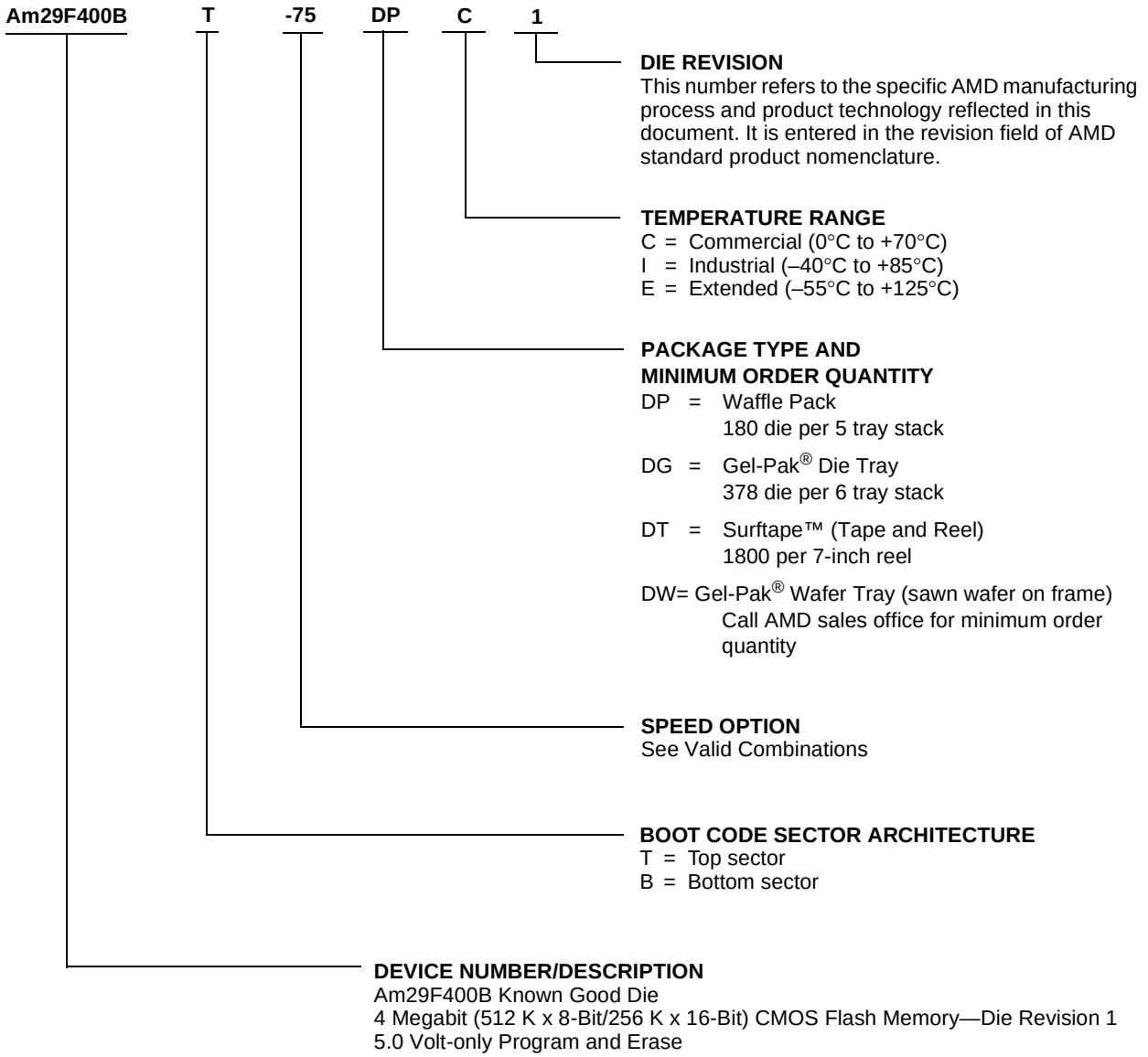
Pad	Signal	Pad Center (mils)		Pad Center (millimeters)	
		X	Y	X	Y
1	V_{CC}	0.00	0.00	0.0000	0.0000
2	DQ4	7.22	0.00	0.1835	0.0000
3	DQ12	13.45	0.00	0.3417	0.0000
4	DQ5	19.59	0.00	0.4977	0.0000
5	DQ13	25.82	0.00	0.6559	0.0000
6	DQ6	31.96	0.00	0.8119	0.0000
7	DQ14	38.19	0.00	0.9701	0.0000
8	DQ7	44.33	0.00	1.1261	0.0000
9	DQ15/A-1	50.56	0.00	1.2843	0.0000
10	V_{SS}	58.61	–1.42	1.4887	–0.0361
11	BYTE#	60.50	6.84	1.5367	0.1738
12	A16	60.50	18.99	1.5367	0.4823
13	A15	60.13	181.06	1.5274	4.5990
14	A14	53.99	181.06	1.3714	4.5990
15	A13	48.28	181.06	1.2264	4.5990
16	A12	42.14	181.06	1.0704	4.5990
17	A11	36.43	181.06	0.9254	4.5990
18	A10	30.29	181.06	0.7694	4.5990
19	A9	24.58	180.80	0.6244	4.5924
20	A8	18.34	181.06	0.4659	4.5990
21	WE#	12.63	181.06	0.3209	4.5990
22	RESET#	2.54	185.03	0.0646	4.6998
23	RY/BY#	–10.00	185.03	–0.2538	4.6998
24	A17	–25.79	181.06	–0.6546	4.5990
25	A7	–31.92	181.06	–0.8106	4.5990
26	A6	–37.63	181.06	–0.9556	4.5990
27	A5	–43.77	181.06	–1.1116	4.5990
28	A4	–49.48	181.06	–1.2566	4.5990
29	A3	–55.62	181.06	–1.4126	4.5990
30	A2	–61.33	181.06	–1.5576	4.5990
31	A1	–67.47	181.06	–1.7136	4.5990
32	A0	–67.84	18.99	–1.7229	0.4823
33	CE#	–67.84	6.84	–1.7229	0.1738
34	V_{SS}	–67.84	–4.00	–1.7229	–0.1015
35	OE#	–57.84	–2.39	–1.4691	–0.0608
36	DQ0	–49.86	0.00	–1.2664	0.0000
37	DQ8	–43.63	0.00	–1.1082	0.0000
38	DQ1	–37.49	0.00	–0.9522	0.0000
39	DQ9	–31.26	0.00	–0.7940	0.0000
40	DQ2	–25.12	0.00	–0.6380	0.0000
41	DQ10	–18.89	0.00	–0.4798	0.0000
42	DQ3	–12.75	0.00	–0.3238	0.0000
43	DQ11	–6.52	0.00	–0.1656	0.0000

Note: *The coordinates above are relative to the center of pad 1 and can be used to operate wire bonding equipment.*

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
Am29F400BT-75 Am29F400BB-75	DPC 1, DPI 1, DPE 1, DGC 1, DGI 1, DGE 1, DTC 1, DTI 1, DTE 1, DWC 1, DWI 1, DWE 1
Am29F400BT-90 Am29F400BB-90	
Am29F400BT-120 Am29F400BB-120	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

PRODUCT TEST FLOW

Figure 1 provides an overview of AMD's Known Good Die test flow. For more detailed information, refer to the Am29F400B product qualification database supplement for KGD. AMD implements quality assurance procedures throughout the product test flow. In addition, an off-line quality monitoring program (QMP) further guarantees AMD quality standards are met on Known Good Die products. These QA procedures also allow AMD to produce KGD products without requiring or implementing burn-in.

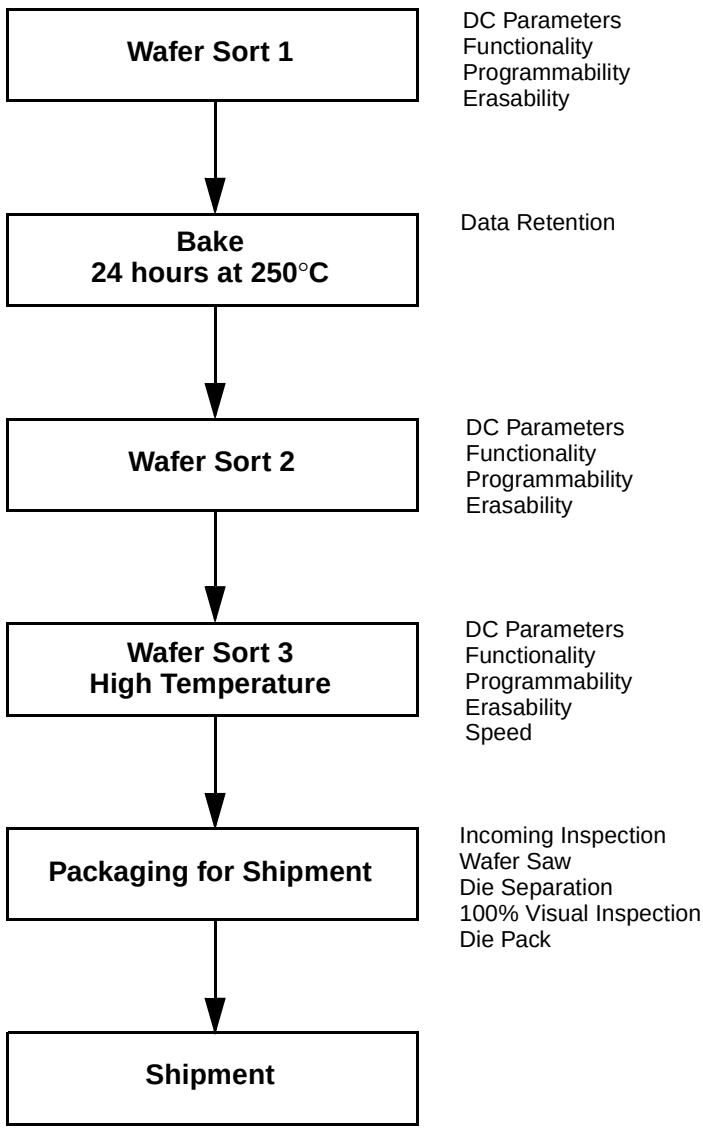


Figure 1. AMD KGD Product Test Flow

PHYSICAL SPECIFICATIONS

Die dimensions . . . . . 141.34 mils x 207.48 mils
. . . . . 3.59 mm x 5.27 mm

Die Thickness. . . . . ~20 mils

Bond Pad Size . . . . . 3.94 mils x 3.94 mils
. . . . . 100 µm x 100 µm

Pad Area Free of Passivation . . . . . 15.52 $mils^2$
. . . . . 10,000 μm^2

Pads Per Die 43

Bond Pad Metalization . . . . . Al/Cu/Si

Die Backside . . . . . No metal,
may be grounded (optional)

Passivation . . . . . Nitride/SOG/Nitride

DC OPERATING CONDITIONS

V_{CC} (Supply Voltage) . . . . . 4.5 V to 5.5 V

Junction Temperature Under Bias . . T_J (max) = 130°C

Operating Temperature

Commercial . . . . . 0°C to +70°C
Industrial . . . . . –40°C to +85°C
Extended . . . . . –55°C to +125°C

MANUFACTURING INFORMATION

Manufacturing . . . . . FASL

Test . . . . . SDC

Manufacturing ID (Top Boot) 98965AK
(Bottom Boot) 98965ABK

Preparation for Shipment . . . . . Penang, Malaysia

Fabrication Process CS39

Die Revision 1

SPECIAL HANDLING INSTRUCTIONS

Processing

Do not expose KGD products to ultraviolet light or process them at temperatures greater than 250°C. Failure to adhere to these handling instructions will result in irreparable damage to the devices. For best yield, AMD recommends assembly in a Class 10K clean room with 30% to 60% relative humidity.

Storage

Store at a maximum temperature of 30°C in a nitrogen-purged cabinet or vacuum-sealed bag. Observe all standard ESD handling procedures.

TERMS AND CONDITIONS OF SALE FOR AMD NON-VOLATILE MEMORY DIE

All transactions relating to AMD Products under this agreement shall be subject to AMD's standard terms and conditions of sale, or any revisions thereof, which revisions AMD reserves the right to make at any time and from time to time. In the event of conflict between the provisions of AMD's standard terms and conditions of sale and this agreement, the terms of this agreement shall be controlling.

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REVISION SUMMARY

Revision B

Formatted to match current template. Updated Distinctive Characteristics and General Description sections using the current main data sheet. Updated for CS39 process technology.

Revision B+1

Distinctive Characteristics

The minimum guarante per sector is now 1 million cycles.

Global

Added -75 and -90 speed options.

Pad Description

Corrected coordinates for pads 2, 19, 22, 35, 40, and 42.

Physical Specifications

Changed die thickness specification to ~20 mils.