FINAL

Am27X1024

1 Megabit (64 K x 16-Bit) CMOS ExpressROM Device

DISTINCTIVE CHARACTERISTICS

- **As an OTP EPROM alternative:**
  - — Factory optimized programming
  - — Fully tested and guaranteed
- **As a Mask ROM alternative:**
  - — Shorter leadtime
  - — Lower volume per code
- **Fast access time**
  - — 70 ns
- **Single +5 V power supply**
- **Compatible with JEDEC-approved EPROM pinout**
- **±10% power supply tolerance**
- **High noise immunity**
- **Low power dissipation**
  - — 20 µA maximum CMOS standby current
- **Available in Plastic Dual-In-line Package (PDIP) and Plastic Leaded Chip Carrier (PLCC)**
- **Latch-up protected to 100 mA from –1 V to V_{CC} + 1 V**
- **Versatile features for simple interfacing**
  - — Both CMOS and TTL input/output compatibility
  - — Two line control functions

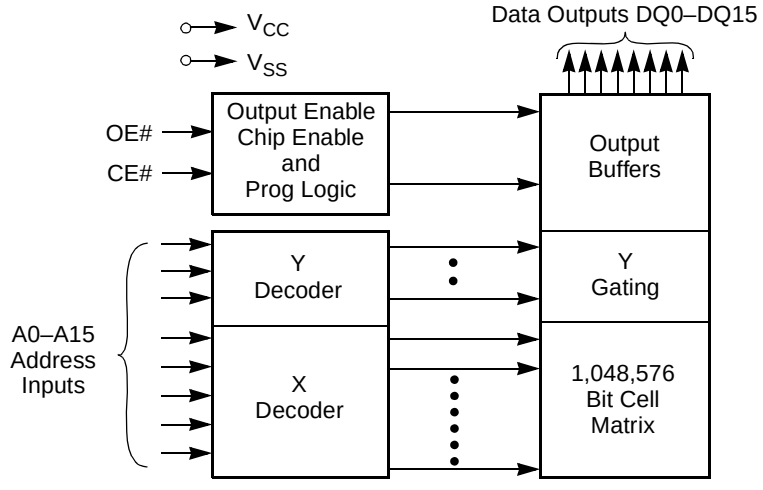
GENERAL DESCRIPTION

The Am27X1024 is a factory programmed and tested OTP EPROM. It is programmed after packaging prior to final test. Every device is rigorously tested under AC and DC operating conditions to your stable code. It is organized as 64 Kwords by 16 bits per word and is available in plastic dual in-line packages (PDIP), as well as plastic leaded chip carrier (PLCC) packages. ExpressROM devices provide a board-ready memory solution for medium to high volume codes with short leadtimes. This offers manufacturers a cost-effective and flexible alternative to OTP EPROMs and mask programmed ROMs.

Data can be accessed as fast as 70 ns, allowing high-performance microprocessors to operate with reduced WAIT states. The device offers separate Output Enable (OE#) and Chip Enable (CE#) controls, thus eliminating bus contention in a multiple bus microprocessor system.

AMD's CMOS process technology provides high speed, low power, and high noise immunity. Typical power consumption is only 125 mW in active mode, and 100 µW in standby mode.

BLOCK DIAGRAM



12079F-1

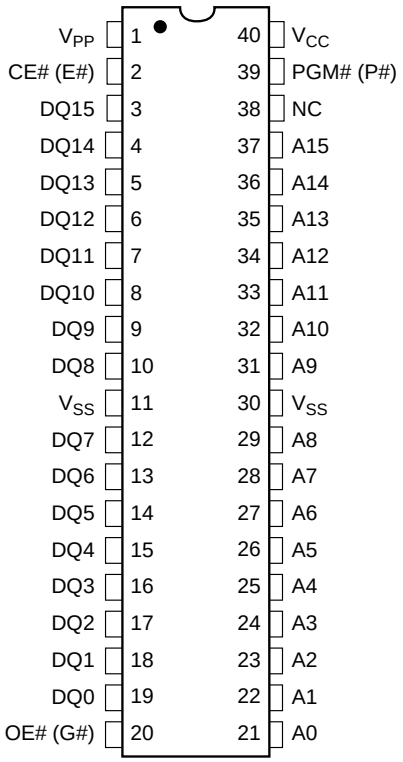
Publication# **12079** Rev: **F** Amendment/**0**
Issue Date: **May 1998**

PRODUCT SELECTOR GUIDE

Family Part Number		Am27X1024					
Speed Options	V_{CC} = 5.0 V ± 5%						**-255**
	V_{CC} = 5.0 V ± 10%	**-70**	**-90**	**-120**	**-150**	**-200**	
Max Access Time (ns)		70	90	120	150	200	250
CE# (E#) Access (ns)		70	90	120	150	200	250
OE# (G#) Access (ns)		70	45	50	65	75	75

CONNECTION DIAGRAMS

DIP



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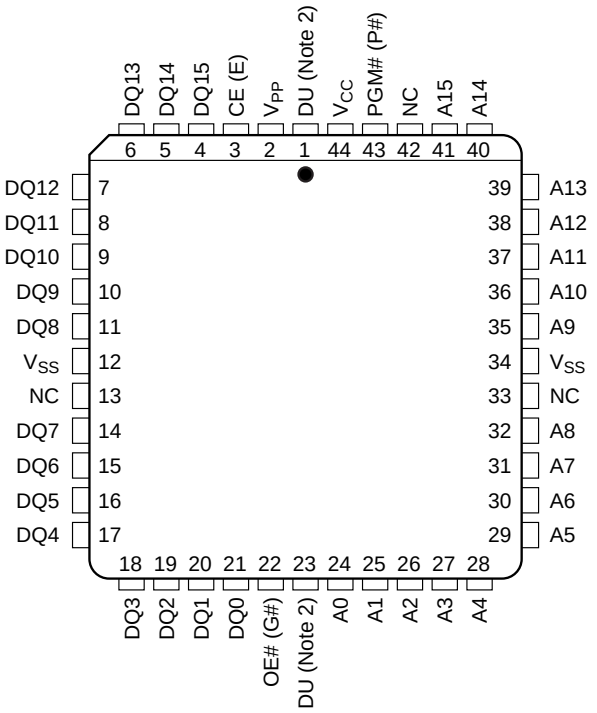
PLCC



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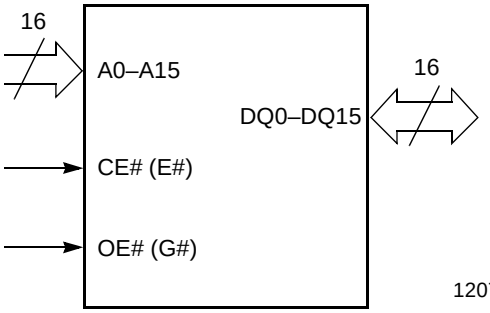
Notes:

1. *JEDEC nomenclature is in parenthesis.*
2. *Don't use (DU) for PLCC.*

PIN DESIGNATIONS

A0–A15 = Address Inputs
CE# (E#) = Chip Enable Input
DQ0–DQ15 = Data Input/Outputs
OE# (G#) = Output Enable Input
PGM# (P#) = Program Enable Input
V_{CC} = V_{CC} Supply Voltage
V_{PP} = Program Voltage Input
V_{SS} = Ground
NC = No Internal Connection

LOGIC SYMBOL



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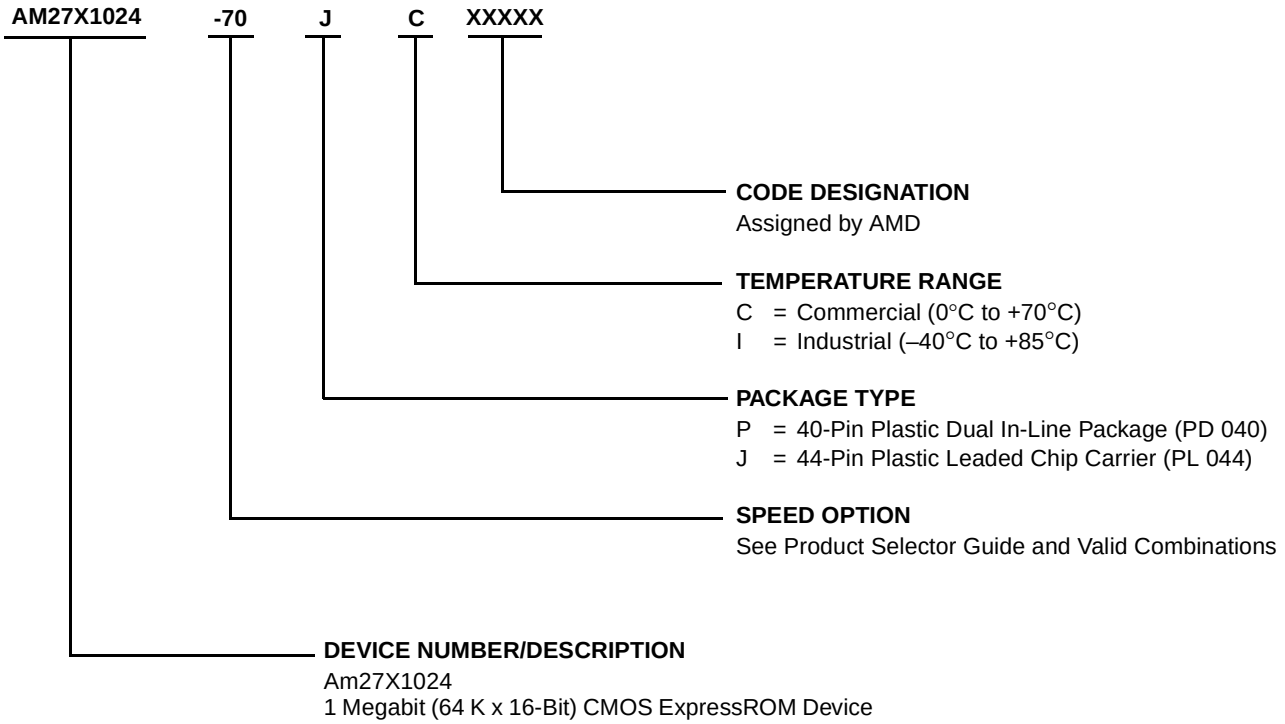
ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of the following:



Valid Combinations	
AM27X1024-70	PC, JC, PI, JI
AM27X1024-90	
AM27X1024-120	
AM27X1024-150	
AM27X1024-200	
AM27X1024-255 V_{CC} = 5.0 V ± 5%	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

FUNCTIONAL DESCRIPTION

Read Mode

To obtain data at the device outputs, Chip Enable (CE#) and Output Enable (OE#) must be driven low. CE# controls the power to the device and is typically used to select the device. OE# enables the device to output data, independent of device selection. Addresses must be stable for at least $t_{ACC}–t_{OE}$. Refer to the Switching Waveforms section for the timing diagram.

Standby Mode

The device enters the CMOS standby mode when CE# is at $V_{CC} \pm 0.3$ V. Maximum V_{CC} current is reduced to 100 µA. The device enters the TTL-standby mode when CE# is at V_{IH}. Maximum V_{CC} current is reduced to 1.0 mA. When in either standby mode, the device places its outputs in a high-impedance state, independent of the OE# input.

Output OR-Tieing

To accommodate multiple memory connections, a two-line control function provides:

- Low memory power dissipation, and
- Assurance that output bus contention will not occur.

CE# should be decoded and used as the primary device-selecting function, while OE# be made a common connection to all devices in the array and connected to the READ line from the system control bus. This assures that all deselected memory devices are in their low-power standby mode and that the output pins are only active when data is desired from a particular memory device.

System Applications

During the switch between active and standby conditions, transient current peaks are produced on the rising and falling edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitance loading of the device. At a minimum, a 0.1 µF ceramic capacitor (high frequency, low inherent inductance) should be used on each device between V_{CC} and V_{SS} to minimize transient effects. In addition, to overcome the voltage drop caused by the inductive effects of the printed circuit board traces on Express-ROM device arrays, a 4.7 µF bulk electrolytic capacitor should be used between V_{CC} and V_{SS} for each eight devices. The location of the capacitor should be close to where the power supply is connected to the array.

MODE SELECT TABLE

Mode	CE#	OE#	PGM#	V_{PP}	Outputs
Read	V_{IL}	V_{IL}	X	X	D_{OUT}
Output Disable	X	V_{IH}	X	X	High Z
Standby (TTL)	V_{IH}	X	X	X	High Z
Standby (CMOS)	$V_{CC} \pm 0.3$ V	X	X	X	High Z

Note:
X = Either V_{IH} or V_{IL}.

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
OTP Products. . . . . –65°C to +125°C
Ambient Temperature
with Power Applied. . . . . –55°C to +125°C

Voltage with Respect to V_{SS}
All pins except V_{CC} . . . . . –0.6 V to V_{CC} + 0.6 V

V_{CC} (Note 1). . . . . –0.6 V to 7.0 V

Note:

1. *Minimum DC voltage on input or I/O pins –0.5 V. During voltage transitions, the input may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input and I/O pins is V_{CC} + 5 V. During voltage transitions, input and I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A) . . . . . .0°C to +70°C

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . .–40°C to +85°C

Supply Read Voltages

V_{CC} for ± 5% devices . . . . . +4.75 V to +5.25 V
V_{CC} for ± 10% devices . . . . . +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over operating range (unless otherwise specified)

Parameter Symbol	Parameter Description	Test Conditions	Min	Max	Unit
V_{OH}	Output HIGH Voltage	I_{OH} = –400 µA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA		0.45	V
V_{IH}	Input HIGH Voltage		2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage		–0.5	+0.8	V
I_{LI}	Input Load Current	V_{IN} = 0 V to V_{CC}		1.0	µA
I_{LO}	Output Leakage Current	V_{OUT} = 0 V to V_{CC}		1.0	µA
I_{CC1}	V_{CC} Active Current (Note 2)	CE# = V_{IL}, f = 10 MHz, I_{OUT} = 0 mA		50	mA
I_{CC2}	V_{CC} TTL Standby Current	CE# = V_{IH}		1.0	mA
I_{CC3}	V_{CC} CMOS Standby Current	CE# = V_{CC} ± 0.3 V		100	µA

***Caution**: The device must not be removed from (or inserted into) a socket when V_{CC} or V_{PP} is applied.*

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}.*
2. *I_{CC1} is tested with OE# = V_{IH} to simulate open outputs.*
3. *Minimum DC Input Voltage is –0.5 V. During transitions, the inputs may overshoot to –2.0 V for periods less than 20 ns. Maximum DC Voltage on output pins is V_{CC} + 0.5 V, which may overshoot to V_{CC} + 2.0 V for periods less than 20 ns.*

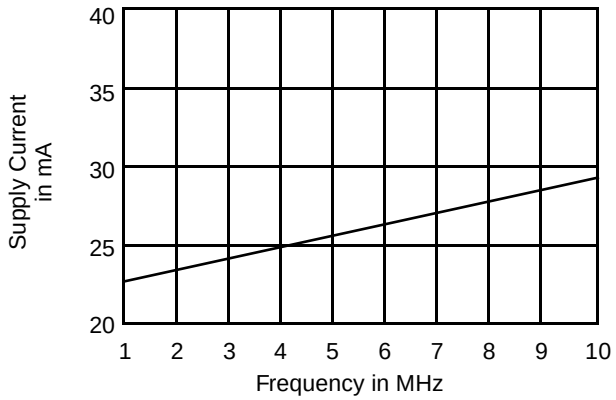


Figure 1. Typical Supply Current vs. Frequency
V_{CC} = 5.5 V, T = 25°C

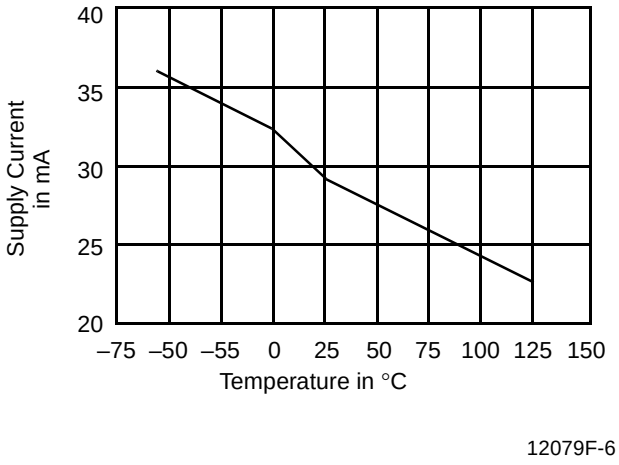
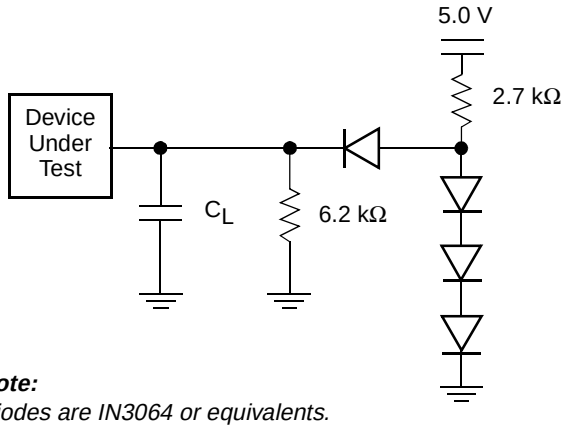


Figure 2. Typical Supply Current vs. Temperature
V_{CC} = 5.5 V, f = 10 MHz

TEST CONDITIONS



Note:
Diodes are IN3064 or equivalents.

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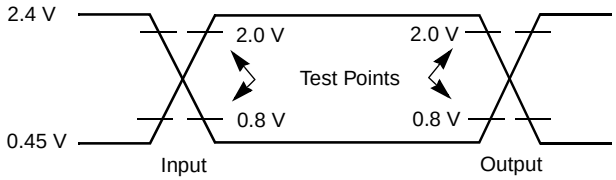
Figure 3. Test Setup

Table 1. Test Specifications

Test Condition	All	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	100	pF
Input Rise and Fall Times	≤ 20	ns
Input Pulse Levels	0.45–2.4	V
Input timing measurement reference levels	0.8, 2.0	V
Output timing measurement reference levels	0.8, 2.0	V

SWITCHING TEST WAVEFORM



Note: *For C_L = 100 pF.*

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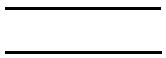
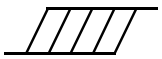
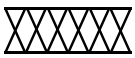
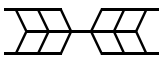
KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

KS000010-PAL

AC CHARACTERISTICS

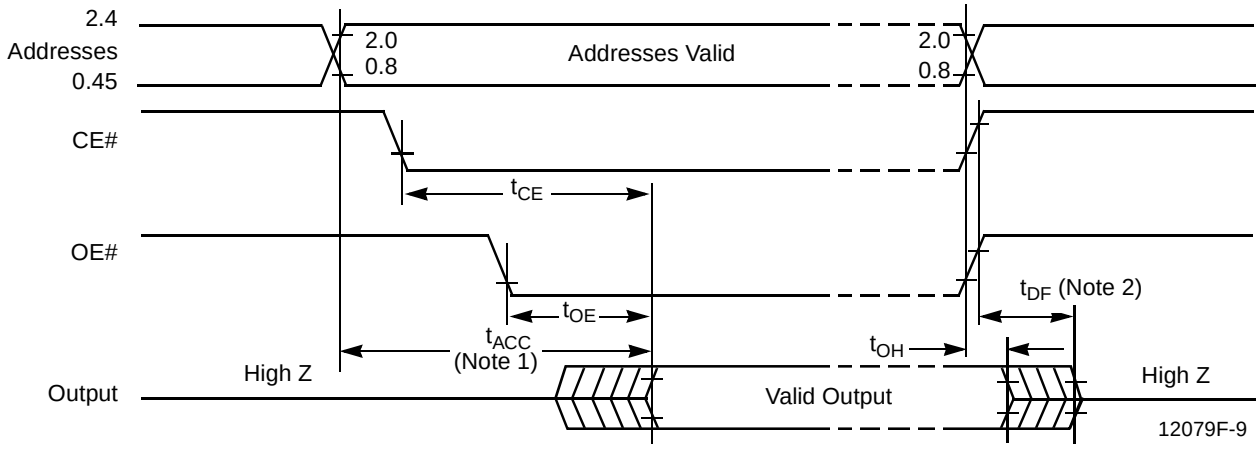
Parameter Symbols		Description	Test Setup		Am27X1024						Unit
JEDEC	Standard				-70	-90	-120	-150	-200	-255	
t_{AVQV}	t_{ACC}	Address to Output Delay	CE#, OE# = V_{IL}	Max	70	90	120	150	200	250	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay	OE# = V_{IL}	Max	70	90	120	150	200	250	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay	CE# = V_{IL}	Max	40	45	50	65	75	75	ns
t_{EHQZ} t_{GHQZ}	t_{DF} (Note 2)	Chip Enable High or Output Enable High to Output High Z, Whichever Occurs First		Max	30	40	50	50	50	50	ns
t_{AXQX}	t_{OH}	Output Hold Time from Addresses, CE# or OE#, Whichever Occurs First		Min	0	0	0	0	0	0	ns

Caution: *Do not remove the device from (or insert it into) a socket or board that has V_{PP} or V_{CC} applied.*

Notes:

1. *V_{CC} must be applied simultaneously or before V_{PP}, and removed simultaneously or after V_{PP}*
2. *This parameter is sampled and not 100% tested.*
3. *Switching characteristics are over operating range, unless otherwise specified.*
4. *See Figure 3 and Table 1 for test specifications.*

SWITCHING WAVEFORMS



Notes:

1. *OE# may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of the addresses without impact on t_{ACC}.*
2. *t_{DF} is specified from OE# or CE#, whichever occurs first.*

PACKAGE CAPACITANCE

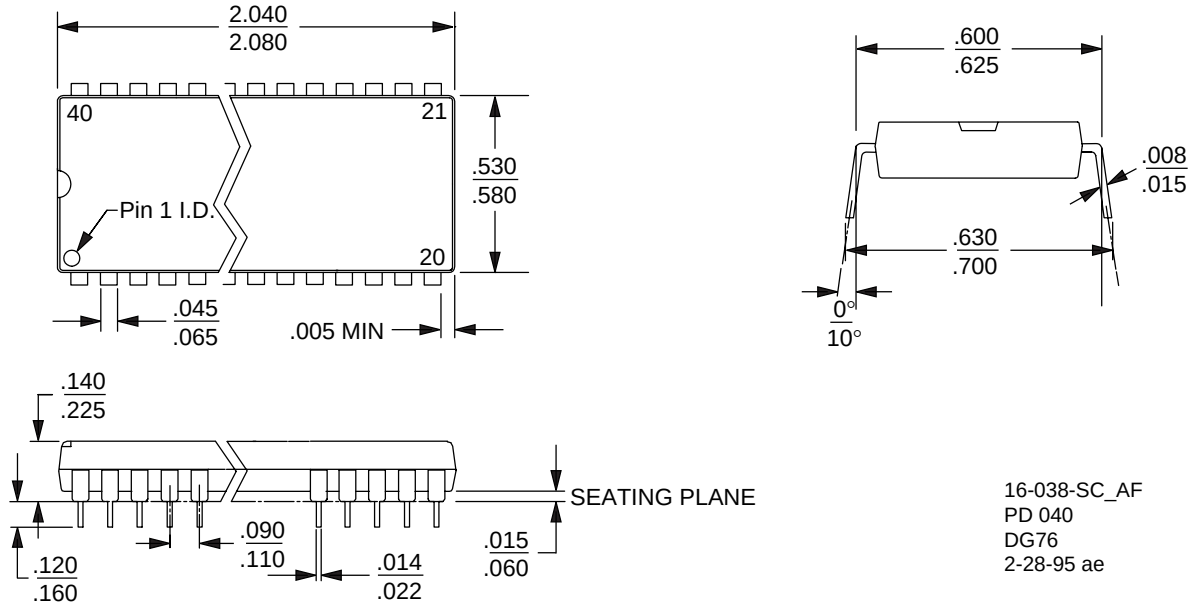
Parameter Symbol	Parameter Description	Test Conditions	PD 040		PL 044		Unit
			Typ	Max	Typ	Max	
C_{IN}	Input Capacitance	V_{IN} = 0	7	12	8	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	11	14	11	14	pF

Notes:

1. *This parameter is only sampled and not 100% tested.*
2. *T_A = +25°C, f = 1 MHz.*

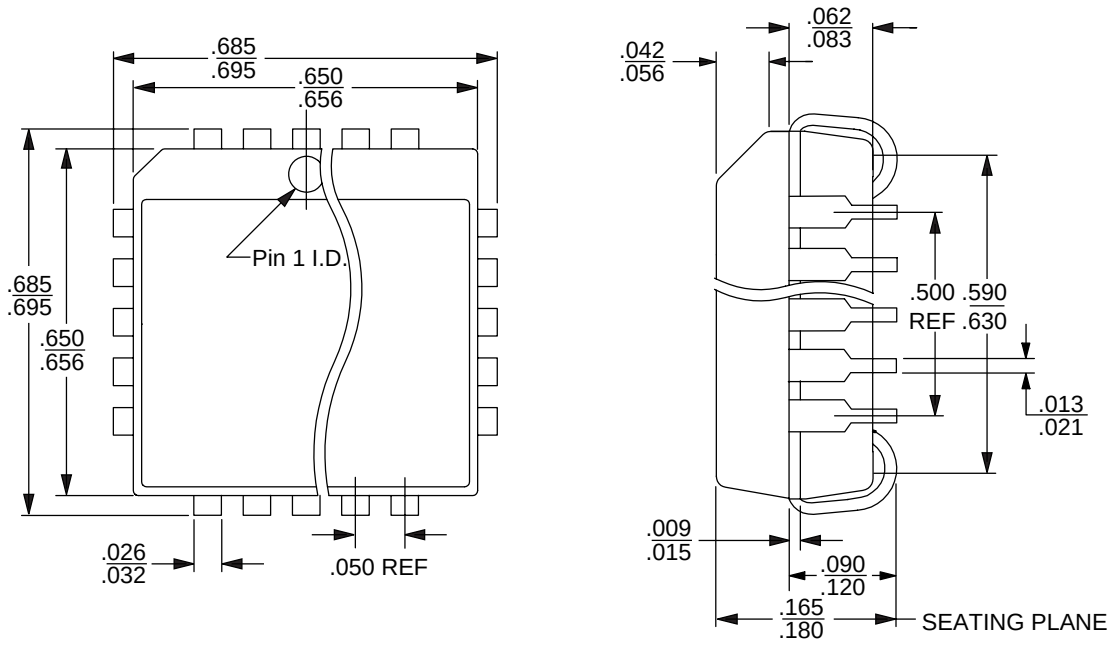
PHYSICAL DIMENSIONS

PD 040—40-Pin Plastic Dual In-Line Package (measured in inches)



16-038-SC_AF
PD 040
DG76
2-28-95 ae

PL 044—44-Pin Plastic Leaded Chip Carrier (measured in inches)



TOP VIEW

SIDE VIEW

16-038-SQ
PL 044
EC80
11.3.97 lv

REVISION SUMMARY FOR AM27X1024

Revision F

Global

Changed formatting to match current data sheets.