**FINAL**

**COM'L: H-5/7/10/15/25, Q-10/15/25**
**IND: H-10/15/25, Q-20/25**

# PALCE16V8 Family

## EE CMOS 20-Pin Universal Programmable Array Logic

### DISTINCTIVE CHARACTERISTICS

- **Pin and function compatible with all 20-pin GAL devices**
- **Electrically erasable CMOS technology provides reconfigurable logic and full testability**
- **High-speed CMOS technology**
  - — 5-ns propagation delay for "-5" version
  - — 7.5-ns propagation delay for "-7" version
- **Direct plug-in replacement for the PAL16R8 series and most of the PAL10H8 series**
- **Outputs programmable as registered or combinatorial in any combination**
- **Peripheral Component Interconnect (PCI) compliant**
- **Programmable output polarity**
- **Programmable enable/disable control**
- **Preloadable output registers for testability**
- **Automatic register reset on power up**
- **Cost-effective 20-pin plastic DIP, PLCC, and SOIC packages**
- **Extensive third-party software and programmer support through FusionPLD partners**
- **Fully tested for 100% programming and functional yields and high reliability**
- **5 ns version utilizes a split leadframe for improved performance**

### GENERAL DESCRIPTION

The PALCE16V8 is an advanced PAL device built with low-power, high-speed, electrically-erasable CMOS technology. It is functionally compatible with all 20-pin GAL devices. The macrocells provide a universal device architecture. The PALCE16V8 will directly replace the PAL16R8 and PAL10H8 series devices, with the exception of the PAL16C1.

The PALCE16V8 utilizes the familiar sum-of-products (AND/OR) architecture that allows users to implement complex logic functions easily and efficiently. Multiple levels of combinatorial logic can always be reduced to sum-of-products form, taking advantage of the very wide input gates available in PAL devices. The equations are programmed into the device through floating-gate cells in the AND logic array that can be erased electrically.

The fixed OR array allows up to eight data product terms per output for logic functions. The sum of these products feeds the output macrocell. Each macrocell can be programmed as registered or combinatorial with an active-high or active-low output. The output configuration is determined by two global bits and one local bit controlling four multiplexers in each macrocell.

AMD's FusionPLD program allows PALCE16V8 designs to be implemented using a wide variety of popular industry-standard design tools. By working closely with the FusionPLD partners, AMD certifies that the tools provide accurate, quality support. By ensuring that third-party tools are available, costs are lowered because a designer does not have to buy a complete set of new tools for each device. The FusionPLD program also greatly reduces design time since a designer can use a tool that is already installed and familiar.



Publication# **16493** Rev. **D** Amendment **/0**
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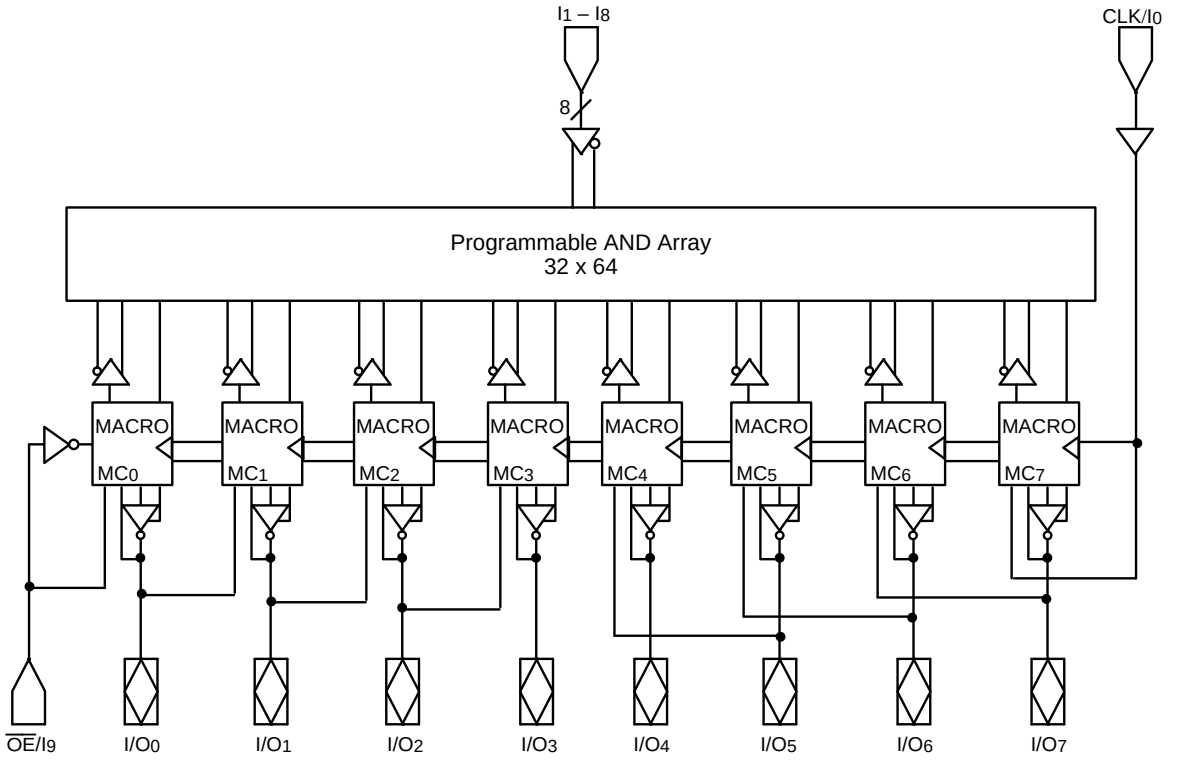
## BLOCK DIAGRAM

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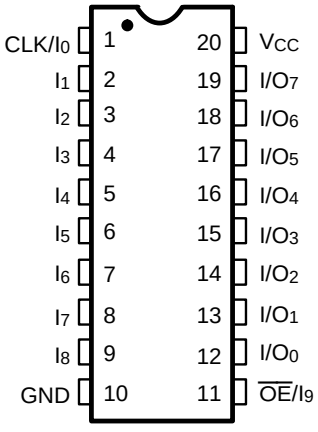
## CONNECTION DIAGRAMS
### Top View

#### DIP/SOIC

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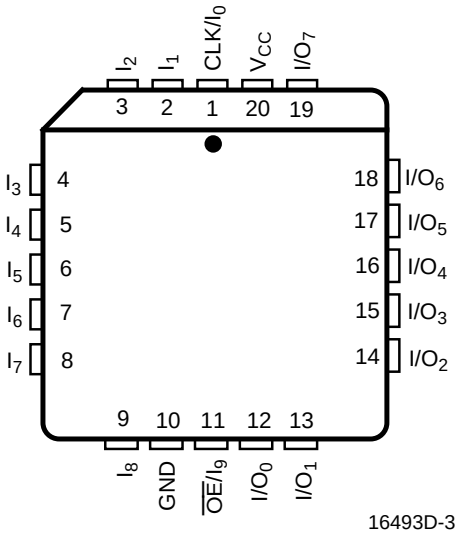
#### PLCC/LCC

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***Note:*** *Pin 1 is marked for orientation.*

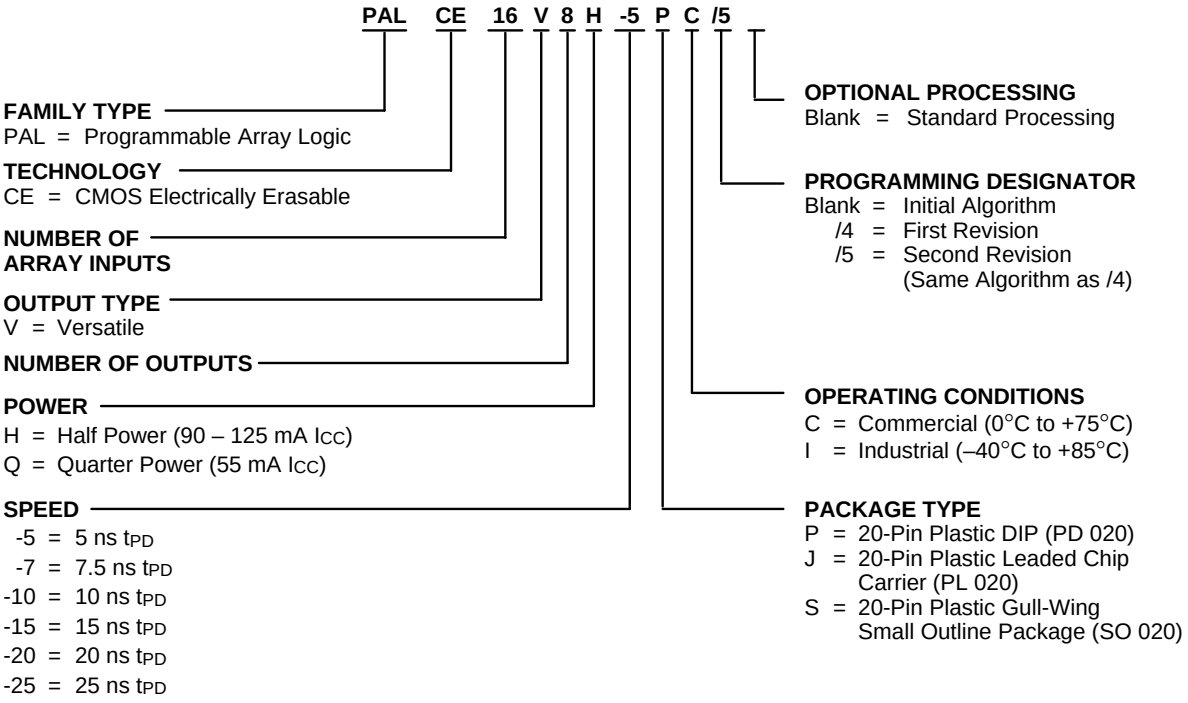
## PIN DESIGNATIONS

| | | |
|---|---|---|
| CLK | = | Clock |
| GND | = | Ground |
| I | = | Input |
| I/O | = | Input/Output |
| $\overline{OE}$ | = | Output Enable |
| $V_{CC}$ | = | Supply Voltage |

## ORDERING INFORMATION

### Commercial and Industrial Products

AMD programmable logic products for commercial and industrial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:




| Valid Combinations | | |
|---|---|---|
| PALCE16V8H-5 | JC | /5 |
| PALCE16V8H-7 | PC, JC | |
| PALCE16V8H-10 | PC, JC, SC, PI, JI | /4 |
| PALCE16V8Q-10 | PC, JC, SC | /5 |
| PALCE16V8H-15 | PC, JC, SC, PI, JI | Blank, /4 |
| PALCE16V8Q-15 | PC, JC | |
| PALCE16V8Q-20 | PI, JI | |
| PALCE16V8H-25 | PC, JC, SC, PI, JI | |
| PALCE16V8Q-25 | PC, JC, PI, JI | |

**Valid Combinations**

Valid Combinations lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations.

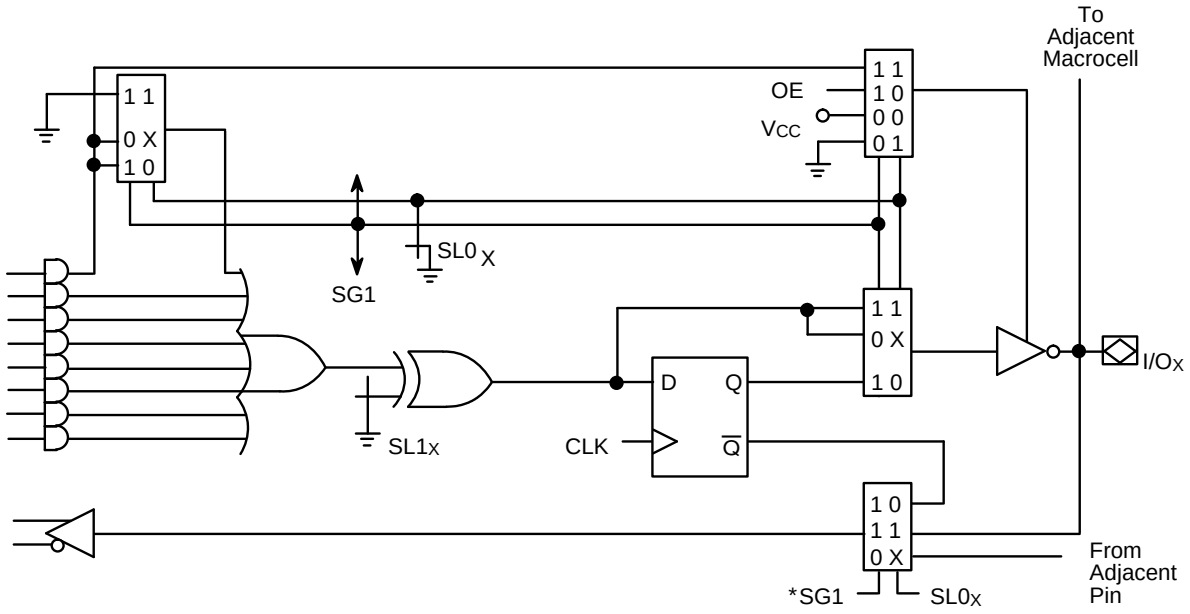
## FUNCTIONAL DESCRIPTION

The PALCE16V8 is a universal PAL device. It has eight independently configurable macrocells ($MC_0$–$MC_7$). Each macrocell can be configured as registered output, combinatorial output, combinatorial I/O or dedicated input. The programming matrix implements a programmable AND logic array, which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Pins 1 and 11 serve either as array inputs or as clock (CLK) and output enable ($\overline{OE}$), respectively, for all flip-flops.

Unused input pins should be tied directly to $V_{CC}$ or GND. Product terms with all bits unprogrammed (disconnected) assume the logical HIGH state and product terms with both true and complement of any input signal connected assume a logical LOW state.

The programmable functions on the PALCE16V8 are automatically configured from the user's design specification. The design specification is processed by development software to verify the design and create a programming file (JEDEC). This file, once downloaded to a programmer, configures the device according to the user's desired function.

The user is given two design options with the PALCE16V8. First, it can be programmed as a standard PAL device from the PAL16R8 and PAL10H8 series. The PAL programmer manufacturer will supply device codes for the standard PAL device architectures to be used with the PALCE16V8. The programmer will program the PALCE16V8 in the corresponding architecture. This allows the user to use existing standard PAL device JEDEC files without making any changes to them. Alternatively, the device can be programmed as a PALCE16V8. Here the user must use the PALCE16V8 device code. This option allows full utilization of the macrocell.

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**In macrocells $MC_0$ and $MC_7$, SG1 is replaced by $\overline{SG0}$ on the feedback multiplexer.*

**PALCE16V8 Macrocell**

## Configuration Options

Each macrocell can be configured as one of the following: registered output, combinatorial output, combinatorial I/O, or dedicated input. In the registered output configuration, the output buffer is enabled by the $\overline{OE}$ pin. In the combinatorial configuration, the buffer is either controlled by a product term or always enabled. In the dedicated input configuration, it is always disabled. With the exception of $MC_0$ and $MC_7$, a macrocell configured as a dedicated input derives the input signal from an adjacent I/O. $MC_0$ derives its input from pin 11 ($\overline{OE}$) and $MC_7$ from pin 1 (CLK).

The macrocell configurations are controlled by the configuration control word. It contains 2 global bits (SG0 and SG1) and 16 local bits ($SL0_0$ through $SL0_7$ and $SL1_0$ through $SL1_7$). SG0 determines whether registers will be allowed. SG1 determines whether the PALCE16V8 will emulate a PAL16R8 family or a PAL10H8 family device. Within each macrocell, $SL0_x$, in conjunction with SG1, selects the configuration of the macrocell, and $SL1_x$ sets the output as either active low or active high for the individual macrocell.

The configuration bits work by acting as control inputs for the multiplexers in the macrocell. There are four multiplexers: a product term input, an enable select, an output select, and a feedback select multiplexer. SG1 and $SL0_x$ are the control signals for all four multiplexers. In $MC_0$ and $MC_7$, $\overline{SG0}$ replaces SG1 on the feedback multiplexer. This accommodates CLK being the adjacent pin for $MC_7$ and $\overline{OE}$ the adjacent pin for $MC_0$.

## Registered Output Configuration

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 0. There is only one registered configuration. All eight product terms are available as inputs to the OR gate. Data polarity is determined by $SL1_x$. The flip-flop is loaded on the LOW-to-HIGH transition of CLK. The feedback path is from $\overline{Q}$ on the register. The output buffer is enabled by $\overline{OE}$.

## Combinatorial Configurations

The PALCE16V8 has three combinatorial output configurations: dedicated output in a non-registered device, I/O in a non-registered device and I/O in a registered device.

## Dedicated Output in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 0. All eight product terms are available to the OR gate. Although the macrocell is a dedicated output, the feedback is used, with the exception of pins 15 and 16. Pins 15 and 16 do not use feedback in this mode. Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as input signals. Pin 1 will use the feedback path of $MC_7$ and pin 11 will use the feedback path of $MC_0$.

## Combinatorial I/O in a Non-Registered Device

The control bit settings are SG0 = 1, SG1 = 1, and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used to enable the output buffer. The signal at the I/O pin is fed back to the AND array via the feedback multiplexer. This allows the pin to be used as an input.

Because CLK and $\overline{OE}$ are not used in a non-registered device, pins 1 and 11 are available as inputs. Pin 1 will use the feedback path of $MC_7$ and pin 11 will use the feedback path of $MC_0$.

## Combinatorial I/O in a Registered Device

The control bit settings are SG0 = 0, SG1 = 1 and $SL0_x$ = 1. Only seven product terms are available to the OR gate. The eighth product term is used as the output enable. The feedback signal is the corresponding I/O signal.

## Dedicated Input Configuration

The control bit settings are SG0 = 1, SG1 = 0 and $SL0_x$ = 1. The output buffer is disabled. Except for $MC_0$ and $MC_7$ the feedback signal is an adjacent I/O. For $MC_0$ and $MC_7$ the feedback signals are pins 1 and 11. These configurations are summarized in Table 1 and illustrated in Figure 2.

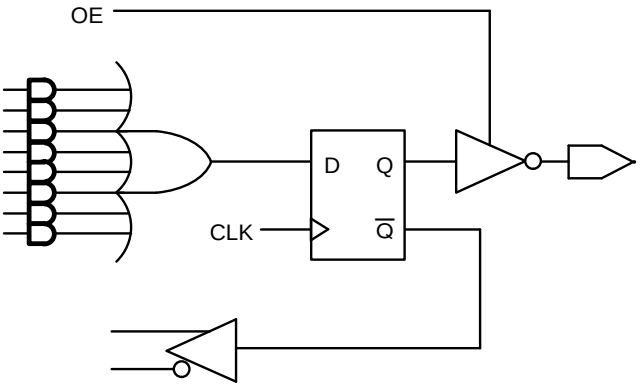
**Table 1. Macrocell Configuration**

| SG0 | SG1 | $SL0_x$ | Cell Configuration | Devices Emulated |
|---|---|---|---|---|
| **Device Uses Registers** | | | | |
| 0 | 1 | 0 | Registered Output | PAL16R8, 16R6, 16R4 |
| 0 | 1 | 1 | Combinatorial I/O | PAL16R6, 16R4 |
| **Device Uses No Registers** | | | | |
| 1 | 0 | 0 | Combinatorial Output | PAL10H8, 12H6, 14H4, 16H2, 10L8, 12L6, 14L4, 16L2 |
| 1 | 0 | 1 | Input | PAL12H6, 14H4, 16H2, 12L6, 14L4, 16L2 |
| 1 | 1 | 1 | Combinatorial I/O | PAL16L8 |

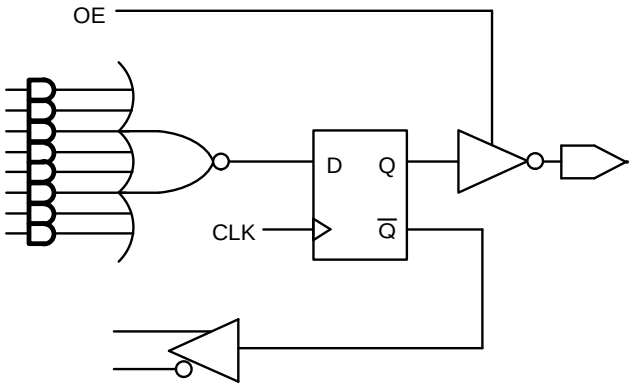
## Programmable Output Polarity

The polarity of each macrocell can be active-high or active-low, either to match output signal needs or to reduce product terms. Programmable polarity allows Boolean expressions to be written in their most compact form (true or inverted), and the output can still be of the desired polarity. It can also save “DeMorganizing” efforts.

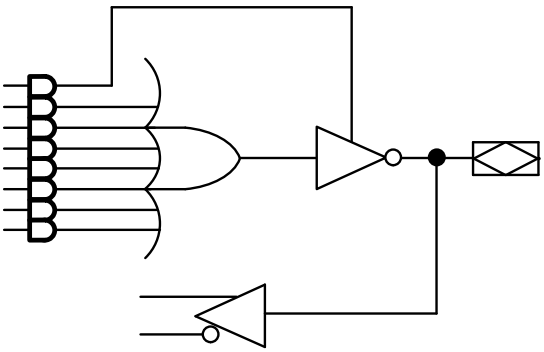
Selection is through a programmable bit $SL1_x$ which controls an exclusive-OR gate at the output of the AND/OR logic. The output is active high if $SL1_x$ is 1 and active low if $SL1_x$ is 0.



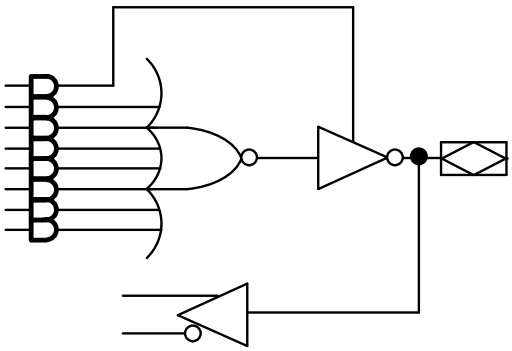

**Registered Active Low**



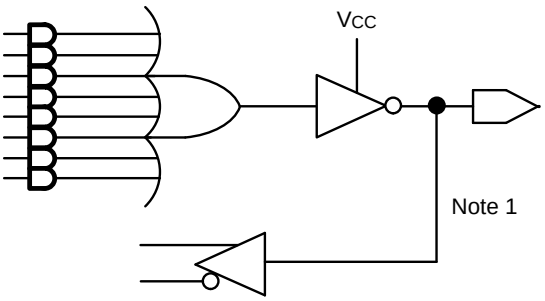

**Registered Active High**



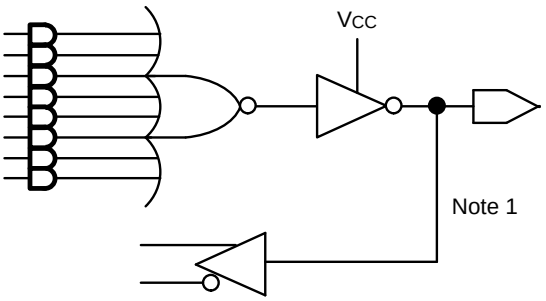
**Combinatorial I/O Active Low**



**Combinatorial I/O Active High**



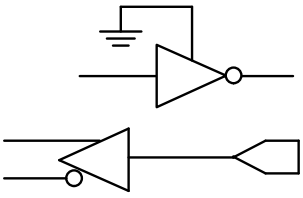

**Combinatorial Output Active Low**




**Combinatorial Output Active High**

***Notes:***

1. *Feedback is not available on pins 15 and 16 in the combinatorial output mode.*
2. *This configuration is not available on pins 15 and 16.*




**Dedicated Input**

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**Figure 2. Macrocell Configurations**

## Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE16V8 will depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be HIGH. If combinatorial is selected, the output will be a function of the logic.

## Register Preload

The register on the PALCE16V8 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

## Security Bit

A security bit is provided on the PALCE16V8 as a deterrent to unauthorized copying of the array configuration patterns. Once programmed, this bit defeats readback and verification of the programmed pattern by a device programmer, securing proprietary designs from competitors. The bit can only be erased in conjunction with the array during an erase cycle.

## Electronic Signature Word

An electronic signature word is provided in the PALCE16V8 device. It consists of 64 bits of programmable memory that can contain user-defined data. The signature data is always available to the user independent of the security bit.

## Programming and Erasing

The PALCE16V8 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Erasure is automatically performed by the programming hardware. No special erase operation is required.

## Quality and Testability

The PALCE16V8 offers a very high level of built-in quality. The erasability of the device provides a direct means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

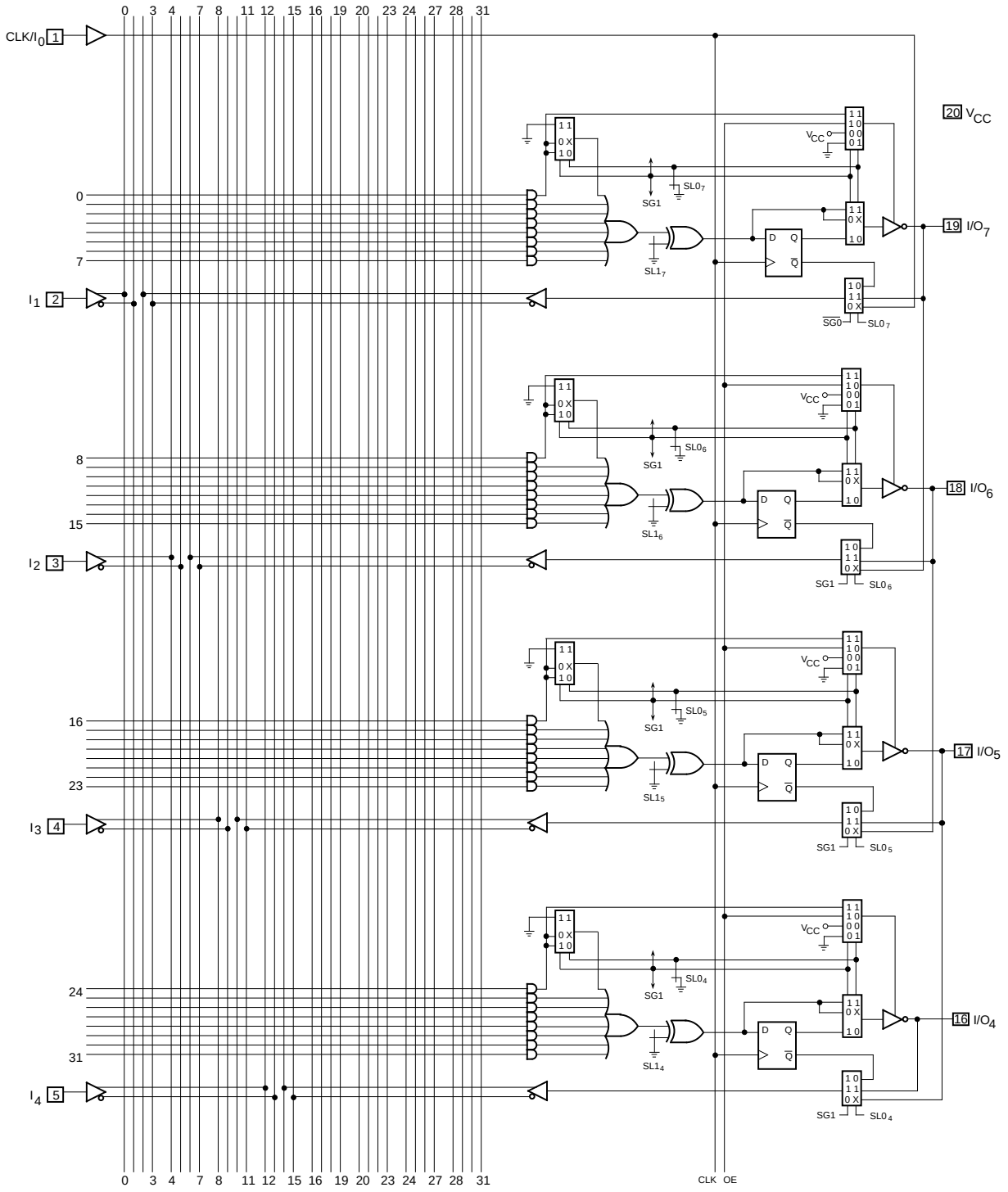
## Technology

The high-speed PALCE16V8 is fabricated with AMD's advanced electrically erasable (EE) CMOS process. The array connections are formed with proven EE cells. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clean switching.

## PCI Compliance

The PALCE22V10H-7/10 is fully compliant with the *PCI Local Bus Specification* published by the PCI Special Interest Group. The PALCE22V10H-7/10's predictable timing ensures compliance with the PCI AC specifications independent of the design.

## LOGIC DIAGRAM

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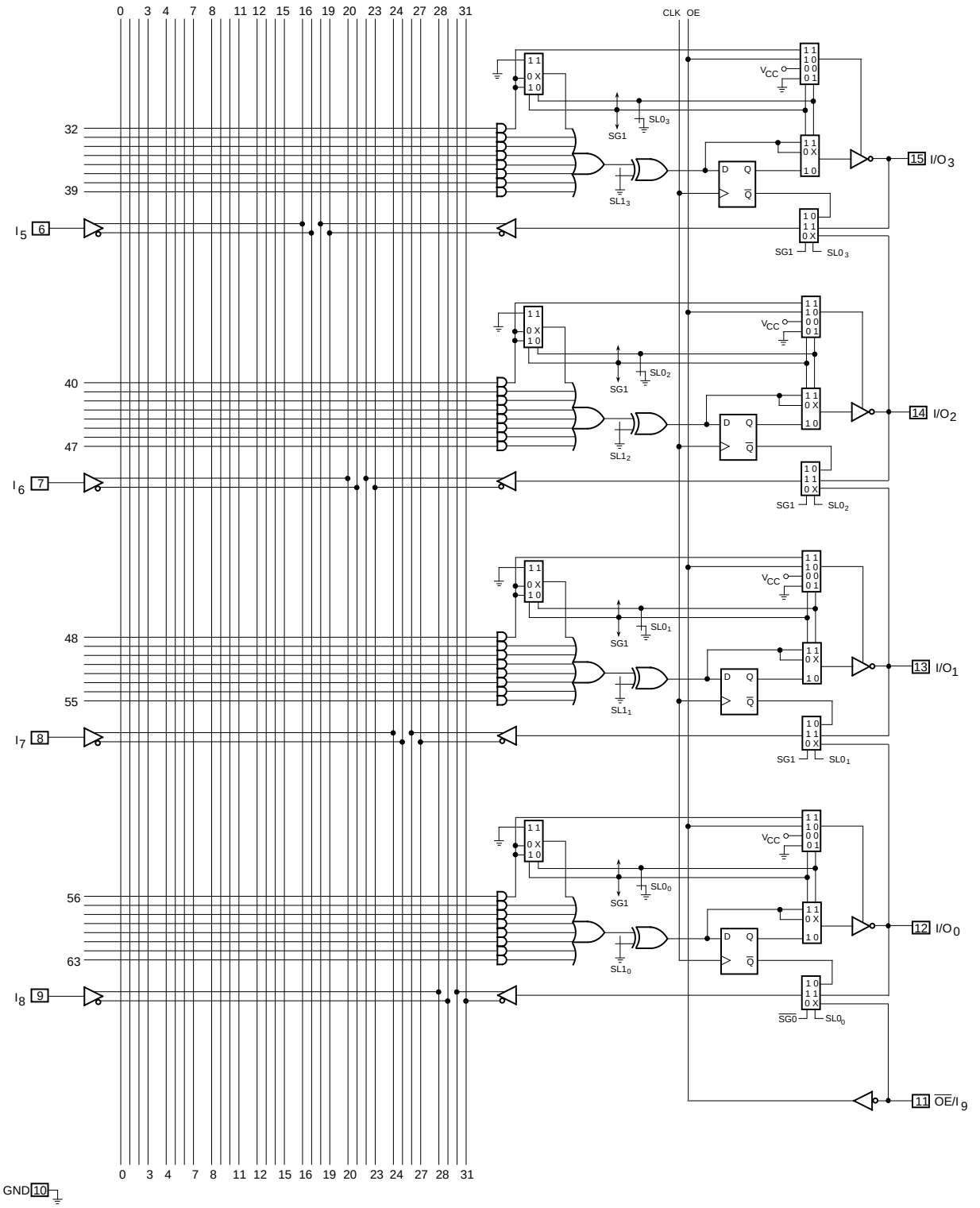
## LOGIC DIAGRAM (continued)




16493D-6
(concluded)

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

DC Output or I/O
Pin Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
($T_A$ = 0°C to 75°C) . . . . . 100 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Temperature ($T_A$) Operating
in Free Air . . . . . 0°C to +75°C

Supply Voltage ($V_{CC}$) with
Respect to Ground . . . . . +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.25 V, $V_{CC}$ = Max (Note 2) | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0 V, $V_{CC}$ = Max (Note 2) | | –100 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.25 V, $V_{CC}$ = Max<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0 V, $V_{CC}$ = Max<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | –100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | –30 | –150 | mA |
| $I_{CC}$ (Static) | Supply Current | Outputs Open ($I_{OUT}$ = 0 mA), $V_{IN}$ = 0 V<br>$V_{CC}$ = Max | | 125 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Descriptions | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | f = 1 MHz | 8 | pF |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | Min (Note 5) | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 1 | 5 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 3 | | ns |
| $t_H$ | Hold Time | | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | 1 | 4 | ns |
| $t_{SKEWR}$ | Skew Between Registered Outputs (Note 4) | | | | 1 | ns |
| $t_{WL}$ | Clock Width | LOW | | 3 | | ns |
| $t_{WH}$ | | HIGH | | 3 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 3) | External Feedback | $1/(t_S+t_{CO})$ | 142.8 | | MHz |
| | | Internal Feedback ($f_{CNT}$), | $1/(t_S+t_{CF})$ (Note 6) | 166 | | MHz |
| | | No Feedback | $1/(t_{WH}+t_{WL})$ | 166 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | 1 | 6 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | 1 | 5 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 2 | 6 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | 2 | 5 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *Output delay minimums for $t_{PD}$, $t_{CO}$, $t_{PZX}$, $t_{PXZ}$, $t_{EA}$, and $t_{ER}$ are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
6. *$t_{CF}$ is a calculated value and is not guaranteed. $t_{CF}$ can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – $t_S$.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature with Power Applied . . . . . –55°C to +125°C

Supply Voltage with Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –0.5 V to $V_{CC}$ + 1.0 V

DC Output or I/O Pin Voltage . . . . . –0.5 V to $V_{CC}$ + 1.0 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current ($T_A$ = 0°C to +75°C) . . . . . 100 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

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Supply Voltage ($V_{CC}$) with Respect to Ground . . . . . +4.75 V to +5.25 V

*Operating Ranges define those limits between which the functionality of the device is guaranteed.*

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| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$ $V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.5 V, $V_{CC}$ = Max (Note 2) | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0 V, $V_{CC}$ = Max (Note 2) | | –100 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.5 V, $V_{CC}$ = Max, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ (Note 2) | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0 V, $V_{CC}$ = Max $V_{IN}$ = $V_{IL}$ or $V_{IH}$ (Note 2) | | –100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | –30 | –150 | mA |
| $I_{CC}$ (Dynamic) | Supply Current | Outputs Open, ($I_{OUT}$ = 0 mA), $V_{CC}$ = Max, f = 25 MHz | | 115 | mA |

***Notes:***

1. *These are absolute values with respect to the device ground and all overshoots due to system and tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be tested at a time. Duration of the short-circuit test should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Descriptions | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | f = 1 MHz | 8 | pF |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | Min (Note 5) | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | 8 Outputs Switching | 3 | 7.5 | ns |
| | | | 1 Output Switching | 3 | 7 | ns |
| $t_S$ | Setup Time from Input or Feedback | | | 5 | | ns |
| $t_H$ | Hold Time | | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | 1 | 5 | ns |
| $t_{SKEWR}$ | Skew Between Registered Outputs (Note 4) | | | | 1 | ns |
| $t_{WL}$ | Clock Width | LOW | | 4 | | ns |
| $t_{WH}$ | | HIGH | | 4 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 3) | External Feedback | $1/(t_S + t_{CO})$ | 100 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | $1/(t_S + t_{CF})$ (Note 6) | 125 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | 125 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | 1 | 6 | ns |
| $t_{PXA}$ | $\overline{OE}$ to Output Disable | | | 1 | 6 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 3 | 9 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | 3 | 9 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Skew testing takes into account pattern and switching direction differences between outputs that have equal loading.*
5. *Output delay minimums for $t_{PD}$, $t_{CO}$, $t_{PZX}$, $t_{PXZ}$, $t_{EA}$, and $t_{ER}$ are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
6. *$t_{CF}$ is a calculated value and is not guaranteed. $t_{CF}$ can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – $t_S$.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

DC Output or I/O
Pin Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
($T_A$ = –40°C to +85°C) . . . . . 100 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Temperature ($T_A$) Operating
in Free Air . . . . . 0°C to +75°C

Supply Voltage ($V_{CC}$) with
Respect to Ground . . . . . +4.75 V to +5.25 V

**Industrial (I) Devices**

Temperature ($T_A$) Operating
in Free Air . . . . . –40°C to +85°C

Supply Voltage ($V_{CC}$) with
Respect to Ground . . . . . +4.5 V to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.25 V, $V_{CC}$ = Max (Note 2) | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0 V, $V_{CC}$ = Max (Note 2) | | –100 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.25 V, $V_{CC}$ = Max<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0 V, $V_{CC}$ = Max<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | –100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V $V_{CC}$ = Max (Note 3) | –30 | –150 | mA |
| $I_{CC}$ (Dynamic) | Commercial Supply Current | Outputs Open ($I_{OUT}$ = 0 mA)<br>$V_{CC}$ = Max, f = 15 MHz | | 115 | mA |
| | Industrial Supply Current | | | 130 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Descriptions | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | f = 1 MHz | 8 | pF |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | Min (Note 4) | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 3 | 10 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 7.5 | | ns |
| $t_H$ | Hold Time | | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | 3 | 7.5 | ns |
| $t_{WL}$ | Clock Width | LOW | | 6 | | ns |
| $t_{WH}$ | | HIGH | | 6 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 3) | External Feedback | $1/(t_S + t_{CO})$ | 66.7 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | $1/(t_S + t_{CF})$ (Note 5) | 71.4 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | 83.3 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | 2 | 10 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | 2 | 10 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 3 | 10 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | 3 | 10 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for $t_{PD}$, $t_{CO}$, $t_{PZX}$, $t_{PXZ}$, $t_{EA}$, and $t_{ER}$ are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
5. *$t_{CF}$ is a calculated value and is not guaranteed. $t_{CF}$ can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – $t_S$.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to +7.0 V

DC Input Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

DC Output or I/O
Pin Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
($T_A$ = 0°C to 75°C) . . . . . 100 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Temperature ($T_A$) Operating
in Free Air . . . . . 0°C to +75°C

Supply Voltage ($V_{CC}$) with
Respect to Ground . . . . . +4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

| Parameter Symbol | Parameter Description | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{CC}$ = Min | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{CC}$ = Min | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.25 V, $V_{CC}$ = Max (Note 2) | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0 V, $V_{CC}$ = Max (Note 2) | | –100 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.25 V, $V_{CC}$ = Max<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0 V, $V_{CC}$ = Max<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | –100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | –30 | –150 | mA |
| $I_{CC}$ | Supply Current (Dynamic) | Outputs Open ($I_{OUT}$ = 0 mA)<br>$V_{CC}$ = Max, f = 15 MHz | | 55 | mA |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Descriptions | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | f = 1 MHz | 8 | pF |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | Min (Note 4) | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | 3 | 10 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 7.5 | | ns |
| $t_H$ | Hold Time | | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | 3 | 7.5 | ns |
| $t_{WL}$ | Clock Width | LOW | | 6 | | ns |
| $t_{WH}$ | | HIGH | | 6 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 3) | External Feedback | $1/(t_S + t_{CO})$ | 66.7 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | $1/(t_S + t_{CF})$ (Note 5) | 71.4 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | 83.3 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | 2 | 10 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | 2 | 10 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | 3 | 10 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | 3 | 10 | ns |

***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *Output delay minimums for $t_{PD}$, $t_{CO}$, $t_{PZX}$, $t_{PXZ}$, $t_{EA}$, and $t_{ER}$ are defined under best case conditions. Future process improvements may alter these values therefore, minimum values are recommended for simulation purposes only.*
5. *$t_{CF}$ is a calculated value and is not guaranteed. $t_{CF}$ can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – $t_S$.*

## ABSOLUTE MAXIMUM RATINGS

Storage Temperature . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –55°C to +125°C

Supply Voltage with
Respect to Ground . . . . . –0.5 V to + 7.0 V

DC Input Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

DC Output or I/O
Pin Voltage . . . . . –0.5 V to $V_{CC}$ + 0.5 V

Static Discharge Voltage . . . . . 2001 V

Latchup Current
($T_A$ = –40°C to +85°C) . . . . . 100 mA

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

## OPERATING RANGES

**Commercial (C) Devices**

Temperature ($T_A$) Operating
in Free Air . . . . . 0°C to +75°C

Supply Voltage ($V_{CC}$) with
Respect to Ground . . . . . +4.75 V to +5.25 V

**Industrial (I) Devices**

Temperature ($T_A$) Operating
in Free Air . . . . . –40°C to +85°C

Supply Voltage ($V_{CC}$) with
Respect to Ground . . . . . +4.5 V to +5.5 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

## DC CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges

| Parameter Symbol | Parameter Description | Test Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –3.2 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{CC}$ = Min | | 2.4 | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 24 mA $V_{IN}$ = $V_{IH}$ or $V_{IL}$<br>$V_{CC}$ = Min | | | 0.5 | V |
| $V_{IH}$ | Input HIGH Voltage | Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1) | | 2.0 | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed Input Logical LOW Voltage for all Inputs (Note 1) | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Leakage Current | $V_{IN}$ = 5.25 V, $V_{CC}$ = Max (Note 2) | | | 10 | µA |
| $I_{IL}$ | Input LOW Leakage Current | $V_{IN}$ = 0 V, $V_{CC}$ = Max (Note 2) | | | –100 | µA |
| $I_{OZH}$ | Off-State Output Leakage Current HIGH | $V_{OUT}$ = 5.25 V, $V_{CC}$ = Max<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | | 10 | µA |
| $I_{OZL}$ | Off-State Output Leakage Current LOW | $V_{OUT}$ = 0 V, $V_{CC}$ = Max<br>$V_{IN}$ = $V_{IH}$ or $V_{IL}$ (Note 2) | | | –100 | µA |
| $I_{SC}$ | Output Short-Circuit Current | $V_{OUT}$ = 0.5 V, $V_{CC}$ = Max (Note 3) | | –30 | –150 | mA |
| $I_{CC}$ (Dynamic) | Commercial Supply Current | Outputs Open ($I_{OUT}$ = 0 mA)<br>$V_{CC}$ = Max, f = 15 MHz | H | | 90 | mA |
| | | | Q | | 55 | |
| $I_{CC}$ (Dynamic) | Industrial Supply Current | Outputs Open ($I_{OUT}$ = 0 mA)<br>$V_{CC}$ = Max, f = 15 MHz | H | | 130 | mA |
| | | | Q | | 65 | |

***Notes:***

1. *These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.*
2. *I/O pin leakage is the worst case of $I_{IL}$ and $I_{OZL}$ (or $I_{IH}$ and $I_{OZH}$).*
3. *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second. $V_{OUT}$ = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.*

## CAPACITANCE (Note 1)

| Parameter Symbol | Parameter Descriptions | Test Conditions | | Typ | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$ = 2.0 V | $V_{CC}$ = 5.0 V, $T_A$ = 25°C, f = 1 MHz | 5 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$ = 2.0 V | | 8 | pF |

***Note:***

1. *These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.*

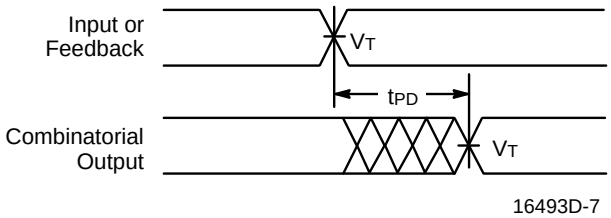
## SWITCHING CHARACTERISTICS over COMMERCIAL and INDUSTRIAL operating ranges (Note 2)

| Parameter Symbol | Parameter Description | | | -15 | | -20 | | -25 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $t_{PD}$ | Input or Feedback to Combinatorial Output | | | | 15 | | 20 | | 25 | ns |
| $t_S$ | Setup Time from Input or Feedback to Clock | | | 12 | | 13 | | 15 | | ns |
| $t_H$ | Hold Time | | | 0 | | 0 | | 0 | | ns |
| $t_{CO}$ | Clock to Output | | | | 10 | | 11 | | 12 | ns |
| $t_{WL}$ | Clock Width | LOW | | 8 | | 10 | | 12 | | ns |
| $t_{WH}$ | | HIGH | | 8 | | 10 | | 12 | | ns |
| $f_{MAX}$ | Maximum Frequency (Note 3) | External Feedback | $1/(t_S + t_{CO})$ | 45.5 | | 41.6 | | 37 | | MHz |
| | | Internal Feedback ($f_{CNT}$) | $1/(t_S + t_{CO})$ (Note 4) | 50 | | 45.4 | | 40 | | MHz |
| | | No Feedback | $1/(t_{WH} + t_{WL})$ | 62.5 | | 50.0 | | 41.6 | | MHz |
| $t_{PZX}$ | $\overline{OE}$ to Output Enable | | | | 15 | | 18 | | 20 | ns |
| $t_{PXZ}$ | $\overline{OE}$ to Output Disable | | | | 15 | | 18 | | 20 | ns |
| $t_{EA}$ | Input to Output Enable Using Product Term Control | | | | 15 | | 18 | | 20 | ns |
| $t_{ER}$ | Input to Output Disable Using Product Term Control | | | | 15 | | 18 | | 20 | ns |

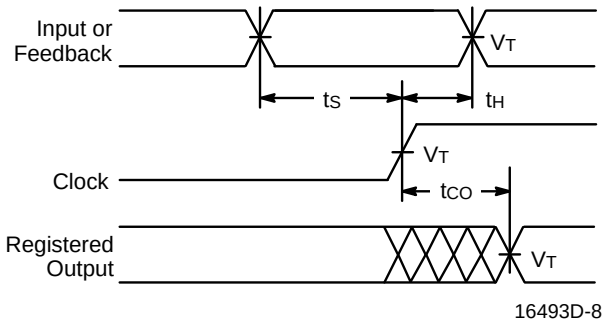
***Notes:***

2. *See Switching Test Circuit for test conditions.*
3. *These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.*
4. *$t_{CF}$ is a calculated value and is not guaranteed. $t_{CF}$ can be found using the following equation: $t_{CF} = 1/f_{MAX}$ (internal feedback) – $t_S$.*

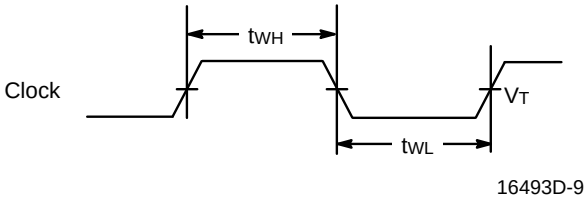
## SWITCHING WAVEFORMS



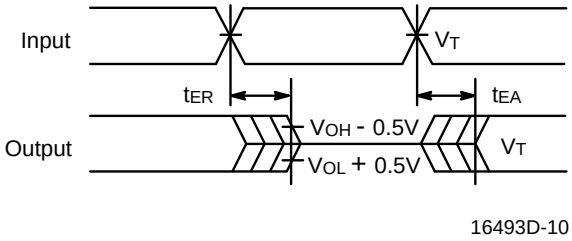

**Combinatorial Output**



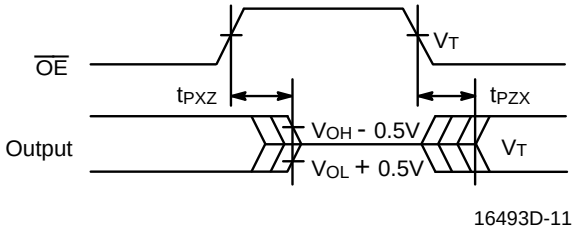

**Registered Output**




**Clock Width**




**Input to Output Disable/Enable**




**$\overline{OE}$ to Output Disable/Enable**

***Notes:***

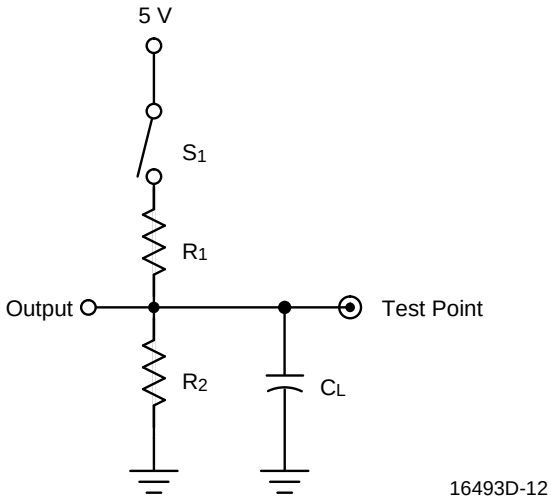
1. *$V_T$ = 1.5 V*
2. *Input pulse amplitude 0 V to 3.0 V.*
3. *Input rise and fall times 2 ns – 5 ns typical.*

## KEY TO SWITCHING WAVEFORMS

| WAVEFORM | INPUTS | OUTPUTS |
|---|---|---|
| | Must be Steady | Will be Steady |
| | May Change from H to L | Will be Changing from H to L |
| | May Change from L to H | Will be Changing from L to H |
| | Don't Care, Any Change Permitted | Changing, State Unknown |
| | Does Not Apply | Center Line is High-Impedance "Off" State |

KS000010-PAL

## SWITCHING TEST CIRCUIT

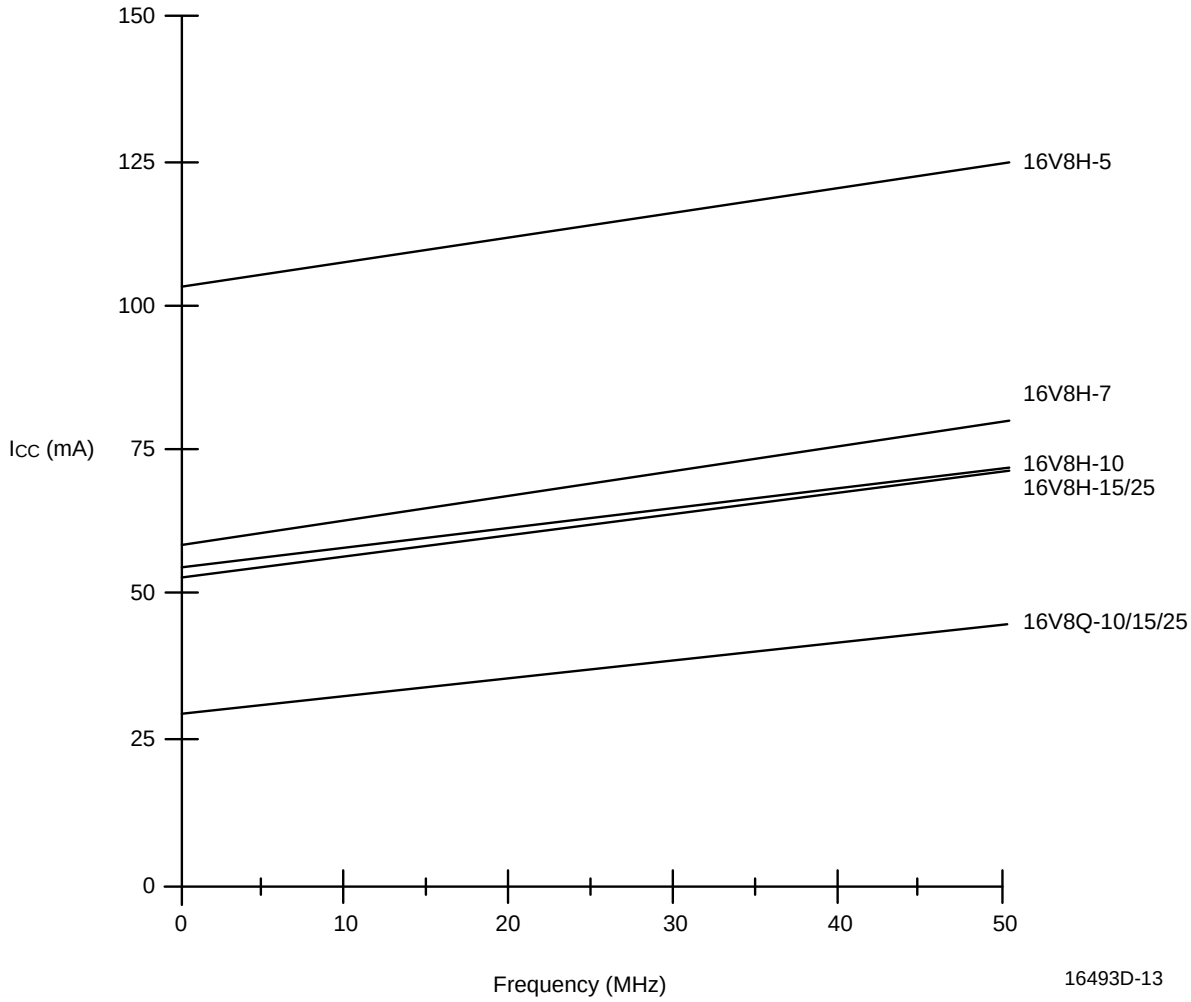



16493D-12

| Specification | $S_1$ | $C_L$ | Commercial | | Measured Output Value |
|---|---|---|---|---|---|
| | | | $R_1$ | $R_2$ | |
| $t_{PD}$, $t_{CO}$ | Closed | 50 pF | 200 Ω | 390 Ω | 1.5 V |
| $t_{EA}$ | Z → H: Open<br>Z → L: Closed | | | | 1.5 V |
| $t_{ER}$ | H → Z: Open<br>L → Z: Closed | 5 pF | | H-5:<br>200 Ω | H → Z: $V_{OH}$ – 0.5 V<br>L → Z: $V_{OL}$ + 0.5 V |

## TYPICAL $I_{CC}$ CHARACTERISTICS

**$V_{CC}$ = 5 V, $T_A$ = 25°C**




**$I_{CC}$ vs. Frequency**

*The selected "typical" pattern utilized 50% of the device resources. Half of the macrocells were programmed as registered, and the other half were programmed as combinatorial. Half of the available product terms were used for each macrocell. On any vector, half of the outputs were switching.*

*By utilizing 50% of the device, a midpoint is defined for $I_{CC}$. From this midpoint, a designer may scale the $I_{CC}$ graphs up or down to estimate the $I_{CC}$ requirements for a particular design.*

## ENDURANCE CHARACTERISTICS

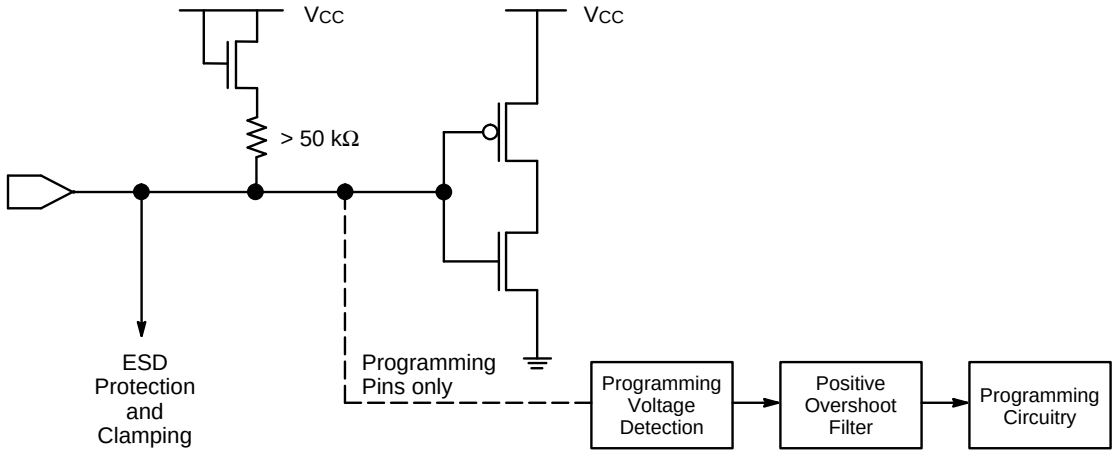
The PALCE16V8 is manufactured using AMD's advanced Electrically Erasable process. This technology uses an EE cell to replace the fuse link used in bipolar parts. As a result, the device can be erased and reprogrammed—a feature which allows 100% testing at the factory.

| Symbol | Parameter | Test Conditions | Min | Unit |
|---|---|---|---|---|
| $t_{DR}$ | Min Pattern Data Retention Time | Max Storage Temperature | 10 | Years |
| | | Max Operating Temperature | 20 | Years |
| N | Min Reprogramming Cycles | Normal Programming Conditions | 100 | Cycles |

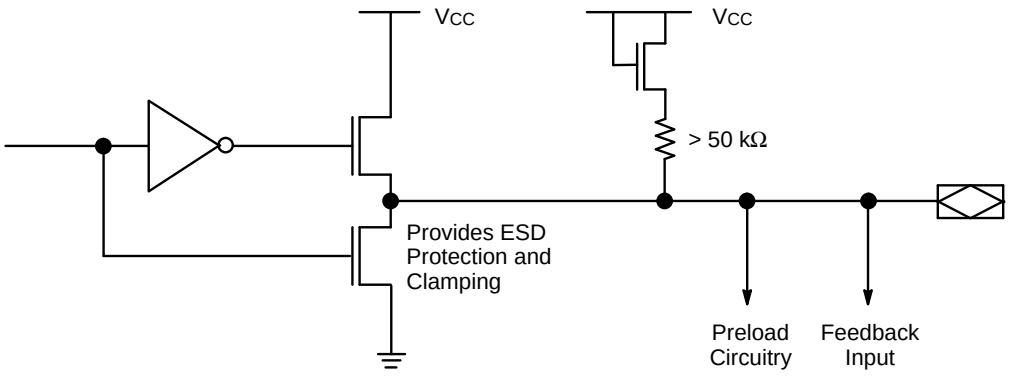
## ROBUSTNESS FEATURES

PALCE16V8X-X/5 devices have some unique features that make them extremely robust, especially when operating in high-speed design environments. Pull-up resistors on inputs and I/O pins cause unconnected pins to default to a known state. Input clamping circuitry limits negative overshoot, eliminating the possibility of false clocking caused by subsequent ringing. A special noise filter makes the programming circuitry completely insensitive to any positive overshoot that has a pulse width of less than about 100 ns for the /5 versions. Selected /4 devices are also being retrofitted with these robustness features. See chart below for device listings.

## INPUT/OUTPUT EQUIVALENT SCHEMATICS FOR /5 VERSIONS AND SELECTED /4 VERSIONS*




**Typical Input**




**Typical Output**

16493D-14

*

| Device | Rev Letter | |
|---|---|---|
| | Filter Only | Filter and Pullups |
| PALCE16V8H-10 | E, F, K | L |
| PALCE16V8H-15 | D, E, F, G, I, J, K | L, M |
| PALCE16V8Q-15 | D, G, J | M |
| PALCE16V8H-25 | D, G, J | M |
| PALCE16V8Q-25 | D, G, J | M |

***Topside Marking:***

*AMD CMOS PLD's are marked on the top of the package in the following manner:*

*PALCEXXXX*
*Date Code (3 numbers) Lot ID (4 characters)– –(Rev. Letter)*

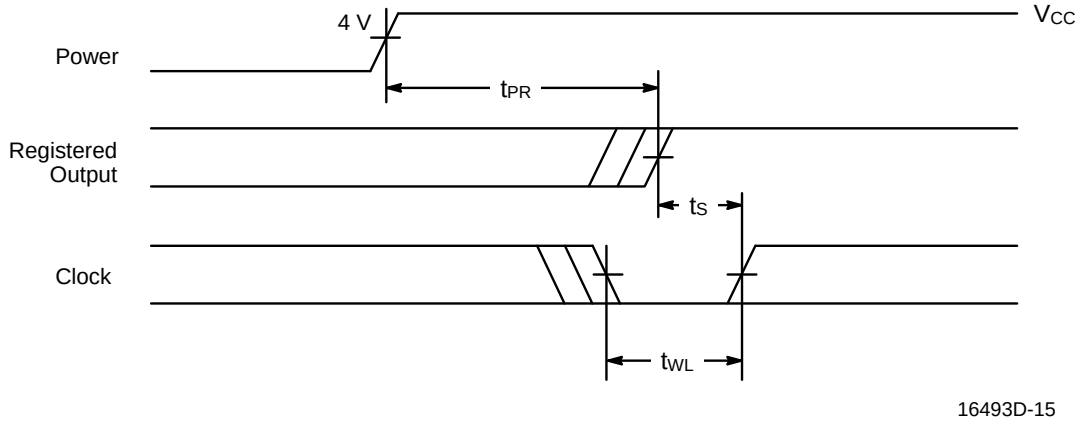
*The Lot ID and Rev Letter are separated by two spaces.*

## POWER-UP RESET

The PALCE16V8 has been designed with the capability to reset during system power-up. Following power-up, all flip-flops will be reset to LOW. The output state will be HIGH independent of the logic polarity. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways $V_{CC}$ can rise to its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

- The $V_{CC}$ rise must be monotonic.
- Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

| Parameter Symbol | Parameter Descriptions | Min | Max | Unit |
|---|---|---|---|---|
| $t_{PR}$ | Power-Up Reset Time | | 1000 | ns |
| $t_S$ | Input or Feedback Setup Time | See Switching Characteristics | | |
| $t_{WL}$ | Clock Width LOW | | | |




**Power-Up Reset Waveform**

## TYPICAL THERMAL CHARACTERISTICS

### /4 Devices (PALCE16V8H-10/4)

Measured at 25°C ambient. These parameters are not tested.

| Parameter Symbol | Parameter Description | | Typ | | Unit |
|---|---|---|---|---|---|
| | | | PDIP | PLCC | |
| $\theta_{jc}$ | Thermal Impedance, Junction to Case | | 25 | 22 | °C/W |
| $\theta_{ja}$ | Thermal Impedance, Junction to Ambient | | 71 | 64 | °C/W |
| $\theta_{jma}$ | Thermal Impedance, Junction to Ambient with Air Flow | 200 lfpm air | 61 | 55 | °C/W |
| | | 400 lfpm air | 55 | 51 | °C/W |
| | | 600 lfpm air | 51 | 47 | °C/W |
| | | 800 lfpm air | 47 | 45 | °C/W |

### /5 Devices (PALCE16V8H-7/5)

Measured at 25°C ambient. These parameters are not tested.

| Parameter Symbol | Parameter Description | | Typ | | Unit |
|---|---|---|---|---|---|
| | | | PDIP | PLCC | |
| $\theta_{jc}$ | Thermal Impedance, Junction to Case | | 29 | 23 | °C/W |
| $\theta_{ja}$ | Thermal Impedance, Junction to Ambient | | 70 | 61 | °C/W |
| $\theta_{jma}$ | Thermal Impedance, Junction to Ambient with Air Flow | 200 lfpm air | 64 | 53 | °C/W |
| | | 400 lfpm air | 58 | 47 | °C/W |
| | | 600 lfpm air | 53 | 44 | °C/W |
| | | 800 lfpm air | X | X | °C/W |

***Plastic $\theta_{jc}$ Considerations***

*The data listed for plastic $\theta_{jc}$ are for reference only and are not recommended for use in calculating junction temperatures. The heat-flow paths in plastic-encapsulated devices are complex, making the $\theta_{jc}$ measurement relative to a specific location on the package surface. Tests indicate this measurement reference point is directly below the die-attach area on the bottom center of the package. Furthermore, $\theta_{jc}$ tests on packages are performed in a constant-temperature bath, keeping the package surface at a constant temperature. Therefore, the measurements can only be used in a similar environment.*